NASIC: Nanoscale Application-Specific ICs and Architectures
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Background
- Carbon nanotubes (CNTs) - C.Dekker, 1999
- Silicon nanowires (SiNWs) - A.M.Morales, 1998
- Nanojunctions
  - Diode effect - T.Rueckes, 2000
  - FET effect - Y.Huang, 2000
- Nanogrid - Lauhon et al., Nature 420, 57

Motivation
- We develop circuits and architectures based on carbon nanotubes and silicon nanowires
- A key objective is to preserve density advantages of nano architectures compared to MOS in presence of fabrication and topology constraints
- We make an initial evaluation at system level

Nanoscale Logics
- red wires: p-doped nanowires
- blue wires: n-doped nanowires
- We can build NAND, AND, NOR, OR logic at the junctions of NWs.
First example: 1-bit Full Adder

- Complementary inputs/outputs
- 2-level OR-AND logic
- Pullup/pulldown network

Second Example: 2-bit ALU

- Cascading of 2-level logic
- The results are selected by the multiplexer
- Building multiple logic blocks together can improve area utilization

Bad Area Efficiency in Sequential Circuits: 1-bit D-Flipflop

Dynamic Circuits

- Dynamic circuits: we use it for pipelined structures and temporary storage (shown next)
- Precharge-Evaluate-Hold phase
- Hold phase for cascading
Nano-Latch

- Cascaded dynamic circuits -> NanoLatch
- Nano-Latch: idea for temporary storage
- Nano-Latch is implicit

Interconnection

- Neighbored Tiles are connected by NWs
- Only minor modifications are needed to interconnect neighbored nanotiles
- Global interconnections are provided by MWs

Pipelined structure

Initial System-Level Evaluation


Assumptions

<table>
<thead>
<tr>
<th>Area</th>
<th>NWs to pitch 4nm</th>
<th>NWs to pitch 90nm</th>
<th>NWs to pitch 30nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>1.8cm</td>
<td>1.8cm</td>
<td>1.8cm</td>
</tr>
<tr>
<td># of transistors</td>
<td>10^3</td>
<td>2.10^4</td>
<td>variable</td>
</tr>
</tbody>
</table>
Conclusion

- Nanodevices have great density advantage over MOS technology, but fabrication (such as high defect density) and topology constraints may break down this advantage.
- Based on our fabric architecture and initial study, even under conservative assumptions, nanoscale systems could still have significant advantages over MOS systems.
- Taking physical layer aspects into consideration when designing nano architectures is key.