

Morteza Fayyazi

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EDUCATION

Northeastern University, Boston, MA (April 2005) (expected)

Ph.D. Computer Engineering, Minor in Computer Science and Signal Processing (GPA: 3.8/4)

- **Research:** Design, evaluation and implementation of parallel algorithms for crossbar scheduling. Improving performance and fault tolerance of packet switch architectures (supported by CenSSIS). Architectural modeling and performance improvement of BlackFin DSP processor (supported by ADI). Evaluation of FX!32, binary translation system (supported by Compaq).
- **Course work:** Combinatorial optimization, analysis of algorithms, parallel computing, computer architecture, digital signal processing, applied probability, pattern recognition, operating system, software engineering, compiler design.
- **Experience:** Teaching assistant for parallel computing, logic design, and HDL and synthesis courses. Research assistant since 1999 (supported by Analog Devices Inc., Compaq and CenSSIS).

University of Tehran, Tehran, Iran (1998)

Master of Science in Computer Engineering

- Ranked among top two percent in the national graduate level university entrance exam.
- **Research:** Hardware acceleration of automatic test pattern generation for digital circuits.
- **Course work:** Digital system design using VHDL, digital system testing and testable design, fault tolerant systems, computer architecture, parallel processing, VLSI design, neural networks, design of special purpose processors for intelligent systems.
- **Experience:** Teaching assistant for logic design and microprocessors courses.

Sharif University of Technology, Tehran, Iran (1995)

Bachelor of Science in Computer Engineering

- Ranked among top 0.2 percent in the national university entrance exam.
- **Research:** Programmable Logic Controllers (PLC).

WORK EXPERIENCE

ATI Research Inc., Marlborough, USA Summer 2004

- *Internship:* Design and implementation of an integer linear programming approach to instruction scheduling for graphics processors.

Valence Semiconductor Inc., Dubai, UAE Summer and Fall 2001

- *Internship:* Design, simulation, synthesis and verification of an Ethernet packet switch.

VLSI laboratory, Tehran, Iran 1997 - 1999

- *Design engineer:* Design, simulation, synthesis and verification of UTS-DSP, a CISC DSP processor compatible with Texas Instrument TMS320C54x DSP processor at instruction level.

Esfahan University, Golpayegan, Iran Spring 1998

- *Instructor:* Teaching fundamentals of computer engineering course to undergraduate students.

Allameh Helli High school, Tehran, Iran 1995 - 1997

- *Teacher:* Teaching Basic programming language to high school students.

PUBLICATIONS

- 1) M. Fayyazi, D. Kaeli, W. Meleis, "An Adjustable Linear Time Parallel Algorithm for Maximum Weight Bipartite Matching," submitted to *Information Processing Letters*.
- 2) M. Fayyazi, D. Kaeli, W. Meleis, "Linear-Time Parallel Algorithms for Maximum Weight Bipartite Matching," submitted to *ACM Symposium on Parallelism in Algorithms and Architectures (SPAA'05)*.
- 3) M. Fayyazi, N. Rubin, C. Reeve, "Integrating Splitting Transformations into an ILP Instruction Scheduler," submitted to *ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES'05)*.
- 4) M. Fayyazi, D. Kaeli, W. Meleis, "Parallel Maximum Weight Bipartite Matching Algorithms for Scheduling in Input-Queued Switches," *IEEE International Parallel and Distributed Processing Symposium (IPDPS 2004)*, pp. 26-30, Santa Fe, New Mexico, April 2004.
- 5) M. Fayyazi, D. Kaeli, Z. Navabi, "Dynamic Input Buffer Allocation (DIBA) for Fault Tolerant Ethernet Packet Switching," *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'03)*, pp. 819-823, Las Vegas, Nevada, June 2003.
- 6) M. Fayyazi, D. Kaeli, "Localized Message Passing Structure for High Speed Ethernet Packet Switching," *International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'02)*, pp. 1551-1557, Las Vegas, Nevada, June 2002.
- 7) M. Fayyazi, Z. Navabi, "Accelerating Test Generation by VLSI Hardware Emulation," *9th IEEE North Atlantic Test Workshop*, pp. 84-89, Gloucester, MA, May 2000.
- 8) P. J. Drongowski, D. Hunter, M. Fayyazi, D. Kaeli, J. Casmira, "Studying the Performance of the FX132 Binary Translation System," *1st IEEE Workshop on Binary Translation*, Newport Beach, CA, October 1999.
- 9) M. Fayyazi, M. R. Movahedin, Z. Navabi, P. A. Riahi, A. G. Dezfoli, "An Efficient CPU Architecture for DSP Processors," *ICEE'99*, Tehran, Iran, June 1999.
- 10) P. A. Riahi, M. R. Movahedin, M. Fayyazi, "Core Architecture of UTS-DSP Processor," *ICEE'99*, Tehran, Iran, June 1999.
- 11) M. Fayyazi, Z. Navabi, "Using VHDL Neural Network Models for Automatic Test Generation," *2nd Workshop on Libraries, Component Modeling and Quality Assurance*, Toledo, Spain, April 1997.

RESEARCH INTERESTS

Developing and implementing parallel and distributed algorithms
Developing optimization algorithms for compilers
Optimizing performance of scientific programs
Providing algorithms for hardware testing
Modeling and simulating hardware components

SKILLS

MPI, C, C++, and Java programming languages, and UNIX, Linux, and Windows operating systems
AMPL modeling language, and CPLEX and GLPK solvers for ILP formulations
VHDL and Verilog hardware description languages
Assembly code development and optimization for ATI graphics processors
Assembly code development and optimization for ADI and TI DSP processors
Cadence and Synopsys synthesis tools

PROFESSIONAL AFFILIATIONS

Awarded membership in Phi Kappa Phi
Institute of Electrical and Electronics Engineers (IEEE)
IEEE Computer Society
IEEE Computer Society Technical Committee on Parallel Processing

REFERENCES

Prof. David Kaeli, ECE department, Northeastern University, Boston, MA
Prof. Waleed Meleis, ECE department, Northeastern University, Boston, MA
Chris Reeve, director of compiler group, ATI Research Inc., Marlborough, MA

Contact information of the references available on request