

Marcos R. de Alba

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Objective

To perform development and research on microprocessors at microarchitecture or circuit level. To develop microprocessor and microcontroller simulators and optimizations to existing ones.

Education

Northeastern University, Boston, MA.
PhD in Computer Engineering, minor in Computer Architecture. To get degree on June 2004.

Northeastern University, Boston, MA.
MS in Computer Science, minor in Operating Systems. June 2000.

Monterrey Institute of Technology, State of Mexico, Mexico.
MS in Computer Science, minor in Computer Networks. December 1996.

Metropolitan Autonomous University, Mexico City, Mexico.
BS in Electronic Engineering, minor in digital systems design. December 1993.

Work experience

Intel Microprocessor Research Laboratory, Barcelona Spain.
Development of microarchitecture-level research for estimating and reducing static power.
Development of leakage estimation model at microarchitecture, circuit and transistor levels.
May 2003 - Present.

ECE Department, Northeastern University. Boston, MA.
Research and teaching assistant. Developed research in computer architecture. Taught and graded Digital Systems and Digital Systems Design Laboratory. Topics in digital systems design on FPGAs using Xilinx. September 1999 to December 2002.

Thinking Machines Corporation. Burlington, MA.
Research internship. Analyzed and combined different data mining models. Summer 1998.

ECE Department, Metropolitan Autonomous University, Mexico City, Mexico.
Associate Professor. Taught and graded Digital Computers Organization and Laboratory, Digital Systems Design and Laboratory, Logic Circuits and Computers and Laboratory. October 1994 to August 1997.

ECE and CS Departments, Monterrey Institute of Technology, State of Mexico, Mexico.
Academic Professor. Taught and graded Computer Organization, Digital Circuits, Logic Circuits Design, Laboratory of Electrical Communications. January 1996 to August 1997.

Mexican Metrology Center, Mexican Bank and Ford Motor Company. Mexico City, Mexico.
BAS and Automation Project consultant. Designed, programmed and installed BAS Systems. Designed and built interfaces for industrial robots and PLCs. January 1994 to December 1995.

Publications

de Alba, M. and D. Kaeli. "Characterization and Evaluation of Hardware Loop Unrolling". First Boston Area Architecture Conference, Cambridge, MA, January 30, 2003.

de Alba, M. and D. Kaeli. "Path-based Hardware Loop Prediction". Submitted to the 4th International Conference on Control, Virtual Instrumentation and Digital Systems, to be held in August 26-30, 2002. Pachuca City, Mexico.

Uht, A., Morano, D., Khalafi, A., de Alba, M. and Kaeli, D. "Realizing High IPC Using Time-tagged Resource-Flow Computing", to appear in Euro-Par Conference, August 27-30, 2002, Paderborn, Germany.

de Alba, M. and Kaeli, D. "Runtime Predictability of Loops". In the IEEE 4th Annual Workshop on Workload Characterization, held with the 34th Annual International Symposium on Microarchitecture. Austin Texas, December 1-5, 2001.

de Alba, M. and Kaeli, D. and Kim, E. S. "Dynamic Analysis of Loops". In the 3rd International Conference on Control, Virtual Instrumentation and Digital Systems, August 27-31, 2001. Mexico City, Mexico.

Uht, A., Morano, D., Khalafi, A., de Alba, M., Wenisch, T., Ashouei, M.. "Levo: IPC in the 10's via Resource Flow Computing". Presented at PACT 2001 Work-In-Progress (WIP) Session, September 2001, IEEE TCCA Newsletters, Special Issue.

A. K. Uht, D. Morano, A. Khalafi, M. de Alba, T. Wenisch, M. Ashouei and D. Kaeli. "IPC in the 10's via Resource Flow Computing with Levo". Technical Report No. 092001-001. Dept. of Electrical and Computer Engineering, University of Rhode Island, September 18, 2001.

de Alba, Marcos. "Formal Specification and Verification of an External Memory Manager for the Mach Operating System, using the LOTOS language". MS Thesis, Monterrey Institute of Technology, State of Mexico, Mexico, December 1996.

de Alba Marcos, Petrov Rossen, Forcada Julio. "Measuring the ozone layer from the Earth". Gyros Magazine, Metropolitan Autonomous University, Mexico City, Mexico. Vol. 1, No. 1, October 1994, pp. 37-43.

Developed Software

Perl tool to generate SPICE code automatically from block-level parameterization.

Instrumentation tool to measure the run-time behavior of loops. Co-developer of LevoSim simulator.

Co-developer of SimpleSim: a Mips simulator. Extensions to SimpleScalar computer simulator to implement hardware loop unrolling and loop prediction.

Computer and Technology Skills

Background: Computer architecture, digital hardware synthesis, algorithms and optimization, profiling evaluation, operating and distributed operating systems, parallel computing and programming, principles of programming, human computer interface design, internetworking.

Programming Languages: C, Java, VHDL, Perl, assembly, HTML, FORTRAN, LISP, scheme. Knowledge on C++.

Circuits design tools: Xilinx, Synopsys, Orcad, Picad, Electronics Workbench, PSPICE/HSPICE.

Networking: Client/Server Computing, Ethernet, ATM, MPI, PVM, RMI, RPC, Sockets, TCP/IP.

Performance evaluation tools: ATOM, Strace.

Operating Systems: UNIX (SunOS, Tru64, Linux), Windows, DOS.

Scholarships and Memberships

Northeastern University Computer Architecture Research Group member since September 1999.

IEEE student member.

Fulbright grantee for graduate studies 1997-2000.