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Education

BS EE	1981	Rutgers University
MS CE	1985	Syracuse University
PhD EE	1992	Rutgers University

Positions Held

1981-1986	Staff Engineer, IBM Enterprise Systems, Poughkeepsie, NY
1986-1993	Advisory Engineer, IBM T.J. Watson Research Center, Yorktown Heights, NY
1993-1999	Assistant Professor, Northeastern University, Boston, MA
1999-2005	Associate Professor, Northeastern University, Boston, MA
2001-2002	Visiting Professor, Universitat Politecnica de Cataluyna, Barcelona, Spain
2005-present	Full Professor, Northeastern University, Boston, MA
2010-2013	Associate Dean, College of Engineering, Northeastern University, Boston, MA
2011-present	Honorary Professor, City University, London, England
2014-present	Courtesy Appointment, CCIS, Northeastern University, Boston MA
2014-present	Distinguished Full Professor, COE, Northeastern University, Boston MA

Journal Publications

1. "UMH: A Hardware-baed Unified Memory Hierarchy for Systems with Multiple Discrete GPUs," with A.K. Ziabari, Y. Sun, Y. Ma, D. Schaa, J.L. Abellan, R. Ubal, J. Kim, A. Joshi and D.R. Kaeli, *ACM Transactions on Architecture and Code Optimization*, to appear, 2016.

2. "Diffraction Pattern Simulation of Cellulose Fibrils using Distributed and Quantized Pair Distance," with Y. Zhang, H. Inouye, M. Crowley, L. Yu, D. Kaeli and L. Makowski, *Journal of Applied Crystallography*, 49(6), 2016.

3. "A Framework for Studying New Approaches to Anomaly Detection," with E.N. Yolacan, *International Journal of Information Security Science*, 5(2), 2016, pp. 39-50.

4. "Patterns of Temporal Scaling of Groundwater Level Fluctuation," *Journal of Hydrology*, vol. 536, 2016, pp. 485-495.

5. "Using Benchmarks for Radiation Testing of Microprocessors and FPGAs," with H. Quinn, W.J. Robinson, P. Rech, M. Aquirre, A. Barnard, M. Desogus, L. Entrena, M. Garcia-Valderas, S.M. Guertin, F. Lima Kastensmidt, B.T. Kiddie, A. Sanchez-Clemente, M. Sonza Reorda, L. Sterpone and M. Wirthlin, *IEEE Transactions on Nuclear Science*, Vol. 62, No. 6, 2015, pp. 2547-2554.

6. "Spatiotemporal Changes of CVOC Concentrations in Karst Aquifers: Analysis of Three Decades of Data from Puerto Rico," with X. Yu, R. Ghasemizadeh, I. Padilla, C. Irizarry and A. Alshawabkeh, *Science of the Total Environment*, 2015, pp. 1-10.

7. "A Reuse-Based Refresh Policy for Energy-Aware eDRAM Caches," with A. Valero, S. Petit, J. Sahuquillo and J. Duato, *Microprocessors and Microsystems*, Elsevier, 39(1), 2015, pp. 37-48.

8. "Analyzing Power Efficiency of Optimization Techniques and Algorithms Design Methods for Applications on Heterogeneous Platforms," with Y. Ukidave, A. Kavyan Ziabari, P. Mistry and G. Schirner, *International Journal of High Performance Computing Applications*, 28(2), 2014.

9. "Harnessing the Power of GPUs to Speed Up Feature Selection for Outlier Detection," with F. Azmandian, A. Yilmazer, J. Dy and J.A. Aslam, *Journal of Computer Science and Technology*, 29(3):408-422, 2014.

10. "Aggressive Value Prediction on a GPU," with E. Sun, *International Journal of Parallel Processing*, Springer, 42(1):30-48, 2014.

11. "Accelerated Mesh-based Monte Carlo Methods for Modern CPU Architectures," with Q. Fang, *Biomedical Optics Express*, 3(12):3223-3230, 2012.

12. "Local Kernel Density Ratio-Based Feature Selection," with F. Azmandian, J. Dy, and J.A. Aslam, *Journal of Machine Learning Research*, Vol. 25, pp. 49-64, 2012.

13. "A Sequentially Consistent Multiprocessor Architecture for Out-of-Order Retirement of Instructions," with R. Ubal, J. Sahuquillo, S. Petit and P. Lopez, *IEEE Transactions on Parallel and Distributed Systems*, 23(8):1361-1368, 2012.

14. "Guest Editor's Introduction: Special Issue on High-Performance Computing with Accelerators," with D. Bader and V. Kindratenko, *IEEE Transactions on Parallel and Distributed Systems*, 22(1):3-6, January 2011.

15. "Virtual Machine Monitor-based Lightweight Intrusion Detection," with F. Azmandian, M. Moffie, M. Alshawabkeh, J. Dy and J. Aslam, *ACM Operating Systems Reviews*, July 2011.

16. "Data Structures and Transformations for Physically Based Simulations on a GPU," with P. Mistry, D. Schaa, B. Jang, A. Dvornik and D. Meglan, *High Performance Computing for Computational Science*, Lecture Notes in Computer Science, No. 6449, Springer 2011.

17. "Exploiting Memory Access Patterns to Improve Memory Performance in Data Parallel Architectures," with B. Jang, D. Schaa and P. Mistry, *IEEE Transactions on Parallel and Distributed Computing,* 22(1): 105-118, 2011.

18. "Design and Simulation of Self-Biased Circulators in the Ultra High Frequency Band," with J. Wang, A. Geiler, P. Mistry, V. Harris and C. Vittoria, *Journal of Magnetism and Magnetic Materials*, 324(6): 991-994, 2011.

19. "Accelerating an Imaging Spectroscopy Algorithm for Submerged Marine Environments Using Graphics Processing Units," with J. Goodman and D. Schaa, *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing*, 4(3): 669-676, 2011.

20. "Adventures in Desktop Supercomputing," *Journal of Computing Sciences in Colleges*, 26(2):172, 2010.

21. "AGAMOS: A Graph-Based Approach to Modulo Scheduling for Clustered Microarchitecture," with A. Aleta, J.M. Codina and A. Gonzalez, *IEEE Transactions on Computers*, 58(6):770-783, 2009.

22. "Special issue: General-purpose Processing Using Graphics Processing Units," with M. Leeser, *Journal of Parallel and Distributed Computing*, 68(10): 1305-1306, 2008.

23. "Soft Error Susceptibility Analysis of SRAM-Based FPGAs in High-Performance Information Systems," with G. Asadi, V. Sridharan, T. Tahoori and K. Granlund, *IEEE Transactions on Nuclear Science (TNS)*, 54(6): 2714-2726, Dec. 2007.

24. "Characterization of File IO Activity for SPEC CPU2006," with D. Ye and J. Ray, *Special Issue of ACM SIGARCH Computer Architecture News: SPEC CPU2006 Analysis*, 35(1):112-117, 2007.

25. "Towards the Development of an Error Checker for Radiotherapy Treatment Plans: A Preliminary Study," with F. Azmandian and S. Jiang, *Physics in Medicine and Biology*, 52/2007, pp. 6711-6524.

26. "Addressing a Workload Characterization Study of the Design of Consistency Protocols," with S. Petit, J. Sahuquillo and A. Pont, *Journal of Supercomputing*, Springer-Verlag, 38(1): 49-72, 2006.

27. "Reducing Data Cache Susceptibility to Soft Errors," with V. Sridharan, G. Asadi and M. Tahoori, *IEEE Transactions on Dependable and Secure Computing*, 3(4): 353-364, 2006.

28. "An Adjustable Linear Time Parallel Algorithm for Maximum Weight Bipartite Matching," with M. Fayyazi and W. Meleis, *Information Processing Letters*, Elsevier, 97(5): 185-190, 2006.

29. "Power-Aware External Bus Arbitration for System-on-Chip Embedded Systems," with K. Ning, *Transactions on High-Performance Embedded Architectures and Compilers*, Springer-Verlag, 1(1):94-113, 2006.

30. "Bus Power Estimation and Power-Efficient Bus Arbitration for System-on-a-Chip Embedded Systems," with K. Ning, *Lecture Notes in Computer Science*, Springer-Verlag, Vol. 3471, pp. 95-106, 2005.

31. "Removing Communications in Clustered Microarchitectures Through Instruction Replication," with A. Aleta, J.M. Codina and A. Gonzalez, *ACM Transactions on Architecture and Code Optimization*, 1(2): 127-151, June 2004.

32. "A Finite State Model for Respiratory Motion Analysis in Image-guided Radiation Therapy," with H. Wu, S. Jiang, G. Sharpe, and B. Salzberg, *Journal of Physics in Medicine and Biology*, 49(23): 5357-5372, 2004.

33. "Developing Object-Oriented Parallel Iterative Methods," with C. Ouarraui, *International Journal of High Performance Computing and Networking*, Vol. 1, Issue 1/2/3, 2004, pp. 85-90.

34. "Levo - A Scalable Processor With High IPC," with A. Uht, D. Morano and A. Khalafi, *Journal of Instruction Level Parallelism*, Vol. 5, August 2003, pp. 1-35.

35. "A Database System to Advance Subsurface Sensing and Imaging," with H. Wu, B. Norum and B. Salzberg, *Journal of Subsurface Sensing Technologies and Applications*, 4(4): 395-408, October 2003.

36. "Profile-Based Characterization and Tuning for Subsurface Sensing and Imaging Applications," with M. Ashouei, D. Jiang, W. Meleis, M. El-Shenawee M., E. Mizan, Y. Wang and C. Rappaport, *International Journal of Systems, Science and Technology,* September 2002, pp. 40-55.

37. "Electromagnetics Computations Using the MPI Parallel Implementation of the Steepest Descent Fast Multipole Method (SDFMM)," with M. El-Shenawee, C. Rappaport, D. Jiang and W. Meleis, *ACES Journal*, , 17(2): 112-122, July 2002.

38. "Introduction to the Special Section on High Performance Memory Systems," with H. Hadimioglu and F. Lombardi, *IEEE Transactions on Computers*, 50(11): 1103-1105, 2001.

39. "Welcome to the Opportunities of Binary Translation," with E. Altman and Y. Sheffer, *IEEE Computer*, special issue on Binary Translation, March 2000, pp. 40-46.

40. "Indirect Branch Prediction Using Data Compression Techniques," with J. Kalamatianos, *Journal of Instruction Level Parallelism*, (1), 1999, http://www.jilp.org/vol1/index.html.

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44. "Program Remapping Using Estimated Profiles," with H. Hashemi, B. Calder, J. Kalamatianos and W. Meleis, *Digital Technical Journal*, 10(2), 1999.

45. "Branch-directed and Pointer-based Data Cache Prefetching," with Y. Liu and M. Dimitri, *Journal of Systems Architecture*, Vol. 45, 1999, pp. 1047-1073.

46. "Creating 3D Circuits Using Transferred Films," with P. Sailer, P. Singhal, J. Hopwood, P.M. Zavracky, K. Warner and P.P. Vu, *IEEE Circuits and Devices Magazine*, November 1997, pp. 27-30.

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48. "Improving the Accuracy of History-Based Branch Prediction," with P. Emma, *IEEE Transactions on Computers,* 46(4): 469-472, April 1997.

49. "Modeling Cache Pollution," with J. Casmira, *International Journal of Modeling and Simulation*, 19(2): 132-138, May 1998.

50. "Real-Time Trace Generation," with O. LaMaire, W. White, P. Hennet, and W. Starke, *International Journal of Computer Simulation,* 6(1): 53-68, 1996.

51. "Issues in Trace-Driven Simulation," *Lecture Notes in Computer Science No. 729, Performance Evaluation of Computer and Communication Systems,* L. Donatiello and R. Nelson eds., Springer-Verlag, 1993, pp. 224-244.

52. "Contrasting Instruction-Fetch and Instruction-Decode Time Branch Prediction Mechanisms: Achieving Synergy Through Their Cooperation Operation," with P. Emma, J. Knight, and T. Puzak, *EuroMicro Journal*, Vol. 35, September 1992, pp. 401-408, also appearing in *Proc. of EuroMicro 92 Software and Hardware Specification and Design,* September 1992.

Textbooks, Edited Books and Book Chapters:

1. "Simulating HSA," with S. Hung, T.B. Jablin, Y. Sun, and R. Ubal, a book chapter in *Heterogeneous System Architecture: Practical Applications for Industry*, 1st edition, Elsevier Nov. 2015.

2. "Computer Organization," book chapter in *Encyclopedia of Computer Science and Technology*, with P. Mistry, Y. Ukidave, and Z. Chen, to appear, Dec. 2016.

3. "GPGPU-8: Proceedings of the 8th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and X. Gong, *ACM Online Conference Proceedings*, February 2015.

4. "Heterogeneous Computing with OpenCL 2.0," with P. Mistry, D. Schaa and D.P. Zhang, *Morgan Kaufmann Publishers*, 3rd Edition, January 2015.

5. "Special Issue on Applications for the Heterogeneous Computing Era," with J. Meng et al., *International Journal of High Performance Computing Applications*, 28(3) 2014.

6. "Fast Fourier Transform (FFT) on GPUs," with Y. Ukidave and G. Schirner, *Numerical Computations with GPUs*, Springer International Publishing, pp. 339-361, 2014.

7. "Proceedings of the 12th Annual IEEE/ACM International Symposium on Code Generation and Optimization, CGO," *ACM Digital Library*, Feburary 2014.

8. "GPGPU-7: Proceedings of the 7th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and X. Gong, *ACM Online Conference Proceedings*, March 2014.

9. "Heterogeneous Computing with OpenCL 1.2," with B. Gaster, L. Howes, P. Mistry and D. Schaa, *Morgan Kaufmann Publishers*, 2nd Edition, January 2013.

10. "GPGPU-6: Proceedings of the 6th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and X. Gong, *ACM Online Conference Proceedings*, 2013.

11. "Topic 16: GPU and Accelerators Computing," with A. Ramirez, D.S. Nikolopoulos and S. Matsuoka, *Proceedings of Europar*, 2012.

12. "Third Joint WOSP/SIPEW International Conference on Performance Engineering," with J. Rolia, L. John and D. Krishnamurthy, *ACM Digital Library*, April 2012.

13. "GPGPU-5: Proceedings of the 5th Annual Workshop on General Purpose Processing with Graphics Processing Units," with J. Cavazos and E. Sun, *ACM Online Conference Proceedings*, 2012.

14. "Heterogeneous Computing with OpenCL," with B. Gaster, L. Howes, P. Mistry and D. Schaa, *Morgan Kaufmann Publishers*, 1st Edition, August 2011.

15. "GPU Acceleration of Iterative Digital Breast Tomosynthesis," wth D. Schaa, B. Brown, B. Jang, P. Mistry, R. Dominguez, R. Moore, and D.B. Koppans, *GPU Computing Gems*, Morgan Kaufmann, 2011, pp. 647-659

16. "Proceedings of the Fourth Workshop on General Purpose Processing on Graphics Processing Units," with J. Cavazos, *ACM Online Conference Proceedings*, March, 2011.

17. "Special Issue on High Performance Computing with Accelerators," with D.A. Bader and V. Kindratenko, *IEEE Transactions on Parallel and Distributed Systems*, 22(1), 2011, pp. 3-6.

18. "Computer Organization and Design: The Hardware/Software Interace," D.A. Patterson and J.L. Hennessy, 4th edition, contributed the problem set for Chapter 7 on Multicores, Multiprocessors and Clusters.

19. "Computer Performance Evaluation and Benchmarking," D. Kaeli and K. Sachs, editors, *Lecture Notes in Computer Science*, Vol. 5419, January 2009.

20. "General Purpose Computing on Graphics Processing Units," D. Kaeli and M. Leeser, guest editors, *Journal of Parallel and Distributed Computing*, Elsevier, October 2008.

21. "High Performance Embedded Architectures and Compilers," K. DeBosschere, D. Kaeli, P. Stentrom, D. Whalley and T. Ungerer, editors, *Springer Verlag*, January 2007.

22. "Recent Speculative Architectures," with D. Morano, a book chapter in "Speculative Execution in Modern Computer Architectures," *CRC Press*, D. Kaeli and P. Yew, editors, 2005.

23. "Speculative Execution in Modern Computer Architectures," CRC Press, co-editor with P. Yew, 2004.

24. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering,* 3rd edition, edited by John Webster, *John Wiley*, 2004.

25. "High Performance Memory Systems," co-editor with H. Hadimioglu, J. Kuskin, A. Nanda and J. Torrellas, eds., *Springer Verlag*, New York, 2003, ISBN: 03870010X.

26. "Microprogramming," in *Encyclopedia of Life Sciences*, UNESCO, 2005.

27. "Computer Architecture," in *Encyclopedia of Life Sciences*, UNESCO, 2005.

28. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering,* 2nd edition, edited by John Webster, John Wiley, 2001.

29. "Parameter Value Characterization of Windows NT-based Applications," with J. Kalamatianos, *Workload Characterization: Methodology and Case Studies,* IEEE Computer Society, 1999, pp.142-149.

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31. "Digital Computer Architecture," in *The Computer Science and Engineering Handbook,* Allen Tucker, editor, CRC Press, June 2004.

32. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering,* 1st edition, edited by John Webster, John Wiley, 1999.

33. "Proceedings of FTPDS'98," with D. Avresky, edited by J. Rolim, *Lecture Notes in Computer Science*, No. 1388, Springer-Verlag, April 1998, pp. 564-789.

34. "Fault-Tolerant Parallel and Distributed Systems," co-edited with D. Avresky, *Kluwer Academic Press*, 1998.

35. "Digital Computer Architecture," a book chapter in *The Computer Science and Engineering Handbook,* edited by A.B. Tucker, CRC Handbook, 1997, pp. 412-425.

36. "The DLX Instruction Set Architecture Handbook," with P.M. Sailer, *Morgan Kaufmann Publishing*, San Francisco, CA. 1996.

37. *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications, PDPTA'96,* Volumes 1, 2 and 3, co-editor with H.R. Arabnia, B.J. d-Auriol, T. Hazra, R.A. Olsson, Y. Pan, and R. Pande, August 1996.

Conference Publications:

1. "Hardware Thread Reordering to Boost OpenCL Throughput on FPGAs," with A. Momeni, H. Tabkhi and G. Schirner, *Proc. of the International Confernce on Computer Design*, Oct 2016, to appear.

2. "Hetero-mark, A Benchmark Suite for CPU-GPU Collaborative Computing," with Y. Sun, X. Gong, A.K. Ziabari, L. Yu, S. Mukherjee, C. McCardwell and A. Villegas, Proc. of the IEEE International Sympsium on Workload Characterization, Oct. 2016, pp. 1-10.

3. "Mystic: Predictive Scheduling for GPU-based Cloud Servers Using Machine Learning," with Y. Ukidave and X. Li, *Proc. of the IEEE Parallel and Distributed Processing Symposium*, May 2016, pp. 353-362.

4. "Balancing Scalar and Vector Execution on GPU Architecture," with Z. Chen, *Proc. of the IEEE Parallel and Distributed Processing Symposium*, May 2016, pp 973-982.

5. "A Comprehensive Performance Analysis of HSA and OpenCL 2.0," with S. Mukherjee, Y. Sun, P. Blinzer and A. Kavyan Ziabari, *Proc. of the IEEE International Symposium on Performance Analysis, Software and Systems*, April 2016, pp. 183-193.

6. "Modeling Player Decisions in a Supply Chain Game," with Y. Sun, C. Liang, S. Sutherland and C. Harteveld, *IEEE Computational Intelligence and Games Conference*, Sept. 2016.

7. "Portable Performance for Monte Carlo Simulations of Photon Migration in 3D Turbid Media for Single and Multiple GPUs," with L. Yu, F. N. Paravecino and Q. Fang, *NVIDIA GPU Technology Conference*, March 2016.

8. "Performance Evaluation of Compiler-based Redundant Multithreading in an HSA Environment," with C. Kalra, D. Lowell, J. Kalamatianos and V. Sridharan, *Proc. of the 12th Workshop on Silicon Errors in Logic - System Effects*, March 2016.

9. "Evaluating the Resilience of Highly Parallel Applications," with M. Wilkening, F. Previlon and V. Sridharan, *Proc. of the 12th Workshop on Silicon Errors in Logic - System Effects*, March 2016.

10. "OpenCL-based Optimizations for Acceleration of Object Tracking on FPGAs and GPUs," with A. Momeni, H.T. Tabkhi and G. Schirner, *Proc. of the Workshop on Architectures and Systems for Real-time Mobile Vision Applications*, March 2016.

11. "A Complete Key Recovery Timing Attack on a GPU," with Z.H. Jiang and Y. Fei, *Proc. of the 22nd Internatinoal Symposium on High Performance Computer Architecture*, March 2016, pp. 395-405.

12. "CLIP: An IP-based GPU Clustering Framework," with C. McCardwell, *Proc. of the Boston Area Computer Architecture Workshop*, Jan. 2016.

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15. "Exploring the Efficiency of the OpenCL Pipe Semantic on an FPGA," with A. Momeni, H. Tabkhi, Y. Ukidave, G. Schirner and D. Kaeli, *Proc. of the International Symposium on High-Efficient Accelerators adn Reconfigurable Technologies - also appearing in SIGARCH Computer Architecture News*, June 2015, pp. 52-57.

16. "A Framework for Visualization of OpenCL Application Execution: A Tutorial," with A.K. Ziabari, R. Ubal Tena, D. Schaa and D. Kaeli, *Proceedings of the 3rd International Worksotp on OpenCL*, ACM, April 2015, pp. 1-22.

17. "The Use of Benchmarks for High-Reliablity Systems," H.Quinn, W. Robinson, P. Rech, A. Barnard, M. Aquirre, M. Desogus, L. Entrena, M. Garcia-Valderas, S.M. Guertin, F. Lima Kastensmidt, B. Kiddie, A. Sanchez-Clement, M. Sonza Reorda, L. Sterpone and M. Wirthlin, *Los Alamos National Laboratory Technical Report*, LA-UR-15-22303, March, 2015.

18. "Performance of the NVIDIA Jetson TK1 in HPC," with Y. Ukidave, U. Gupta and K. Keville, *Proc. of IEEE International Conference on Cluster Computing*, Sept., 2015, pp. 533-534.

19. "Side-channel Power Analysis on GPU AES Implementation," *Proc. of the IEEE International Conference on Computer Design*, October 2015, pp. 281-288.

20. "Securing Virtualized Execution Environments through Machine Learning-based Intrusion Detection," with F. Azmandian, J.G. Dy and J.A. Aslam, *Proc. of the IEEE International Workshop on Machine Learning for Signal Processing*, Sept. 2015, pp. 1-6.

21. "Asymmetric NoC Architectures for GPU Systems," with A.K. Ziabari, J.L. Abellan, Y. Ma and A. Joshi, *Proceedings of the 9th IEEE/ACM Symposium on Networks on Chip*, Sept. 2015, pp. 1-.

22. "Leveraging Silicon-Photonic NOC for Designing Scalable GPUs," with A.K. Ziabari, J.L. Abellan, R. Ubal, C. Chen. with A. Joshi, *Proceesings of the 29th ACM International Conference on Supercomputing*, June, 2015, pp. 273-282.

23. "Hardware Support for Local Memory Transactions on GPU Architectures," with A. Villegas, A. Navarro, R. Asenjo, and O. Plata, *Proc. of 10th SIGPLAN Workshop on Transactional Computing*, June 2015, pp. 1-9.

24. "Exploring the Features of OpenCL 2.0," with S. Mukherjee, X. Gong, L. Yu, C. McCardwell, Y. Ukidave, T. Dao, and F. Nina Paravecino, *Proceedings of the International Workshop on OpenCL (IWOCL)*, May 2015.

25. "Field, Experimental, and Analytical Data on Large-scale HPC Systems and Evaluaton of the Implications for Exascale System Design," with N. DeBardeleben, S. Blanchard and P. Rech, *IEEE 33rd VLSI Test Symposium*, April 2015, pp. 1-2.

26. "Big Data Analysis on Puerto Rico Testsite for Exploring Contamination Threats," with X. Li, L. Yu, Y. Yao, P. Wang, and R. Giese, ALLDATA, April 2015, pp. 29-34.

27. "Spatiotemporal Change of CVOC Concentrations in Karst Acquifers: Analysis of Three Decades of Data from Puerto Rico," with X. Yu, R. Ghasemizadeh, I. Padilla, C. Irizarry and A. Alshawabkeh, *Science of the Total Environment*, No. 511, 2015, pp. 1-10.

28. "Side-Channel Analysis of MAC-Keccak Hardware Implemmentations," with P. Luo, Y. Fei, A.A. Ding and M. Leeser, *Proc. of the Fourth Workshop on Hardware and Architectural Support for Security and Privacy*, June 2015, pp. 1-8.

29. "Mahout on Heterogeneous Clusters using HadoopCL," with X. Li and M. Grossman, *Proc. of the 2nd Workshop on Parallel Programming for Analytics*, February, 2015, pp. 9-16.

30. "High Performance Computing of Fiber Scattinger Simulation," with L. Yu, Y. Zhang, X. Gong, N. Roy and L. Makowski, *Proc. of GPGPU-8*, *Proc. of the 8th Workshop on General Purpose Processing with Graphics Processing Units*, February, 2015, pp. 90-98.

31. "Bridging Architecture and Programming for Throughput-Oriented Vision Processing," with A. Momeni, H. Tabkhi and G. Schirner, *FPGA 2015*, pp. 275.

32. "NUPAR: A Benchmark Suite for Modern GPU Architecture," with Y. Ukidave, F. Nina Paravecino, L. Yu, C. Kalra, A. Momemi, Z. Chen, N. Materise and B. Daley, *Proc. of the the 6th ACM International Conference of Performance Engineering*, Feb. 2015, pp. 253-264.

33. "Speech Recognition on Modern Graphics Processing Units," with L. Yu, J. Magrath, A. Pandey and M. Sears, Proceedings of the *6th Boston Area Computer Architecture Workshop*, January, 2015.

34. "Image Segmentation Using Graph Analysis on GPUs," with E. Hovaniak and F. Nina-Paravecino, Proceedings of the *6th Boston Area Computer Architecture Workshop*, January, 2015.

35. "Side Channel Attack on GPUs," with S. Mukherjee, C. Luo, C. Finnegan, and Y. Fei, Proceedings of the *6th Boston Area Computer Architecture Workshop*, January, 2015.

36. "FIR Filtering and AES Encryption with OpenCL 2.0," with C. McCardwell, T. Dao and S. Mukherjee, Proceedings of the *6th Boston Area Computer Architecture Workshop*, January, 2015.

37. "GPU-accelerated HMM for Speech Recognition," with L. Yu and Y. Ukidave, *Proc. of the 43rd International Conference on Parallel Processing Workshops*, 2014, pp. 395-402.

38. "Power Analysis Attack on Hardware Implementation of MAC-Keccak on FPGAs," with P. Luo, Y. Fei, X. Fang, A.A. Ding, and M. Leeser, *Proc. of the Conference on Reconfigurable Computing and FPGAs (ReConfig'14)*, Dec. 2014, pp. 854.

39. "Fast Simulation of X-ray Difffration Patterns from Cellulose Fibrils using GPUs," with Y. Zhang, L. Yu and L. Makowski, *IEEE Northeast Bioengineering Conference*, 2014, pp. 1-2.

40. "Calculating Architectural Vulnerability Factors for Spatial Multi-Bit Transient Faults," with M. Wilkening, V. Sridharan, S. Gurumurthi, F. Previlon and S. Li, *Prof. of the 47th IEEE/ACM International Symposium on Microarchitecture*, Cambridge, England, Dec., 2014, pp. 293-305.

41. "Scalable Open-source Side-channel Evaluation Platform for Cryptographic Devices," with N. Shah, T. Swamy, H. Dimmig and Y. Fei, *Advanced Cyber Security Center Conference*, Nov. 2014, Best poster award.

42. "Runtime Support for Adaptive Spatial Partitioning and Inter-Kernel Communication on GPUs," with Y. Ukidave, C. Kalra, P. Mistry and D. Schaa, *Proc. of the 26th IEEE International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Paris, France, 2014, pp. 168-175.

43. "System Call Anomaly Detection Using Multi-HMMs," with E. Yolacan and J.G. Dy, *Proc. of the 8th IEEE International Conference on Software Security and Reliability - Companion*, 2014, pp. 25-60.

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183. "Binary Translation," with E. Altman, *IEEE TCCA News*, October 2001, pp. 4-5

184. "Accurate Simulation and Evaluation of Code Reordering," with J. Kalamatianos, *Proceedings of the IEEE International Symposium on the Performance Analysis of Systems and Software*, Austin, TX, April 2000.

185. "Model Based Parallel Programming with Profile-Guided Application Optimization," with J. Smith, *Proceedings of the 4th Annual High Performance Embedded Computing Workshop*, MIT Lincoln Labs, Lexington, MA, September 2000, pp.85-86.

186. "Scalable Cached Disk Arrays," with M. Singh and W. Zahavi, *Proceedings of the 3rd Workshop on Computer Architecture Evaluation using Commercial Workloads*, Toulouse, France, January 2000.

187. "Using Cache Line Coloring to Perform Aggressive Procedure Inlining," with H. Aydin, *Proceedings of Interact-4*, Toulouse, France, January 2000, ACM SIGARCH News, March 2000.

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189. "Studying the Performance of the FX!32 Binary Translation System," with P.Drongowski, M. Fayyazi, D. Hunter and J. Casmira, *Proceedings of the 1st Workshop on Binary Translation*, Newport Beach, CA, Oct. 1999, also appearing in the IEEE TCCA News, December 1999, pp. 56-68.

190. "A Study of Dynamic Branch Predication for SHARC DSP's", with S. Sair and J. Fridman, *Proceedings of the 2nd International Workshop on Compiler and Architecture Support for Embedded Systems (CASES'99)*, Washington, D.C., Oct. 1999.

191. "Improving the Accuracy of Indirect Branch Prediction via Branch Classification," with J. Kalamatianos, *Proceedings of the 3rd Workshop on the Interaction Between Compilers and Computer Architecture*, October 1998, San Jose, CA, also appearing in ACM Computer Architecture News, Vol. 27, No. 1, March 1999, pp. 23-26.

192. "Predicting Indirect Branches via Data Compression," with J. Kalamatianos, *Proceedings of 31st ACM/IEEE Symposium on Microarchitecture*, Dec. 1998, Dallas, TX, pp. 272-281.

193. "Parameter Value Characterization of Windows NT-based Applications," with J. Kalamatianos and R. Chaiken, *Proceedings of the 1st Workshop on Workload Characterization*, IEEE Press, Dallas, TX, December 1998.

194. "A Study of Loop Unrolling for VLIW-based DSP Processors," with S. Sair and W. Meleis, *Proceedings of the IEEE Workshop on Signal Processing Systems: Design and Implementation*, October 1998, pp. 519-527.

195. "Performance Analysis Using NT-based Workloads," with J. Casmira and D. Hunter, *Proceedings of the 3rd Workshop on Pre-Hardware Performance Analysis Techniques*, Barcelona, Spain, June 1998.

196. "Memory Performance Tuning using Graph-based Analysis," with J. Kalamatianos, A. Khalafi, and W. Meleis, *Proceedings of the 3rd Workshop on Pre-Hardware Performance Analysis Techniques*, Barcelona, Spain, June 1998.

197. "Temporal-based Procedure Reordering for Improved Instruction Cache Performance," with J. Kalamatianos, *Proceedings of the 4th International Conference on High Performance Computer Architecture*, February 1998, pp. 244-253.

198. "Operating System Impact on Trace-Driven Simulation," with J. Casmira, J. Fraser, and W. Meleis, *Proceedings of the 31st Annual Simulation Symposium*, IEEE Computer Society, April 1998, pp. 76-82.

199. "Efficient Procedure Mapping using Cache Line Coloring," with A.H. Hashemi and B. Calder, *Proceedings of ACM SIGPLAN Conference on Programming Languages Design and Implementation*, June 1997, Las Vegas, Nevada, pp. 171-182.

200. "Analytical Models of Workload Behavior and Pipeline Performance," with M. Squillante and H. Sinha, *Proceedings of IEEE MASCOTS*, January 1997, Israel, pp. 91-96.

201. "Efficient Static Procedure Mapping using Cache Line Coloring," with A.H. Hashemi and B. Calder, *Proceedings of the 2nd Workshop on Interaction between Compilers and Computer Architectures*, February 1997, San Antonio, TX.

202. "Improving Multiprocessor Scalability Using Lockup Free Caches," *Proceedings of Parallel and Distributed Processing, with H. Sinha, Technology and Applications 1996,* Sunnyvale, CA, Aug. 1996, pp. 619-622.

203. "Using a BTB to Guide Data Cache Prefetching," with Y. Liu, *Proceedings of the 1996 IEEE International Conference on Computer Design*, Austin, Tx., Oct. 1996, pp. 225-230.

204. "Performance Modeling Using Object-Oriented Execution-Driven Simulation," with A.V. Sampogna, D. Green, M. Silva and C.J. Sniezek, *Proceedings of the 29th Annual Simulation Symposium,* New Orleans, LA, April 1996, pp. 183-192.

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206. "A Discussion on Non-Blocking/Lockup-Free Caches," with S. Belayneh, *Computer Architecture News,* Vol. 24, No. 4, September 1996.

207. "A Discussion on Non-Blocking/Lockup-Free Caches," with S. Belayneh, *Computer Architecture News,* Vol. 24, No. 3, June 1996.

208. "Efficient Procedure Mapping for Improved Instruction Cache Performance," with A.H. Hashemi, *Proceedings of the Workshop on Interaction Between Compilers and Computer Architectures,* San Jose, CA, Feb. 1996.

209. "Combining Object-Oriented Design and Computer Architecture into a Single Senior-Level Class," *Proceedings of the Workshop on Undergraduate Computer Architecture Education*, Santa Margherita, Italy, June 1995.

210. "Scalable Performance on a Distributed Shared-Memory Machine," with L. Fong, D. Renfrew, R. Booth, and K. Imming, *Proceedings of Parallel and Distributed Processing, Technology and Applications 1995,* Athens, Georgia, Nov. 1995, pp. 728-737.

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212. "Reducing Cache Pollution," with J. Casmira, *Proceedings of IASTED International Conference on Modeling and Simulation*, Pittsburgh, PA, April 1995, pp. 123-126.

213. "Branch-Directed Data-Cache Prefetching," with P.Y. Chang and Y. Liu, *Proceedings of the 4th Workshop on Scalable Shared Memory Multiprocessors,* Chicago, IL, 1994.

214. "Predicting the Number of Branches in a Finite-Length Pipeline," with M. Squillante and P. Emma, *Proceedings of the 23rd Annual Pittsburgh Modeling and Simulation Conference,* Vol. 23, Part 2, April 1992, pp. 765-772.

215. "A Study of 80X86/80X87 Floating-Point Execution," with Z. Miljanic, *Proc. of the 1991 ACM SIGSMALL/PC Symposium on Small Systems,* June 1991, pp. 34-42.

216. "Branch History Table Prediction of Moving Target Branches Due to Subroutine Returns," with P. Emma, *Proceedings of the ACM 18th Annual International Symposium on Computer Architecture,* Vol. 19, No. 3, May 1991, pp. 34-42.

217. "Issues in Trace-Driven Simulation," *Proceedings of the 22rd Annual Pittsburgh Modeling and Simulation Conference*, Vol. 22, Part 5, May 1991, pp. 2533-2540.

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U.S. Patents and Industrial Disclosures:

1. *Evaluating and Predicting Computer System Performance Using Kneepoint Analysis*, with G. Smirnov, L. Fairbanks and K. Hu, U.S. Serial No. 8,805,647, August 12, 2014.

2. *VMM-Based Intrusion Detection System,* with M. Moffie, A. Cohen, J. Aslam, M. Alshawabkeh, J. Dy and F. Azmandian, U.S. Serial No. 8,719,936, May 6, 2014.

3. *Not-taken Path Instruction for Selectively Generating a Forwarded Result from a Previous Instruction Based on Branch Outcome,* with G. Uht and D. Morano, U.S. Serial No. 8,601,245, December 3, 2013.

4. *Systems and Methods for Determining Placement of Virtual Machines,* with G. Smirnov and K. Hu, U.S. Serial No. 8,099,487, January 17, 2012.

5. *Concurrent Execution of Instruction in a Processing System,* with A. Uht and D. Morano, U.S. Serial No. 7,991,980, August 21, 2011.

6. *Resource Flow Computer,* with A. Uht and D. Morano, U.S. Patent Application 20110276792, November 10, 2011.

7. *Managing Application System Load,* with R. Corley, W. Stronge, K. Faulkner, B. Schofer and P. Beale, U.S. Patent Application 20110060827, March 10, 2011.

8. *A VMM-Based Intrusion Detection System,* with M. Moffie, A. Cohen, J. Aslam, and M. Alshawabkeh, PCT International Application No. PTC/US2009/32858, February 2009.

9. *Resource Flow Computer,* with A. Uht and D. Morano, U.S. Patent Application 20090043994, February 12, 2009.

10. *Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates,* with G. Uht and D. Morano, U.S. Serial No. 7,409,524, August 5, 2008.

11. *Methods and Systems for Identifying Application System Storage Recourses,* with W. Stronge, R. Strechay, K. Faulkner and R. Corley, U.S. Patent Application No. 20080163234, July 3, 2008.

12. *Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates,* with G. Uht and D. Morano, U.S. Serial No. 7,380,108, May 27, 2008.

13. *Method and Apparatus for Managing Application Storage Load Based on Storage Network Resources*, with R. Corley, W. Stronge, K. Faulkner, B. Schofer, P. Beale, U.S. Serial No. 60/806,699, U.S. and International patent pending, July 2007.

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15. *Automatic and Transparent Hardware Conversion of Traditional Control Flow to Predicates,* with A. Uht and D. Morano, U.S. Patent No. 7,210,025, April 2007.

16. *Resource Flow Computing Device,* with A. Uht and D. Morano, U.S. Patent No. 6,976,150, December 13, 2005.

17. *Memory Architecture Dependent Program Mapping*, with B. Calder and A. Hashemi, U.S. Patent No. 5963972, filed jointly with Digital Equipment Corporation, October 5, 1999 U.S. Patent Office.

18. *Case Block Table for Predicting the Outcome of Blocks of Conditional Branches Having A Common Operand,* with P. Emma, U.S. Patent No. 5,333,283, July 26, 1994, U.S. Patent Office.

19. *Selective Prefetching Based on Miss Latency,* with N. Perugini, IBM Technical Disclosure No. Y08921147.

20. *Tying Data Prefetching to Branch Prediction,* with N. Perugini, IBM Technical Disclosure No. Y08901085.

21. *Aliasing Reduction in the DHT,* with P. Emma, J. Knight, and T. Puzak, IBM Technical Disclosure No. Y08920597.

22. *Folding Resolution of a Case Block into a Case-Block Table,* with P. Emma, IBM Technical Disclosure No. Y08920590.

23. *Efficient Case-Block-Table Miss Handling,* with P. Emma, IBM Technical Disclosure No. Y08920598.

24. *A Tool to Validate Trace Tape Representativeness,* with J. Morris and S. Ong, IBM Technical Disclosure No. Y08900481, IBM Tech. Disc. Bulletin Vol. 34, No. 4B, Sept. 1991, pp. 345-346.

25. *Branch History Table for an Intel 80386,* with S. Ong, IBM Technical Disclosure No. Y08880663, IBM Tech. Disc. Bulletin Vol. 33, No. 4, Sept. 1990, pp. 67.

Publication Editing:

- **Associate Editor** - ACM Transaction on Architecture and Code Optimization, 2014-present.
- **Associate Editor** - Journal of Parallel and Distributed Computing, 2011 - present.
- **Associate Editor** - IEEE Transactions on Parallel and Distributed Systems, 2011 - present.
- **Associate Editor** - Journal of Instruction Level Parallelism, November 2003 - 2010.
- **Associate Editor** - IEEE Computer Architecture Letters, December 2001 - 2011.
- **Guest Editor** - Journal of Parallel and Distributed Computing, *General-Purpose Parallel Processing Using GPUs*, 2008, with M. Leeser.
- **Associate Editor** - IEEE Transactions on Computers, February 2000 - June 2004.

- **Guest Editor** - IEEE Transactions on Computers, Special Issue on High Performance Memory Systems, with F. Lombardi and H. Hadimioglu, November 2001.
- **Co-Editor** - IEEE Computer Magazine, special issue on Binary Translation, March 2000.
- **Co-Editor** - UNESCO Encyclopedia on Life Sciences, Volume on Computer Sciences, June 2000.
- **Editor** - IEEE Technical Committee on Computer Architecture Newsletter, July 1998 - March 2000.
- **Guest Editor** - IEEE Technical Committee on Computer Architecture Newsletter, Proceedings of WCAE-2, June 1996.
- **Guest Editor** - IEEE Technical Committee on Computer Architecture Newsletter, Proceedings of WCAE-1, Spring 1995.

Invited and Tutorial Talks:

1. "How can GPUs become First-class Computing Devices?," *The College of William and Mary Distinguished Lecture Series*, October 2016.
2. "Multi2sim 5.0," *Tutorial at IISWC*, September 2016.
3. "Managing Big Data in SRP Research," *NIEH 50 years of NIEHS*, July 2016.
4. "Accelerators as First-class Computing Devices," *MULTIPROG Workshop*, January 2016.
5. "Integrating Data from Multidisciplinary Research," *NIEHS Superfund Research Program e-Learning Web Seminar Serices*, November 2015.
6. "How Cyber Hacks are Changing Higher Ed," *NPR On Campus Series*, January 2015.
7. "The Road to New Heterogeneous Systems," *Drexel University*, May 2014.
8. "Preventing Cyber Threats," *Fox-25 News*, November 2014.
9. "Utilizing EQuIS to Study Exposure and its Impact on Reproductive Heath in Northern Puerto Rico," *Earthsoft Corporation*, October 2014.
10. "Protecting Reproductive Health through Environmental Big Data Analysis," *Making Sense from Big Data*, Northeastern University, October 2014.
11. "Exploring the Heterogeneous Design Space for both Performance and Reliability," *Invited Speaker at the 51st Design Automation Conference*, June 2014.
12. "The Road to New Programming Models and Architectures for Future Heterogeneous Systems," *HIPEAC Keynote*, January 2014.
13. "Secure Embedded Systems," Special Session Organizer, *IEEE HPEC*, Sept. 2013.

14. “SHPEC - Secure High Performance Extreme Computing,” *IEEE HPEC Panelist*, Sept. 2013.

15. “Heterogeneous Computing: Evolving Programming Models and Emerging Platforms,” *IEEE HPEC Invited Talk*, Sept. 2012.

16. “The Convergence of HPC and Embedded Systems in our Heterogeneous Computing Future.” *IEEE ICCD Keynote*, Oct. 2011.

17. “Biomedical Computing with GPUs,” *Analogic Corporation*, May 2011.

18. “Adventures in Desktop Supercomputing,” *Keynote at the 24th Annual CCSC:Southeastern Conference at Spelman College*, November 2010.

19. “Macroarchitecture: A Unifying Framework for Manycore Architecture Research,” *Workshop on Micro Architectural Support for Virtualization, Data Center Computing, and Clouds*, December 2010.

20. “GPU Computing - Low-cost High-performance Embedded Computing,” *Analogic Distinguished Lecture Series*, October 2010.

21. “Biomedical Research on GPUs” - panel sponsored by Dell Computer and NVIDIA, *Harvard Medical School and Dell*, October 2010.

22. “Commodity Desktop Supercomputing,” *Analogic Corporation*, August 2010.

23. “GPUs in Biomedical Imaging,” *BK Medical*, Copenhagen, Denmark, August 2010.

24. “GPU Computing,” *University Polytechnica of Catalonia - PUMPS Summer School*, June 2010.

25. “Many-core Computing: A Disruptive Technology Enabling Low-cost, Low-power Desktop Computing Organization/Sponsor,” Keynote Talk, *IEEE Systor Conference*, May 2010.

26. “Adventures in Desktop Supercomputing,” *Hewlett Packard Invited Lecture Series*, March 2010.

27. “The Road to Many-Core Computing,” *IBM T.J. Watson Research Center - Invited Lecture Series*, March 2010.

28. “Challenges in Binary Translation for Desktop Supercomputing,” *3rd Workshop on Architectural and Microarchitectural Support for Binary Translation*, February 2011.

29. “GPUs and Biomedical Computing,” *Boston University*, November 2009.

30. “Trends in GPU Computing,” *Harvard Medical School*, October 2009.

31. “GPU Computing,” *Tufts University*, October 2009.

32. “GPU Computing,” *Spelman College*, September 2009.

33. “GPU Computing,” *University of Illinois*, July 2009.

34. “Biomedical Computing with Graphics Processing Units,” *IEEE ISBI*, July 2009.

35. “Architectural Approaches to Support Software Security,” *IBM T.J. Watson Research Center*, June 2006.

36. “Architectural Approaches to Support Software Security,” *Boston University*, May 2006.

37. “Power-Aware Profiling and Benchmarking,” *Universitat Politecnica de Cataluyna*, Spain, May 2004.

38. “Profiling and Instrumentation,” *Universitat Politecnica de Cataluyna*, Spain, May 2004.

39. “Power-aware Embedded Benchmarking,” *The EEMBC Quarterly Meeting*, Boston MA, April 2004.

40. “A High IPC Multipath Microarchitecture,” *Universitat Politecnica de Valencia*, Valencia, Spain, February 2003.

41. “Realizing High IPC Through a Scalable, Multipath Microarchitecture,” *Universitat Politecnica de Cataluyna*, Barcelona, Spain, July 2002.

42. “Profile Guided Compilation,” *Tufts University, Department of Electrical and Computer Engineering*, June 2001.

43. “Profile-Guided Compilation,” *University of Massachusetts at Amherst*, Department of Electrical and Computer Engineering, March 2001.

44. “Compilation Techniques for Data Parallel Applications,” *Mercury Computer Systems*, April 2001.

45. “Profile-Guided Compilation,” InCert Corporation Lecture Series, May 2000.

46. “High-Level Language Control and Hardware-based Branch Prediction,” presented at the *University of Rhode Island Electrical Engineering Invited Lecture Series,* October 1998.

47. “Tying High-level Language Control Structure to Dynamic Branch Prediction,” presented at the *IBM Mid-Hudson Valley Server Group Technical Vitality Council Seminar*, September 1998.

48. “Operating System Rich Workload Analysis,” presented at *IBM T.J. Watson Research Center*, Yorktown Heights, N.Y., July 1998.

49. “Memory Performance Tuning using Graph-based Analysis,” presented at the *University Polytechnic of Cataluyna*, Barcelona, Spain, June 1998.

50. “Instruction and Data Cache Prefetching,” presented at *Brooklyn Polytechnic’s Technical Seminar Series*, Brooklyn, N.Y., September 1997.

51. "3-D VLSI Design Automation," presented at *Digital Equipment Corporation's ETE Technical Seminar Series*, Hudson, MA, June 1997.

52. "Procedure Mapping Using Static Call Graph Estimation," invited talk at Microsoft Research, Redmond, WA, May 19, 1997 and at Boston University's *Computer Science Colloquium*, Boston, MA, February 26, 1997.

53. "Issues in Trace-Driven Simulation," invited talk at *Intel Corporation*, Santa Clara, CA, February 1997.

54. "Issues in Trace-Driven Simulation," half-day tutorial presented at *IEEE MASCOTS*, Israel, January 1997.

55. "Issues in Trace-Driven Simulation," half-day tutorial presented at *Performance '97*, Lausanne, Switzerland, Oct. 1996.

56. "Performance Modeling Using Object-Oriented, Execution-Driven Simulation," presented at *Performance Analysis and its Impact on Design,* IBM Austin Research Laboratory, March 27, 1996.

57. "Real-Time Trace Generation," invited keynote talk at *Performance Analysis and its Impact on Design,* IBM Austin Research Laboratory, March 27, 1996.

58. "Prefetching Strategies for the Instruction and Data Stream," presented at *Digital Equipment Corporation's ETE Technical Seminar Series*, Hudson, MA, Sept. 1995.

59. "Issues in Trace-Driven Simulation," half-day tutorial presented at the *20th International Symposium on Computer Architecture,* San Diego, CA, May 1993.

60. "Trace-Driven Simulation," half-day tutorial presented at the *1993 Sigmetrics and Performance '93*, Santa Clara, CA, May 1993.

Research Funding - PI, unless stated otherwise

1. $15,000, "Northeastern University Planning Grant: I/UCRC Energy-Smart Electronic Systems," NSF I/UCRC Program, 2016.

2. $1,240,428, "Environmental Influences on Child Health Outcomes in Puerto Rico (ECHO-PRO)," NIH ECHO Program, 2016-2020, co-PI.

3. $50,000, "Heterogeneous Systems Architecture Unrestricted Gift," HSA Foundation, 2016.

4. $50,000, "Evaluation a Parallel Programming Model for Heterogeneous SoCs," Analog Devices, 2016.

5. $450,000, "STARSS: Small: Side-Channel Analysis and Resiliency Targeting Accelerators," NSF STARSS joint program with SRC, 2016-2019.

6. $500,000, "CRISP Type 1: Multi-Agent Modeling Framewrk for Mitigating Distributed Disruptions in Critical Suppy Chains," NSF CRISP, 2016-2018, co-PI

7. $359,587, “REU Site: REU Research Experiences and Mentoring in Data-Driven Discovery,” NSF REU Site Program, 2016-2019, PI.

8. $100,000, “GPU-Accelerated Monte Carlo Photon Transport Simulation Platform,” NIH/NIGMS R01-GM114365, 2015-2019, co-PI.

9. $30,000 “Analog Devices Unrestricted Gift for 2015,” Analog Devices, 2015.

10. $860,648, “BIGDATA: IA: Exploring Analysis of Environment and Health Through Multiple Alternative Clustering,” NSF-IIS, 2016-2019, co-PI.

11. $250,000 “CSR: Small: Collaborative Research: Leveraging Intra-chip/Inter-chip Silicon-Photonic Networks for Designing Next-Generation Accelerators,” NSF-CNS, 2015-2018.

12. $30,000 “Advanced Micro Device Unrestricted Gift,” AMD, 2015.

13. $1,257,461 “DMREF: Engineering Strong, Highly Conductive Nanotube Fibers Via Fusion,” NSF-DMREF, 2014-2017, co-PI.

14. $50,000 “Heterogeneous Sytems Architecture Unrestricted Gift,” HSA Foundation, 2014-201.

15. $70,000 “Advanced Micro Device Unrestricted Gift,” AMD, 2014.

16. $50,000 “Analog Devices Unrestricted Gift for 2014,” Analog Devices, 2014.

17. $450,000 “CSR:Small:Power Efficient Emerging Heterogeneous Platforms,” NSF-CNS, 2013-2016, co-PI.

18. $500,00 “MRI: Development of a Testbed for Side Channel Analysis and Security Evaluation (TeSCASE),” NSF-MRI, 2013-2016, co-PI.

19. $16,607 “Full System Taint,” MIT Lincoln Labs, 2013.

20. $30,000 “Analog Devices Unrestricted Gift for 2013,” Analog Devices, 2013.

21. $25,000 “Samsung Southern Islands Simulator,” 2013.

22. $55,000 “AMD GPU Research Gift,” 2013.

23. $18,000 “Reducing Uncertainties in SBRT for Pancreatic Cancer,” Massachusetts General Hospital, 2013, subcontract.

24. $20,016 “Reducing Uncertainties in SBRT for Pancreatic Cancer,” Massachusetts General Hospital, 2012, subconstract.

25. $40,000 “A System Model for Effective Anomaly Analysis and Detection,” NU-Technion Collaboration, 2012.

26. $4,500,000 “NSF Scholarship for Service Program,” 2012-2017, co-PI.

27. $4,540,000 “C3DDB Phase II Application,” MA Life Science, 2012, co-PI.

28. $95,000 “Multiscale Computation of Nanomaterials,” MGHPCC, 2012, co-PI.

29. $31,126 “Portable Dynamic Taint Analysis with QEMU”, MIT Lincoln Labs, 2012-2013.

30. $45,495 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor”, MIT Lincoln Labs, 2012-2013.

31. $25,000 “Qualcomm Unrestricted Gift,” 2012.

32. $25,000 “Analog Devices Unrestricted Gift for 2012 Student Support,” Analogic Devices, 2012.

33. $90,000 “Analogic Research Gift,” 2012.

34. $30,517 “Analogic GPU Research Project,” 2012.

35. $65,000 “AMD GPU Research Gift,” 2012.

36. $8,000 “AMD Reliability Research,” 2012.

37. $48,121 “Portable Dynamic Taint Analysis with QEMU,” MIT Lincoln Labs, 2011.

38. $48,121 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor,” MIT Lincoln Labs, 2011.

39. $90,000 “Analogic Research Gift,” 2011.

40. $30,517 “Analogic GPU Research Project,” 2011.

41. $30,000 “Ultrasound Image Reconstruction Acceleration,” Analogic Corp., 2011.

42. $56,000 “AMD GPU Research Gift,” 2011.

43. $25,000 “Analog Devices Unrestricted Gift for 2011 Student Support,” Analogic Devices, 2011.

44. $349,999 “ SHF:Small:The Cross-layer Reliability Stack,” NSF CCF, 2009-2013.

45. $824,248 “Puerto Rico Testsite For Exploring Contamination Threats,” NIEHS, 2010-2013, co-PI.

46. $90,000 “Analogic CenSSIS Corporate Membership to fund GPU Research,” Analogic Corp., 2010.

47. $30,000 “Analog Devices Unrestricted Gift for 2010 Student Support,” Analogic Devices, 2010.

48. $199,947 “In-situ Calibration of Stereo Camera and Acoustic Bathymetric Sensors,” NSF ERC SECO, 2010, co-PI.

49. $80,000 “PRoTECT Partial Equipment Supplement,” NIH, 2010.

50. $38,371 “Analogic-BK Phase I Grant,” Analogic Corp., 2010.

51. $30,744 “Analogic-BK Phase II Grant,” Analogic Corp., 2010.

52. $48,121 “A Disk-subsystem Interposer Using a Lightweight Virtual Machine Monitor,” MIT Lincoln Labs, 2011.

53. $26,000 “AMD GPU Research Gift - Part 1,” 2010.

54. $26,617 “AMD GPU Research Gift - Part 2,” 2010.

55. $12,500 “AMD GPU Research Gift - Part 3,” 2010.

56. $44,567 “Open Computational Infrastructure for Surgical Skill Development and Assessment,” NIST, 2010, subcontract.

57. $44,502 “A Disk-subsytem Interposer Using a Lightweight Virtual Machine Monitor,” MIT Lincoln Labs, 2010.

58. $36,000 “Analogic-BK Ultrasound Acceleration”, Analogic Corp., May 2010.

59. $56,000, “AMD Biomedical Computing,” AMD Corp, Feb. 2010.

60. $248,400, “REU Site: BIOSENSE,” NSF EEC-HRD, Apr. 2010-2013, co-PI.

61. $20,000, “Careers in High Performance Systems Mentoring Workshop,” NSF CCF, 7, 2009, co-PI.

62. $28,100 “Analog Devices Unrestricted Gift for 2009 Student Support,” Analogic Devices, 2009.

63. $1,300,000, “Biomedical Imaging Acceleration Toolbox,” NSF-ERC Innovation Program, Dec. 2009-2013.

64. $1,935,701, “Multi-disciplinary Preparation of Next Generation Information Assurance Practitioners,” NSF DUE, Nov. 2008-2013.

65. $50,000, “Binary Translation and Optimization on Larrabee,”, Intel Corporation, November 2008.

66. $67,631, “CRI:CRD Collaborative Research: Archer - Seeding a Community-based Computing Intrastructure for Computer Architecture Research and Education,” NSF-CRI Program, April 15, 2008, co-PI.

67. $61,146, “Benchmarking Virtual Machine Performance,” Network Engines, May 2008.

68. $25,000, “A Binary Translation Layer for ATI Stream Computing,” AMD, May 2008.

69. $46,007,“Draper Research Fellowship,” Draper Labs, Cambridge MA., July 2007.

70. $6,656,“Akorri Funding,” Akorri Funding, May 2007.

71. $57,899,“Modeling and Performance Analysis of Multiple Virtual Machines working in Context,” Network Engines, March 2007.

72. $150,000,“Commercial Grade Automatic and Manual Parallelization and Performance Tools,” NSF STTR, January 2007, subcontract.

73. $199,999,“MRI/Acq: Enabling Research on Terabyte-Scale Datasets,” National Science Foundation, May 2006, co-PI.

74. $113,352,“Soft-Error Modeling,” EMC, Hopkington, MA., April 2006, co-PI.

75. $40,973,“Draper Research Fellowship,” Draper Labs, Cambridge MA., July 2006.

76. $55,000,“BlackFin Research,” Analog Devices, Norwood, MA., April 2006.

77. $23,000,“BlackFin Research,” Analog Devices, Norwood, MA., September 2005.

78. $10,000, “Parallelization of Segmentation Codes,” Massachusetts General Hospital, September 2005, co-PI.

79. $50,000,“BlackFin Research,” (PI) Analog Devices, Norwood, MA., October 2004.

80. $500,“Undergraduate Research,” (PI) NU Provosts Office, Northeastern University, October 2004.

81. $12,107,“Developing Power-Aware Compilation Strategies For the Blackfin Platform,” Analog Devices, Norwood, MA., July 2004.

82. $300,000 “Collaborative Research: Tuning Libraries to Effectively Exploit the Memory Hierarchy,” National Science Foundation, Advanced Computational Research Program, January 2004, PI.

83. $1,000 “Boston Area Computer Architecture Research Workshop,” (PI), Intel Corporation, Santa Clara, CA, January 2004.

84. $22,400 “NSF REU Grant,” December 2003.

85. $30,673, “Partitioning of Multimedia Applications on a Multi-core Blackfin Platform,” Analog Devices, Norwood, MA., October 2003.

86. $23,546 “Developing Power-Aware Compilation Strategies For the Blackfin Platform,” Analog Devices, Norwood, MA., October 2003.

87. $241,043 “Architectural Features for Virus Detection and Recovery,” National Science Foundation, Computer Systems Architecture Program, Aug. 2003.

88. $681,674 “Institute of Complex Software Science, ICSS, 5 years, 2002, co-PI.

89. $19,463 “Software-Defined Radio,” Mercury Computer Systems, January 2002.

90. $25,000 “Foreign Visitors Program,” Spanish Ministry of Education and Sports, September 2001.

91. $9,734 “Research at UPC Barcelona, Spain,” NSF Supplemental Award - NSF International Program, July 2001.

92. $74,961 “Profile-Guided Optimization and Parallelization Targeting Mercury Dataflow Architectures,” Mercury Computer, December 2000.

93. $500,000 “Mercury RACE-system Grant,” Mercury Computer, December 2000.

94. $45,243 “FRIO Processor Performance,” Analog Devices, May 2000.

95. $10,000 “NSF REU Grant,” September 2000, co-PI.

96. $43,000 “Compaq Corporation Funding,” October 2000.

97. $16,500,000(estimated) “An Engineering Research Center for Subsurface Sensing and Imaging System,” NSF NSF ERC Program, September 2000, senior investigator, though thrust lead. .

98. $143,000 “A Memory Intensive Compilation Environment Targeting VLIW and DSP Architectures, NSF MRI Program, September 2000, co-PI.

99. $21,000 “IBM Partnership Award,” IBM Corporation, August 1999.

100. $255,427 “Interprocedural Value-Based Program Optimization,” National Science Foundation, July 1999, co-PI.

101. $5,000 “Undergraduate Research Fellowship,” Sun Microsystems, June 2000.

102. $32,000 “Compaq Research Grant,” Compaq Corporation, May 1999.

103. $25,778 “Shared University Research Grant,” IBM Corporation, September 1998.

104. $329,794 “A High-Performance, Low-Cost Testbed for Network-based Research,” NSF Major Research Instrumentation Program, August 1998, co-PI.

105. $30,000 “Data/Knowledge Bases for Image Generation,” Northeastern Pre-ERC Funding, Northeastern University, June 1998.

106. $35,000 “Prototype Low-cost Parallel/Distributed Testbed,” Northeastern Pre-ERC Funding, Northeastern University, June 1998.

107. $30,000 “ IBM Partnership Award,” IBM Corporation, August 1998.

108. $22,000 “EMC/NUCAR Joint Research Program,” EMC Corporation, December 1997.

109. $84,198 “Development of a DSP Compilation Testbed,” NCRI: 97-29856, National Science Foundation, 1997-1998.

110. $35,000 “Compiler Research,” Microsoft Research, August 1997.

111. $12,000 “Design in the 3rd Dimension,” Design Automation Conference, June 1997.

112. $59,000 “Research on Plasma Etching of Vias for 3-D Microelectronics,” Office of Naval Research, April 1996, co-PI.

113. $79,946 “Three-Dimensional Electronics Using Transferred SOI Films,” Kopin Corporation, 1994, co-PI.

114. $200,000 “Three-Dimensional Electronics Using Transferred SOI Films,” Kopin Corporation, 1994-1997, co-PI.

115. $131,995 “CAREER Program: Research and Education Plan,” NSF CAREER Program, Grant Number 95-01172, 1995-1998.

116. $25,000 “Open Systems I/O Characterization,” EMC Corporation, June 1996.

117. $21,708 “Autobahn Research,” Data General Corporation, July 1996.

118. $21,000 “Tools and Techniques for Open System I/O Tracing,” , EMC Corporation, Oct. 1996.

119. $5,000 “Studying the Characteristics of I/O Database Mining,” , Northeastern University College of Engineering, 1996.

Equipment/Software Donations

1. $5,000 “ AMD APU Hardware,” AMD, 2014.

2. $5,000 “ Altera FPGA Boards,” Altera, 2013.

3. $80,000 “ EQiUS Software License,” Earthsoft, 2012-2014.

4. $20,000 “ APU Cluster,” AMD, 2012.

5. $2,000, “Snapdragon Tablets,” Qualcomm, 2012.

6. $10,000, “Developing a GPU Teaching and Research Testbed,” NVIDIA, January 2008.

7. $14,000, “VI3 ESX Server Licenses,” VMWare, November 2007.

8. $38,585, “BlackFin BF561s with FPGAs,” Analog Devices, January 2006.

9. $1,500 “EEMBC Benchmark Consortium Membership,” EEMBC, June 2004.

10. $3,400 “Power Measurement Equipment,” Analog Devices, May 2004.

11. $8,000 “BlackFin BF533 Easykits,” Analog Devices, August 2003.

12. $5,200 “RTExpress Licenses,” Integrated Sensors Incorporated, May 2001.

13. $5,319,050 “Synopsys Software Licenses Renewal,” Synopsys Corp., January 2000.

14. $15,683 “Alpha Miata Machines,” Compaq Corporation, May 1999.

15. $20,000 “EDG Compilation Toolset,” Edison Design Group, April 1997-2000.
16. $15,610 “Microsoft Software Licenses,” Microsoft Corporation, August 1997.
17. $10,740 “Alpha PC-164 Gift,” Digital Equipment Corporation, April 1997.
18. $300,000 “EMC Centriplex Donation,” EMC Corporation, December 1996.
19. $6,000 “SCSI-bus Analyzer,” EMC Corporation, June 1996.
20. $6,144,013 “Synopsys University Program,” April 1996.
21. $77,688 “Hewlett Packard Equipment Grant,” January 1995.

Panels, Program Chairs and Committees

- **General Chair** - IEEE CGO 2014, Orlando, FL.
- **Committee Member** - IEEE Computer Society Fellows Selection Committee, 2010, 2011, 2012, 2014.
- **Panel Member** - Natural Sciences and Engineering Research Council Strategic Project Grants Program, 2010, 2011, 2012, 2013.
- **Panel Member** - Austrian Science Fund Program, 2009.
- **Distinguished Reviewer** - HIPEAC, 2014.
- **Panel Member** - NSF CAREER Awards, November 1998, October 2003, October 2005, October 2006, October 2007.
- **Panel Member** - NSF CyberTrust PI Meeting, August 2004.
- **Panel Member** - NSF ITR Panel, May 2004.
- **Panel Member** - NSF Next Generation Software Program, 2001.
- **Panel Moderator** - IEEE ICCD, 2011.
- **General Co-Chair** - ACM ICPE, 2012, Boston, MA.
- **General Chair** - ACM/IEEE ISCA, 2006, Boston, MA.
- **General Co-Chair** - ACM/IEEE PACT, 2003, New Orleans, LA.
- **General Co-chair** - IEEE HPCA-8, 2002, Cambridge, MA.
- **General Co-chair** - High Performance Embedded Architectures and Compilers, 2007.
- **Program Chair** - IEEE CGO 2010.
- **Program Chair** - SPEC 2009 Workshop.

- **Program Chair** - IEEE International Symposium on Workload Characterization, 2005.
- **Program Vice-Chair** - IEEE Frontiers, 2007.
- **Program Vice-Chair** - IEEE International Symposium on Parallel and Distributed Systems (IPDPS), 2008, 2013.
- **Program Vice-Chair** - IEEE International Conference on Parallel and Distributed Systems (ICPADS), 2006.
- **Benchmark Chair** - IEEE Symposium on Workload Characterization, 2006.
- **Program Committee** - InfoComp, 2014
- **Program Committee** - SELSE, 2014
- **Program Committee** - ICPE, 2014
- **Program Committee** - Digital Systems Design, 2014
- **Program Committee** - HotPAR, 2013
- **Program Committee** - EduPar, 2013, 2014
- **Program Committee** - CLOSER, 2013, 2014
- **Program Committee** - NPC, 2013, 2014
- **Program Committee** - FutureTech 2012
- **Program Committee** - 2012 CC-Grid Conference
- **Program Committee** - Euromicro Digital System Design Conference 2012
- **Program Committee** - International Workshop on Frontiers of GPU Computing, 2012
- **Program Committee** - IEEE International Conference on Supercomputing 2012
- **Program Committee** - 2012 On-chip Memory Hierarchy and Interconnects
- **Program Committee Member** - ACM/IEEE ISCA, 2008, 2011, 2012.
- **Program Committee Member** - ACM/IEEE MICRO, 2001, 2003, 2004, 2005, 2008, 2011.
- **Program Committee Member** - ICCD, 2010, 2011, 2012.
- **Program Committee Member** - FGC , 2010, 2011.
- **Program Committee Member** - AINA , 2011.
- **Program Committee Member** - AMAS-BT , 2010, 2011, 2012, 2013.
- **Program Committee Member** - NaBIC , 2011.

- **Program Committee Member** - NPC , 2011.
- **Program Committee Member** - SAAHPC , 2009, 2010, 2011, 2012.
- **Program Committee Member** - VALID, 2011, 2012.
- **Program Committee Member** - WACY, 2011.
- **Program Committee Member** - GPGPU, 2008, 2009, 2010, 2011, 2012, 2013, 2014.
- **Program Committee Member** - ACM International Conference on Scientific and Statistical Database Management, 2004.
- **Program Committee Member** - IEEE HPCA, 1999, 2002, 2004, 2007, 2008, 2011.
- **Program Committee Member** - MEDEA Workshop, 2000, 2003, 2004, 2006.
- **Program Committee Member** - MTEAC Workshop, 2000-2002, 2007.
- **Program Committee Member** - WMPI Workshop, 2004, 2005.
- **Program Committee Member** - ICPP-HPSEC04, 2004.
- **Program Committee Member** - IEEE ISPASS, 2002-2006.
- **Program Committee Member** - IEEE Frontiers, 2004, 2007, 2008.
- **Program Committee Member** - IEEE PACT, 2000.
- **Program Committee Member** - SBAC-PAD, 2004, 2005, 2006, 2007.
- **Program Committee Member** - CGO 2008.
- **Program Committee Member** - ICPP, 2002.
- **Program Committee Member** - IPDPS, 2004.
- **Program Committee Member** - Workshop on Storage Networks Architecture and Parallel IO, 2003, 2004.
- **Program Committee Member** - Conference on Communication Networks and Distributed Modeling and Simulation, SCS, 2002.
- **Program Committee Member** - IEEE Workshop on Workload Characterization, 2000-2004.
- **Program Committee Member** - Annual Simulation Symposium, 2000-2006.
- **Program Committee Member** - Interaction between Compilers and Computer Architectures, 2000-2001.
- **Program Committee, Technical Committee** - SHARC, Boston, MA, September 2000.

- **Program Committee Member** - Workshop on Embedded Fault-Tolerant Systems, Dallas, TX, 1996.
- **Program Committee Member** - International Conference on Parallel and Distributed Processing Techniques and Applications, Sunnyvale, CA., 1996.
- **Registration Chair** - ACM ASPLOS, 2004.
- **Tutorial Chair** - IEEE HPCA-10, 2003.
- **Panel Member** - Canada Foundation for Innovation, Ottawa, Ontario, February 2002.
- **Organizer** - Workshop on Architecture and System Support for Improving Software Dependability, 2006.
- **Organizer** - Workshop on Architectural Support for Security and Anti-virus, 2004.
- **Co-Organizer** - Workshop on Memory Performance Issues, May 2002, Alaska.
- **Co-Organizer** - Workshop on Memory Performance Issues, July 2001, Goteborg, Sweden.
- **Program Committee Member** - International Symposium on Performance Analysis of Software and Systems, 2001.
- **Co-Organizer** - Workshop on Binary Instrumentation and Applications, 2005, 2006.
- **Co-Organizer** - 3rd Workshop on Binary Translation, September 2001.
- **Local Arrangements Chair** - ACM Sigmetrics, Cambridge, MA, June 2001.
- **Local Arrangements Chair** - ACM ASPLOS, Cambridge, MA November 2001.
- **Local Arrangements Chair** - 9th ACM Conference on Architectural Support for Programming Languages and Operating Systems, November 2000.
- **Co-Organizer** - 1st Workshop on Solving the Memory Wall, June 2000.
- **Co-Organizer** - 2nd Workshop on Binary Translation, Philadelphia, PA, 2000.
- **Co-Organizer** - 1st Workshop on PC-based System Performance Analysis, Santa Clara, CA, October, 1998.
- **Organizer** - 4th International Workshop on Computer Architecture Education, Las Vegas, NV, February 1998.
- **Co-Organizer** - Workshop on Computer Architecture Education, Barcelona, Spain, June 1998.
- **Tutorial and Workshop Chair** - 8th ACM Conference on Architectural Support for Programming Languages and Operating Systems, San Jose, CA, October 1998.

- **Co-organizer** - 3rd Annual Workshop on Fault-Tolerant Parallel and Distributed Systems, in conjunction with the 12th International Parallel Processing Symposium, Orlando, FL, April 1998.
- **Co-Organizer** - 2nd Annual Workshop on Fault-Tolerant Parallel and Distributed Systems, in conjunction with the 11th International Parallel Processing Symposium, Geneva, Switzerland, April 1997.
- **Organizer** - 3rd International Workshop on Computer Architecture Education, San Antonio, TX, February 1997.
- **Tutorial and Workshop Chair** - 3rd International Conference on High Performance Computer Architecture, San Antonio, Texas, February 1997.
- **Co-Organizer** - Workshop on Fault-Tolerant Parallel and Distributed Systems, in conjunction with the 10th International Parallel Processing Symposium, Honolulu, HA, April 1996.
- **Organizer** - 2nd International Workshop on Computer Architecture Education, San Jose, CA, February 1996.
- **Organizer** - Workshop on Undergraduate Computer Architecture Education, Santa Margherita, Italy, June 1995.
- **Workshop Chair** - IEEE/ACM PACT, 2004.
- **Organizer** - 1st International Workshop on Computer Architecture Education, Raleigh, N.C., January 1995.

Professional Activities:

- **Chair** - IEEE Technical Commmittee on Computer Architecture, 2009-present.
- **Chair** - IEEE Technical Commmittee on Microarchitecture and Microprogramming, 2007-2010.
- **Vice-Chair** - IEEE Technical Commmittee on Computer Architecture, 2006-2009.
- **Member** - NSF TeraGrid Scientific Advisory Board, 2007-2010.
- **Member** - CRA Computing Community Consortium, 2007-2010.
- **Member-at-Large** - ACM SIGMICRO - 2006-2013.
- **Executive Committee** - IEEE Technical Committee on Computer Architecture, 2000-2006.
- **Chair** - IEEE Technical Committee on Microprogramming and Microprocessors, 2007-2009.
- **Treasurer** - ACM SIGMICRO - 2006-2008.
- **Director** - ACM SIGMICRO Awards Program, November 2001-2005.

- **Chair** - Sigmetrics Corporate Sponsor Program - 1994-95.

Other Honors:

- **IEEE Fellow** - 2010.
- **ACM Distinguished Scientist** - 2014.
- **COE Distinguished Professor** - 2014.
- **HSA Distinguished Professor** - 2014-present.
- **NVIDIA Research Center** co-director - 2011-2016.
- **AMD Academic Research Partner** - 2010-present.
- **Award of Recognition** - Northeastern University, presented by SWE, SHPE, BESS and SASE, 2014.
- **Research Award** - Northeastern RISE, 2012.
- **Outstanding Service Award** - SPEC, 2009.
- **Outstanding Researcher Award** - Northeastern University College of Engineering, 2009.
- **Mentorship Award** - Northeastern University College of Engineering, 2007.
- **Distinguished Researcher Award Program** - Northeastern University Provost's Office, 2004, 2005, 2006.
- **Eta Kappa Nu Engineering Honor Society**
- **Sigma Xi Honor Society**
- **Who's Who in Teaching in America, 1996**

Consulting and Textbook Reviews:

- **Expert Witness, Oblon, Spivak, McClelland, Maier and Neustadt, LLP, 2014.**
- **Chief Science Advisor of Apposable Software, Medway, MA, 2011-present**
- **CTO of NUIC Technologies, Medway, MA, 2007-2011**
- **Consultant for Akorri Networks, Littleton, MA, 2005-2011**
- **Consultant for InCert Corporation, Cambridge, MA, 2000**
- **Motorola Paging Systems, Boynton Beach, FL, 1997-98**
  Course developer for the Motorola Architecture Leadership Program
- **Intel Corporation, Santa Clara, CA, 1997**
  Expert witness in the Intel-DEC patent lawsuit case

- **Dynamics Research Corporation, West Newton, MA 1994**
  Education on Object-oriented Design and C++ Programming
- **Modular Computing Technology, Concord, MA 1993**
  Performance modeling and simulation of client-server platforms
- **Various publishers including: Morgan Kaufmann, CRC, Elsevier, Weste, McGraw Hill**
  Reviewing textbooks and proposals for texts

Graduate Students:

Defended Ph.D. Theses

1. Dr. Amir Hooshang Hashemi, *Efficient Procedure Mapping for Improved Cache Performance*, PhD, May 1996.
2. Dr. John Kalamatianos, *Microarchitectural and Compile Time Optimizations for Performance Improvement of Procedural and Object Oriented Languages*, PhD, January 2000.
3. Dr. Alireza Khalafi, *Exploring Multipath Execution on a Distributed Microarchitecture*, PhD, June 2003.
4. Dr. Jennifer Black, *Multi-criteria Data Flow Testing*, PhD, August 2003.
5. Dr. Marcos de Alba, *Exposing Instruction Level Parallelism in the Presence of Loops*, PhD, December 2003.
6. Dr. Morteza Fayyazi, *Fault-Tolerant and Efficient Cluster Switch Architecture*, PhD, April 2005.
7. Dr. Huanmei Wu, *Time-based Indexing of Multidimensional Databases*, PhD, May 2005.
8. Dr. David Morano, *Exploring Instruction Level Parallelism Using Resource Flow Execution*, PhD, April 2006.
9. Dr. Yijian Wang, *Modeling and Acceleration of File-IO Dominated Parallel Workloads*, PhD, December 2006.
10. Dr. Ke Ning, *System-Level Memory Power and Performance Optimization for System-on-a-Chip Embedded Systems*, PhD, May 2007.
11. Dr. Micha Moffie, *Investigating the Utility of Software Semantics for Host-based Intrusion Detection Systems*, PhD, August 2008.
12. Dr. Vilas Sridharan, *The System Vulnerability Stack: Abstraction for Vulnerability Assessment*, PhD, May 2010.
13. Dr. Byunghyun Jang, *Evaluation and Enhancement of Memory Efficiency Targeting General-Purpose Computations on Scalable Data-Parallel GPU Architectures*, PhD, December 2010.

14. Dr. Demetris Galatopolullous, *p2pSOA: A Middleware Architecture to Enable Group Collaboration*, PhD, December 2011.

15. Dr. Emmanuel Arzuaga, *Using Live Virtual Machine Migration to Improve Resource Efficiency in Virtualized Data Centers*, PhD, December 2011.

16. Dr. Fatemeh Azmandian, *Virtual Machine Monitor Characterization using Machine Learning*, PhD, August 2012.

17. Dr. Malak Alshawabkeh, *Hypothesis Margin Based Weighting for Feature Selection Using Boosting: Theory, Algorithms and Applications*, PhD, April 2013.

18. Dr. Rodrigo Dominguez, *Dynamic Translation of Runtime Environments for Heterogeneous Computing*, PhD, April 2013.

19. Dr. Jennifer Mankin, *Classification of Malware Persistence Mechanisms using Low-Artifact Disk Instrumentation*, PhD, September 2013.

20. Dr. Ayse Yilmazer, *Micro-architectural Support for Improving Synchronization and Efficiency of SIMD Execution on GPUs*, PhD, December 2013.

21. Dr. Dana Schaa, *Improving the Cooperative Capability of Heterogeneous Processors*, PhD, April 2014.

22. Dr. Perhaad Mistry, *Architectural Support for Irregular Programs and Performance Monitoring for Heterogeneous Systems*, PhD, April 2014.

23. Dr. Esra Yolacan, *Learning from Sequential Data for Anomaly Detection*, PhD, October 2014.

24. Dr. Yash Ukidave, *Architectural and Runtime Enhancements for Dynamically Controlled Multi-Level Concurrency on GPUs*, PhD, December 2015.

25. Dr. Thomas McCormick, *Ultra-Reliable Flash Memory Systems for Embedded Applications*, PhD, April 2016.

26. Dr. Enqiang Sun, *Cross-Platform Heterogeneous Runtime Environment*, PhD, April 2016.

Defended MS Theses

1. Angela Sampogna, *Architectural Implications of C and C++ Programming Models*, MSEE 1995

2. Yue Liu, *Analysis of Branch Directed Data Cache Prefetching*, MSEE 1995

3. Samson Belayneh, *The Effect of Balanced Instruction Scheduling on the Performance of Non-Blocking Caches*, MSEE 1996

4. Himanshu Sinha, *Non-blocking Caches in Shared Memory Multiprocessors*, MSEE 1996

5. John Fraser, *Cache Analysis in a Multiprocess Environment Using Execution Driven Simulation*, MSEE 1996

6. Mona Dimitri, *Cache Pointer-Based Prefetching for Complex Data Structures*, MSCSE 1997

7. Svetlana Sokolova, *Static Branch Prediction Using High-Level Control Structure*, MSEE 1997

8. Tracy Tao, *Branch Prediction With Branch History Chain Table for Wide-Issue Superscalar Processors*, MSEE 1998

9. Jason Casmira, *Operating System Rich Workload Characterization*, MSEE 1998

10. Mekalu Teshome, *I/O Cache Structures and System Performance*, MSEE 1998

11. Kyle Bowers, *Characterization of the Java Virtual Machine*, MSEE 1999.

12. Hua Huang, *A Buffering Scheme for Improved BSD Fast File System Performance*, MSEE 1999.

13. Ying Liu, *A Channel Routing Algorithm for 3-D VLSI*, MSEE 1999.

14. Manpreet Singh, *Scalable Interconnects and Topologies for High Performance ICDSs*, MSEE 1999.

15. Philip Sailer, *YIFAN is a Pure RISC in a Three-Dimensional Integrated Circuit*, MSEE 2000.

16. Hakan Aydin, *Exploring the Effects of Cache Line Coloring and Procedure Inlining*, MSEE 2000.

17. Efe Yardimci, *Profile-guided Heap Layout*, MSEE, 2001.

18. Songqing Zhang, *BDSPTune: Binary-level Instrumentation of the SHARC DSP*, MSEE, 2001.

19. Murat Bicer, *A Software Communications Architecture Compliant Software Defined Radio Implementation*, MSEE 2002.

20. Deniz Balkan, *Side-Effects of Value Speculation on Branch Resolution and Performance in Out-of-Order Superscalar Microprocessors*, MSEE 2003.

21. Stephen VanderSanden, *Developing Power-Aware Strategies for Embedded DSPs*, MSEE 2004.

22. Anita Thomas, *Value Prediction with Perceptrons*, MSEE 2004.

23. Darren Ng, *Aspect Oriented Garbage Collection*, MSEE 2005.

24. Kaushal Sanghai, *A Code Layout Framework for Embedded Processors with a Configurable Memory Hierarchy*, MSEE 2005.

25. Vilas Sridharan, *Soft Errors in Cache Memories*, MSEE 2006.

26. Diego Rivera, *Accelerating Sparse Matrix Computations*, MSCSE 2007.

27. Brian Mullins, *Soft Errors in Storage Systems*, MSECE 2007.

28. Michael Benjamin, *A Study of Video Processing using Stream Computing on Blackfin Processors*, MSECE 2007.

29. Fatemeh Azmandian, *The Chart Checker: Applying Data Mining Techniques to Detect Major Errors in Radiotheraphy Treatment Charts*, MSECE 2008.

30. Seth Molloy, *Energy Conservation Techniques for the Blackfin Processor*, MSEE, 2008.

31. Burak Erem, *Interactive Deformable Registration Visualization and Analysis of 4D Computed Tomography*, MSEE 2008.

32. Derek Uluski, *Real Time Anti-virus for a Virtualized Environment*, MSECE 2008.

33. Wassim Bassalle, *Optimization of Cryptographic Algorithms on an Embedded Architecture*, MSECE 2008.

34. Zhaoqian Chen, *Performance Evaluation and Characterization of Virtual Appliances*, MSECE 2008.

35. Dana Schaa, *Multi-GPU Performance Modeling*, MSECE 2009.

36. Jenny Mankin *Embedded System Transactional Memory*, MSECE 2009.

37. Yungho Yang *Memory Forensics on Embedded Linux*, MS Project 2009.

38. Sarmad George *Multi-core Reliability*, MS Project 2009.

39. Tong Pan *Mapping Decision Tree Algorithms to GPUs*, MSECE 2010.

40. Roberto Cabral *Upgrading a Fieldable Air Traffic Control Interrogator*, MSECE 2010.

41. Joshua Hodosh *Memory System Introspection*. MSECE 2010.

42. Kin Kone Kito *Power profiling on Embedded Processors*, MSECE 2010.

43. Kevin McKinley *GPU Acceleration in a Gordon Challenge Project*, MS Project 2010.

44. Kulin Seth *Heterogeneous System Modeling*, MSECE 2011.

45. Stephen Maresh *Using HAsim to Model a Re-Order Buffer*, MS Project 2011.

46. Matthew Sellitto *Exploring GPU Computing for Hyperspectral Image Analysis*, MSECE 2011.

47. Cristy Casella *Wireless Management of Unattended Ground Sensors*, MS Gordon Leadership, 2011.

48. Jie Tang *An X86 Application on Android*, MS Project, 2011.

49. Allen Lee *Transparent and Dynamic Software Updates for Security*, MS Project, 2012.

50. Raghu Varier *MADNESS - Multi-Resolution Adaptive Numerical Environment for Scientific Simulation*, MS Project, 2012.

51. Yash Ukidave *Investigating Power-Efficiency of Optimization Techniques Applied to Heterogeneous Applications*, MS Thesis 2012.

52. Ryan Whelan *Architecture-Independent Dynamic Information Flow Tracking*, MS Thesis, 2012.

53. Sam Coe, *Full System Taint Analysis*, MS Project, 2014.

54. Yuqing Shi, *A Software Model for Control-Flow Instructions on an NVIDIA Kepler GPU*, MS Project, 2014.

55. Xiangyu Li, *Accelerating Mahout on Heterogeneous Clusters Using HadoopCL*, MS Thesis, 2014.

56. Adrienne Horne, *Power Congestion Analysis Constraint Impact Tool*, MS Gordon Leadership, 2015.

University/College/Department Service and Leadership

- University Faculty Senate Academic Policy Committee (Chair) - 2016-2017.
- University Faculty Senate Academic Policy Committee - 2015-2016.
- Associate Dean for Undergraduate Programs - 2010-2013.
- ECE Faculty Search Committee - 2010-2013, (Chair) 2013-2016.
- Goldwater Scholarship Award Committee - 2009-present.
- University Undergraduate Research Committee - 2014.
- University International Student Success Task Force (Chair) - 2011-2013.
- University Research Computing Advisory Committee - 2015-2017.
- University Research Computing Advisory Committee (Co-Chair) - 2012-2015.
- MGHPCC Research Committee (NU Lead) - 2010-present.
- University Intellectual Property Committee - 2007-2013.
- University Retention Taskforce - 2010-2013.
- COE Research Computing Group, Co-chair, 2014.
- Co-director of the Institute for Information Assurance - 2005-2012.

- ECE Department Council (Chair), 2014-2016.
- ECE Undergraduate Study, (Chair) 2005-2010, 2013.
- NU Academic Research Computing Users Group Chair, 2006-2008.
- ECE Faculty Search Committee in Architecture and Computation Chair, 2014-present.
- ECE Faculty Search Committee in NeuroComputing Chair, 2013-2014.
- ECE Graduate Admissions Chair, 1995-2000.
- ECE Undergraduate Study Committee Member, 1999-present.
- College of Engineering Computer Committee, 1994-2000, 2002-2003.
- ECE Faculty Search Committee Chair - 1994-1998.
- ECE Faculty Search Committee Chair - 1994-1998.
- ECE Faculty Search Committee Member - 1998-2000, 2005, 2009, 2013.
- ECE Tenure and Promotion Committee - 1999-2000, 2002-2006, 2009(chair), 2014-2016.

Courses Taught

- Embedded Design - Enabling Robotics (undergraduate)
- Computer Architecture (both undergraduate and graduate)
- Advanced Computer Architecture (graduate)
- Parallel Computing (undergraduate)
- Computer Security (graduate)
- Software Engineering (both undergraduate and graduate)
- Profiling and Instrumentation (graduate)
- VLSI Design (undergraduate)
- Digital Design (undergraduate)
- Introduction to Programming (undergraduate)
- Engineering Programming Models (undergraduate)

Teaching Awards

- **University Teaching Award** - nominated, 1996, 1997, 2012, 2013.
- **COE Teaching Award** - Student Speaks Award, 2011.

- **Most Outstanding ECE Professor Award** - Northeastern University Eta Kappa Nu Award, 1996, 2016.

Present Ph.D. Students

- Nicolas Bohm Agostini, Zhongliang Chen, Shi Dong, Navid Farazmand, Xiang Gong, Xun Gong, Julian Gutierrez, Jack Harwood, Charu Kalra, Elmira Karimi, Akshay Lahiry, Xiangyu Li, Amir Momeni, Saoni Mukherjee, Fanny Nina Paravecino, Fritz Previlon, Yifan Sun, Leiming Yu, Amir Kavian Ziabari

Present MS Students

- Trinayan Baruah, Brad Courville