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### **Education**

BSEE 1981 Rutgers University  
MSCE 1985 Syracuse University  
PhD 1992 Rutgers University

### **Positions Held**

1981-1986 Staff Engineer, IBM Enterprise Systems, Poughkeepsie, NY  
1986-1993 Advisory Engineer, IBM T.J. Watson Research Center, Yorktown Heights, NY  
1993-1999 Assistant Professor, Northeastern University, Boston, MA  
1999-2005 Associate Professor, Northeastern University, Boston, MA  
2005-present Full Professor, Northeastern University, Boston, MA  
2009-present Associate Dean, College of Engineering, Northeastern University, Boston, MA  
2001-2002 Visiting Professor, Universitat Politecnica de Catalunya, Barcelona, Spain

## Journal Publications

1. “Guest Editor’s Introduction: Special Issue on High-Performance Computing with Accelerators,” with D. Bader and V. Kindratenko, *IEEE Transactions on Parallel and Distributed Systems*, Vol. 22, No. 1, pp. 3-6, January 2011.
2. “Virtual Machine Monitor-based Lightweight Intrusion Detection,” with F. Azmandian, M. Moffie, M. Alshawabkeh, J. Dy and J. Aslam, *ACM Operating Systems Reviews*, July 2011.
3. “Data Structures and Transformations for Physically Based Simulations on a GPU,” with P. Mistry, D. Schaa, B. Jang, A. Dvornik and D. Meglan, *High Performance Computing for Computational Science*, Lecture Notes in Computer Science, No. 6449, Springer 2011.
4. “Exploiting Memory Access Patterns to Improve Memory Performance in Data Parallel Architectures,” with B. Jang, D. Schaa and P. Mistry, *IEEE Transactions on Parallel and Distributed Computing*, 22(1), 2011, pp. 105-118.
5. “AGAMOS: A Graph-Based Approach to Modulo Scheduling for Clustered Microarchitecture,” with A. Aleta, J.M. Codina and A. Gonzalez, *IEEE Transactions on Computers*, 58(6), June 2009, pp. 770-783.
6. “Special issue: General-purpose Processing Using Graphics Processing Units,” with M. Leeser, *Journal of Parallel and Distributed Computing*, 68(10), 2008, pp. 1305-1306.
7. “Soft Error Susceptibility Analysis of SRAM-Based FPGAs in High-Performance Information Systems,” with G. Asadi, V. Sridharan, T. Tahoori and K. Granlund, *IEEE Transactions on Nuclear Science (TNS)*, 54(6), Dec. 2007, pp. 2714-2726.
8. “Characterization of File IO Activity for SPEC CPU2006,” with D. Ye and J. Ray, *Special Issue of ACM SIGARCH Computer Architecture News: SPEC CPU2006 Analysis*, 35(1), 2007, pp. 112-117.
9. “Towards the Development of an Error Checker for Radiotherapy Treatment Plans: A Preliminary Study,” with F. Azmandian and S. Jiang, *Physics in Medicine and Biology*, 52/2007, pp. 6711-6524.
10. “Addressing a Workload Characterization Study of the Design of Consistency Protocols,” with S. Petit, J. Sahuquillo and A. Pont, *Journal of Supercomputing*, Springer-Verlag, 38(1), 2006, pp. 49-72.
11. “Reducing Data Cache Susceptibility to Soft Errors,” with V. Sridharan, G. Asadi and M. Tahoori, *IEEE Transactions on Dependable and Secure Computing*, 3(4): 353-364, 2006.
12. “An Adjustable Linear Time Parallel Algorithm for Maximum Weight Bipartite Matching,” with M. Fayyazi and W. Meleis, *Information Processing Letters*, Elsevier, 97(5): 185-190, 2006.
13. “Power-Aware External Bus Arbitration for System-on-Chip Embedded Systems,” with K. Ning, *Transactions on High-Performance Embedded Architectures and Compilers*, Springer-Verlag, 1(1):94-113, 2006.

14. "Bus Power Estimation and Power-Efficient Bus Arbitration for System-on-a-Chip Embedded Systems," with K. Ning, *Lecture Notes in Computer Science*, Springer-Verlag, Vol. 3471, pp. 95-106, 2005.
15. "Removing Communications in Clustered Microarchitectures Through Instruction Replication," with A. Aleta, J.M. Codina and A. Gonzalez, *ACM Transactions on Architecture and Code Optimization*, Vol. 1, No. 2, June 2004, pp. 127-151.
16. "A Finite State Model for Respiratory Motion Analysis in Image-guided Radiation Therapy," with H. Wu, S. Jiang, G. Sharpe, and B. Salzberg, *Journal of Physics in Medicine and Biology*, 49(23), 2004, pp. 5357-5372.
17. "Developing Object-Oriented Parallel Iterative Methods," with C. Ouarraoui, *International Journal of High Performance Computing and Networking*, Vol. 1, Issue 1/2/3, 2004, pp. 85-90.
18. "Levo - A Scalable Processor With High IPC," with A. Uht, D. Morano and A. Khalafi, *Journal of Instruction Level Parallelism*, Vol. 5, August 2003, pp. 1-35.
19. "A Database System to Advance Subsurface Sensing and Imaging," with H. Wu, B. Norum and B. Salzberg, *Journal of Subsurface Sensing Technologies and Applications*, Vol. 4, No. 4, October 2003, pp. 395-408.
20. "Profile-Based Characterization and Tuning for Subsurface Sensing and Imaging Applications," with M. Ashouei, D. Jiang, W. Meleis, M. El-Shenawee M., E. Mizan, Y. Wang and C. Rappaport, *International Journal of Systems, Science and Technology*, September 2002, pp. 40-55.
21. "Electromagnetics Computations Using the MPI Parallel Implementation of the Steepest Descent Fast Multipole Method (SDFMM)," with M. El-Shenawee, C. Rappaport, D. Jiang and W. Meleis, *ACES Journal*, , Vol. 17, No. 2, July 2002, pp. 112-122.
22. "Introduction to the Special Section on High Performance Memory Systems," with H. Hadimioglu and F. Lombardi, *IEEE Transactions on Computers*, Vol. 50, No. 11, 2001, pp. 1103-1105.
23. "Welcome to the Opportunities of Binary Translation," with E. Altman and Y. Sheffer, *IEEE Computer*, special issue on Binary Translation, March 2000, pp. 40-46.
24. "Indirect Branch Prediction Using Data Compression Techniques," with J. Kalamatianos, *Journal of Instruction Level Parallelism*, (1), 1999, <http://www.jilp.org/vol1/index.html>.
25. "Analysis of Temporal-based Program Behavior for Improved Cache Performance," with J. Kalamatianos, A. Khalafi, and W. Meleis, Special Issue on Cache Memory, *IEEE Transactions on Computers*, Vol.48, No. 2, February 1999, pp. 168-175.
26. "VLSI Design in the 3rd Dimension," with S. Strickland, E. Ergin, and P. Zavracky, *Integration: The Journal of VLSI*, Elsevier, North-Holland, Vol 25/1, September 1998, pp. 1-16.
27. "Tracing and Characterization of NT-based System Workloads," with J. Casmira, and D. Hunter, *Digital Technical Journal*, Vol. 10, No. 1, December 1998, pp. 6-21.

28. "Program Remapping Using Estimated Profiles," with H. Hashemi, B. Calder, J. Kalamantianos and W. Meleis, *Digital Technical Journal*, Vol. 10, No. 2, 1999.
29. "Branch-directed and Pointer-based Data Cache Prefetching," with Y. Liu and M. Dimitri, *Journal of Systems Architecture*, Vol. 45, 1999, pp. 1047-1073.
30. "Creating 3D Circuits Using Transferred Films," with P. Sailer, P. Singhal, J. Hopwood, P.M. Zavracky, K. Warner and P.P. Vu, *IEEE Circuits and Devices Magazine*, November 1997, pp. 27-30.
31. "Performance Analysis on a CC-NUMA Prototype," with L. Fong, D. Renfrew, K. Imming, and R. Booth, *IBM Journal of Research and Development, Special Issue on Performance Tools*, 41, No. 3, May 1997, pp. 205-214.
32. "Improving the Accuracy of History-Based Branch Prediction," with P. Emma, *IEEE Transactions on Computers*, Vol. 46, No. 4, April 1997, pp. 469-472.
33. "Modeling Cache Pollution," with J. Casmira, *International Journal of Modeling and Simulation*, in Vol. 19, No. 2, May 1998, pp. 132-138.
34. "Real-Time Trace Generation," with O. LaMaire, W. White, P. Hennes, and W. Starke, *International Journal of Computer Simulation*, Vol. 6, No. 1, 1996, pp. 53-68.
35. "Issues in Trace-Driven Simulation," *Lecture Notes in Computer Science No. 729, Performance Evaluation of Computer and Communication Systems*, L. Donatiello and R. Nelson eds., Springer-Verlag, 1993, pp. 224-244.
36. "Contrasting Instruction-Fetch and Instruction-Decode Time Branch Prediction Mechanisms: Achieving Synergy Through Their Cooperation Operation," with P. Emma, J. Knight, and T. Puzak, *EuroMicro Journal*, Vol. 35, September 1992, pp. 401-408, also appearing in *Proc. of EuroMicro 92 Software and Hardware Specification and Design*, September 1992.

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1. "Heterogeneous Computing with OpenCL," with B. Gaster, L. Howes, P. Mistry and D. Schaa, Morgan Kaufmann Publishers, August 2011.
2. "GPU Acceleration of Iterative Digital Breast Tomosynthesis," with D. Schaa, B. Brown, B. Jang, P. Mistry, R. Dominguez, R. Moore, and D.B. Koppans, *GPU Computing Gems*, Morgan Kaufmann, 2011, pp. 647-657
3. "Proceedings of the Fourth Workshop on General Purpose Processing on Graphics Processing Units," with J. Cavazos, March, 2011.
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5. "Computer Organization and Design: The Hardware/Software Interface," D.A. Patterson and J.L. Hennessy, 4th edition, contributed the problem set for Chapter 7 on Multicores, Multiprocessors and Clusters.

6. "Computer Performance Evaluation and Benchmarking," D. Kaeli and K. Sachs, editors, *Lecture Notes in Computer Science*, Vol. 5419, January 2009.
7. "General Purpose Computing on Graphics Processing Units," D. Kaeli and M. Leeser guest editors, *Journal of Parallel and Distributed Computing*, Elsevier, October 2008.
8. "High Performance Embedded Architectures and Compilers," K. DeBosschere, D. Kaeli, P. Stentrom, D. Whalley and T. Ungerer editors, Springer Verlag, January 2007.
9. "Recent Speculative Architectures," with D. Morano, a book chapter in "Speculative Execution in Modern Computer Architectures," CRC Press, D. Kaeli and P. Yew Editors, 2005.
10. "Speculative Execution in Modern Computer Architectures," CRC Press, co-editor with P. Yew, 2004.
11. "Microprogramming," a book chapter in *The Wiley Encyclopedia of Electronic and Electrical Engineering*, 3rd edition, edited by John Webster, John Wiley, 2004.
12. "High Performance Memory Systems," Springer-Verlag, 2003, co-editor with H. Hadimioglu, J. Kuskin, A. Nanda and J. Torrellas, eds., Springer Verlag, New York, 2003, ISBN: 03870010X.
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17. "Profile-Tuned Heap Access," with E. Yardimci, in *High Performance Memory Systems*, Springer Verlag, New York, 2003, pp. 153-162.
18. "Digital Computer Architecture," in *The Computer Science and Engineering Handbook*, Allen Tucker, editor, CRC Press, June 2004.
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20. "Proceedings of FTPDS'98," with D. Avresky, edited by J. Rolim, *Lecture Notes in Computer Science*, No. 1388, Springer-Verlag, April 1998, pp. 564-789.
21. "Fault-Tolerant Parallel and Distributed Systems," co-edited with D. Avresky, Kluwer Academic Press, 1998.
22. "Digital Computer Architecture," a book chapter in *The Computer Science and Engineering Handbook*, edited by A.B. Tucker, CRC Handbook, 1997, pp. 412-425.

23. *The DLX Instruction Set Architecture Handbook*, with P.M. Sailer, Morgan Kaufmann Publishing, San Francisco, CA. 1996.
24. *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications, PDPTA'96*, Volumes 1, 2 and 3, co-editor with H.R. Arabnia, B.J. d-Auriol, T. Hazra, R.A. Olsson, Y. Pan, and R. Pande, August 1996.

### Conference Publications:

1. "Workload Characterization at the Virtualization Layer," with F. Azmandian, *Proc. of 19th IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems*, July 2011.
2. "Developing Portable Profiling and Performance Analysis Tools for Heterogeneous Applications," with P. Mistry, D. Schaa, N. Rubin and R. Ubal, *AMD Fusion Summit*, 2011.
3. "Increasing Power/Performance Resource Efficiency on Virtualized Enterprise Servers," with E. Arzuaga, *Proceeding of the 2011 IEEE Computing Frontiers*, Ischia, Italy, May 2011.
4. "Analyzing Program Flow with a Many-kernel OpenCL Application," with P. Mistry, C. Gregg, N. Rubin and K. Hazelwood, *GPGPU-4 Proceedings of the 4th Workshop on General Purpose Processing on Graphics Processing Units*, ACM Conference Proceedings Series, April 2011.
5. "Caracal: Dynamic Translation of Runtime Environments for GPUs," Rodrigo Dominguez, Dana Schaa and David Kaeli, *GPGPU-4 Proceedings of the 4th Workshop on General Purpose Processing on Graphics Processing Units*, ACM Conference Proceedings Series, April 2011.
6. "Macroarchitecture: A Unifying Framework for Manycore Architecture Research," with B. Cordes and G. Schirner, *Proc. of the Workshop on MicroArchitectural Support for Virtualization, Data Center Computing and Clouds*, Dec. 2010.
7. "Interdisciplinary Three-Level Approach to Study Impact of Contamination on Public Health in Puerto Rico," with M.B. Silevitch, R. Giese, T. Sheahan, M. Nobrega, A. Alshawabkeh, J. F. Cordero, I. Padilla R.Loeh-Caruso, J. Meeker, *Proc. of Sixth International Congress on Environmental Geotechnics*, New Delhi, India, November, 2010.
8. "Out-of-Order Retirement of Instructions in Sequentially Consistent Multiprocessors," with R. Ubal, J. Sahuquillo, S. Petit, and P. Lopez, *IEEE International Conference on Computer Design*, 2010, pp. 1-8.
9. "Leveraging Graphical Processor Units for the Acceleration of an Imaging Spectrometry Algorithm in the Littoral Zone," with James Goodman, Dana Schaa and Ayse Yilmazer, *International Symposium on Spectral Sensing Research*, pp. 8, 2010
10. "Accelerating a Hyperspectral Inversion Model for Submerged Marine Ecosystems using High-performance Computing on Graphical Processor Units," with J. Goodman, D. Schaa and A. Yilmazer, *SPIE Defense, Security and Sensing: Algorithms and Technologies for Multispectral, Hyperspectral, and Ultraspectral Imagery XVI*, Vol. 7695, 2010.

11. "Toward Whole-System Dynamic Analysis for ARM-based Mobile Devices," with R. Whelan, *Recent Advances in Intrusion Detection, 13th International Symposium*, Sept. 2010, pp. 512-513
12. "Using Hardware Vulnerability Factors to Improve AVF Analysis," with V. Sridharan, *IEEE/ACM International Symposium on Computer Architecture (ISCA-37)*, June, 2010, pp. 461-472.
13. "Data Structures and Transformations for Physically Based Simulations on a GPU," with P. Mistry, D. Schaa, B. Jang, A. Dvornik and D. Meglan, *9th International High performance Computing for Computational Science (VECPAR)*, online proceedings, 2010.
14. "Accelerating the Local Outlier Factor Algorithm on a GPU for Intrusion Detection Systems," with M. Alshwabkeh, and B. Jang, *Proc. of GPGPU-3*, 2010, pp. 104-110.
15. "Data Transformations Enabling Loop Vectorization on Multithreaded Data Parallel Architectures," with B. Jang, P. Mistry, and D. Schaa, *ACM SIGPLAN Symposium on the Principles and Practice of Parallel Programming*, Jan. 2010, pp. 353-354.
16. "Quantifying Load Imbalance on Virtualized Enterprise Servers," with E. Arzuaga, *ACM Conference on Performance Engineering WOSP/SIPEW*, Jan 2010, pp. 235-242.
17. "A Binary Instrumentation Tool for the Blackfin Processor," with E. Sun, *Proceedings of the Workshop on Binary Instrumentation and Applications*, Dec. 2009.
18. "Improving the Open64 Backend for GPUs," with R. Dominguez, J. Cavazos and M. Murphy, *NVIDIA NVISIONS Workshop*, October 2009.
19. "Profile-Guided Optimization of Critical Medical Imaging Algorithms," with B. Jang, P. Mistry and D. Schaa, *IEEE International Symposium on Biomedical Imaging*, Invited Session, June 2009, pp. 1293-1294.
20. "Multi GPU Implementation of Iterative Tomographic Reconstruction Algorithms," with B. Jang, S. Do and H. Pien, *IEEE International Symposium on Biomedical Imaging*, June 2009, pp. 185-188.
21. "Architecture-aware Optimization Targeting Multi-Threaded Stream Computing," with B. Jang, S. Do, H. Pien, *Proceedings of GPGPU 2009*, pp. 62-70.
22. "Accelerating Phase Unwrapping and Affine Transformations for Optical Quadrature Microscopy Using CUDA," with P. Mistry, S. Braganza, and M. Leeser, *Proceedings of GPGPU 2009*, pp. 28-37.
23. "Software Transactional Memory for Multicore Embedded Systems," with J. Mankin and J. Ardini, *Proceedings of the ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems*, June 2009, pp. 90-98.
24. "Exploring the Multiple-GPU Design Space," with D. Schaa, *IEEE International Parallel and Distributed Processing Symposium*, **Best Paper Award**, May 2009, pp. 1-12.

25. "Eliminating Microarchitectural Dependency from Architectural Vulnerability," with V. Sridharan, Proceedings of the *15th International Conference on High Performance Computer Architecture*, IEEE Computer Society, Feb. 2009, pp. 117-128.
26. "Performance Prediction in Multi-GPU Execution," with D. Schaa, *NVISION'08* August, 2008.
27. "A Taxonomy to Enable Error Recovery and Correction in Software," with V. Sridharan and D. Liberty, *Workshop on Quality-Aware Design (W-QUAD)*, June, 2008.
28. "Quantifying Software Vulnerability," Vilas Sridharan and David R. Kaeli, *WREFT '08: Proceedings of the 2008 workshop on Radiation effects and fault tolerance in nanometer technologies*, May 2008, pp. 323-328.
29. "A Field Analysis of System-Level Effects of Soft Errors Occurring in Microprocessors used in Information Systems," with S. Shazli, M. Abdul-Aziz and M.B. Tahoori, *International Test Conference*, November 2008.
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31. "Field Failure Analysis of Microprocessors used in Information Systems," with S. Shazli, M. Abdul-Aziz and M. Tahoori, *DSN 2008 Workshop on Resilience Assessment and Dependability Benchmarking*, June 2008.
32. "Performance Evaluation of Virtual Appliances," with Z. Chen and K. Murphy, *First International Workshop on Virtualization Performance: Analysis, Characterization, and Tools (VPACT'08)*, April, 2008.
33. "Resource-Conscious Optimization of Cryptographic Algorithms on an Embedded Architecture," with W. Bassalee, Proceedings of the *ACM Workshop on Optimizations for DSP and Embedded Systems*, April 2008, pp. 82-92.
34. "Interactive Deformable Registration Visualization and Analysis of 4D Computed Tomography," with B. Erem, G. Sharp, and Z. Wu, Proceedings of the *1st International Conference on Medical Biometrics*, ICMB Hong Kong, China, January 4-5, 2008, pp. 232-239.
35. "An M/G/1 Queue Model for Multiple Application on Storage Area Networks," with E. Arzuaga, Proceedings of the *11th Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW-11)*, February 2008.
36. "Characterizing the Relationship Between ILU-based Preconditioners and the Storage Hierarchy," with D. Rivera and M. Kilmer, Proceedings of the *International Conference on Preconditioning Techniques for Large Sparse Matrix Problems in Scientific and Industrial Applications*, 2007, pp. 74-77.
37. "Exploring Novel Parallelization Technologies for 3-D Imaging Applications," with D. Rivera, D. Schaa, and M. Moffie, *The 19th Symposium on Computer Architecture and High Performance Computing*, October 2007, pp. 26-35.

38. "Stream Image Processing on a Dual-Core Embedded System," with M. Benjamin, Proceedings of the *Embedded Computer Systems: Architectures, Modeling, and Simulation, 7th International Workshop, SAMOS 2007*, Samos, Greece, July 2007, also appearing in *Lecture Notes in Computer Science*, Springer 2007, pp. 185-194.
39. "Reliability in the Shadow of Long-Stall Instructions," with V. Sridharan and A. Biswas, Proceedings of the *3rd Workshop on Silicon Errors in Logic - System Effects (SELSE-3)*, April 2007.
40. "External Memory Page Remapping for Embedded Multimedia Systems," with K. Ning, Proceedings of the *ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems*, June 2007, pp. 185-194.
41. "Heterogeneous Clustered VLIW Microarchitectures," with A. Aleta, J.M. Codina, A. Gonzalez and D. Kaeli, Proceedings of the *5th IEEE International Symposium on Code Generation and Optimization*, March 2007, pp. 354-366.
42. "Case Study: Soft Error Rate Analysis in Storage Systems," with B. Mullins, H. Asadi, M. Tahoori, K. Granlund, R. Bauer, and S. Romano, Proceedings of the *25th IEEE VLSI Test Symposium*, May 2007, pp. 256-264.
43. "Use of an Embedded Configurable Memory for Stream Image Processing," with M. Benjamin, Proceedings of the *5th Workshop on Optimizations for DSP and Embedded Systems*, March 2007, pp. 14-20.
44. "A Code Layout Framework for Embedded Processors with Configurable Memory Hierarchy," with K. Sanghai, A. Raikman and K. Butler," Proceedings of the *5th Workshop on Optimizations for DSP and Embedded Systems*, March 2007, pp. 29-38.
45. "Stream Programming on the Blackfin Architecture," with M. Benjamin, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 29-30.
46. "Characterizing the Relationship Between Sparse Matrix Preconditioners and the Storage Hierarchy," with D. Rivera and M. Kilmer, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 37-38.
47. "Performance Characterization of SPEC CPU2006 Integer Benchmarks," with D. Ye and J. Ray, Proceedings of the *4th Boston Area Computer Architecture Workshop*, January 2007, pp. 67-72.
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52. "Performance Characterization of SPEC CPU2006 Integer Benchmarks on the x86-64 Architecture," with D. Ye, C. Harle, and J. Ray, Proceedings of the *IEEE Symposium on Workload Characterization*, invited paper, October 2006, pp. 120-129.
53. "Experiences with the Blackfin Architecture for an Embedded Systems Lab," with M. Benjamin and R. Platcow, Proceedings of the *Workshop on Computer Architecture Education*, July 2006. pp. 3-9.
54. "Vulnerability Analysis of L2 Cache Elements to Single Event Upsets," with H. Asadi, V. Sridharan and M. Tahoori, Proceedings of *Design Automation and Test in Europe (DATE) Conference*, March 2006, pp. 1276-1281.
55. "Visualization of 4-D Computed Tomography Images," with N. Dedual and G. Chen, Proceedings of the *IEEE Southwest Symposium on Image Analysis and Interpretation*, March 2006, pp. 120-123.
56. "Model-based Probabilistic Prediction of Tumor Respiratory Motion," with H. Wu, G. Sharp, B. Salzberg, D. Kaeli, H. Shirato and S. Jiang, Proceedings of the *47th Annual Meeting of the American Association of Physicists in Medicine (AAPM)*, 2005.
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58. "ASM: An Application Security Monitor," with M. Moffie and W. Cheng, Proceedings of the *Workshop on Binary Instrumentation and Applications (WBIA '05)*, September 2005, pp. 31-36.
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60. "Load Balancing using Grid-based Peer-to-Peer Parallel I/O," with Y. Wang, Proceedings of the *2005 IEEE Cluster Computing Conference*, Boston, MA, 2005.
61. "Power Aware External Bus Arbitration for System-on-a-Chip Embedded Systems," with K. Ning, Proceedings of *HIPEAC*, November, 2005, pp. 95-106.
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63. "A Multinomial Clustering Model for Fast Simulation of Computer Architecture Designs," with K. Sanghai, T. Su, and J. Dy, *Proceedings of the 11th ACM SIGKDD International Conference on Knowledge Discovery and Data Mining*, Aug. 2005, pp. 808-813.

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65. "Demystifying On-the-Fly Spill Code," with A. Aleta, J.M. Codina, and A. Gonzalez, *Proc. of the ACM Conference on Programming Languages, Design and Implementation (PLDI)*, 2005, pp. 180-189.
66. "Code and Data Partitioning on the Blackfin 561 Dual-core Platform," with K. Sanghai and R. Gentile, *Proc. of the Workshop on Optimization of DSP and Embedded Systems*, March 2004, pp. 92-100.
67. "A MATLAB Toolbox for Hyperspectral Image Analysis," with E. Arzuaga-Cruz, L.O. Jimenez-Rodriguez, M. Velez-Reyes, M., E. Rodriguez-Diaz, H.T. Velazquez-Santana, A. Castrodad-Carrau, L.E. Santos-Campis, C. Santiago, *Geoscience and Remote Sensing Symposium*, Vol. 7, Sept. 2004, pp. 4839-4842.
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70. "Bus Power Estimation and Power-Efficient Bus Arbitration for System-on-a-Chip Embedded Systems," with Ke Ning, *Workshop on Power Aware Computing Systems*, December 2004.
71. "Execution-Driven Simulation of Network Storage Systems," with Y. Wang, *Proceedings of the 12th ACM/IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS)*, October 2004, pp. 604-611.
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73. "A Reliable Return Address Stack: Microarchitectural Features to Defeat Stack Smashing," with D. Ye, *Proceedings of the Workshop on Architectural Support for Security and Anti-Virus*, October 2004, pp. 69-76, also appearing in *ACM SIGARCH News*, March 2005.
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76. "A Study of Errant Pipeline Flushes caused by Value Misspeculation," with D. Balkan and J. Kalamatianos, *The 15th Symposium on Computer Architecture and High Performance Computing*, October 2004, pp. 32-39.

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- **Associate Editor** - IEEE Computer Architecture Letters, December 2001 - 2011.
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- **Co-Editor** - IEEE Computer Magazine, special issue on Binary Translation, March 2000.
- **Co-Editor** - UNESCO Encyclopedia on Life Sciences, Volume on Computer Sciences, June 2000.
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### **Invited and Tutorial Talks:**

1. "Biomedical Computing with GPUs," *Analogic Corporation*, May 2011.
2. "Adventures in Desktop Supercomputing," *Keynote at the 24th Annual CCSC:Southeastern Conference at Spelman College*, November 2010.
3. "Macroarchitecture: A Unifying Framework for Manycore Architecture Research," *Workshop on Micro Architectural Support for Virtualization, Data Center Computing, and Clouds*, December 2010.
4. "GPU Computing - Low-cost High-performance Embedded Computing," *Analogic Distinguished Lecture Series*, October 2010.
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9. "Many-core Computing: A Disruptive Technology Enabling Low-cost, Low-power Desktop Computing Organization/Sponsor," Keynote Talk, *IEEE Systor Conference*, May 2010.
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20. \$28,100 “Analog Devices Unrestricted Gift for 2009 Student Support,” Analogic Devices, 2009.
21. \$1,300,000, “Biomedical Imaging Acceleration Toolbox,” NSF-ERC Innovation Program, Dec. 2009.

22. \$1,935,701, "Multi-disciplinary Preparation of Next Generation Information Assurance Practitioners," NSF DUE, Nov. 2008.
23. \$50,000, "Binary Translation and Optimization on Larrabee," Intel Corporation, November 2008.
24. \$67,631, "CRI:CRD Collaborative Research: Archer - Seeding a Community-based Computing Infrastructure for Computer Architecture Research and Education," (PI), NSF-CRI Program, April 15, 2008.
25. \$61,146, "Benchmarking Virtual Machine Performance," (PI) Network Engines, May 2008.
26. \$25,000, "A Binary Translation Layer for ATI Stream Computing," (PI) AMD, May 2008.
27. \$46,007, "Draper Research Fellowship," (PI) Draper Labs, Cambridge MA., July 2007.
28. \$6,656, "Akorri Funding," (PI) Akorri Funding, May 2007.
29. \$57,899, "Modeling and Performance Analysis of Multiple Virtual Machines working in Context," (PI) Network Engines, March 2007.
30. \$150,000, "Commercial Grade Automatic and Manual Parallelization and Performance Tools," NSF STTR, January 2007.
31. \$199,999, "MRI/Acq: Enabling Research on Terabyte-Scale Datasets," (co-PI) National Science Foundation, May 2006.
32. \$113,352, "Soft-Error Modeling," (co-PI) EMC, Hopkington, MA., April 2006.
33. \$40,973, "Draper Research Fellowship," (PI) Draper Labs, Cambridge MA., July 2006.
34. \$55,000, "BlackFin Research," (PI) Analog Devices, Norwood, MA., (PI), April 2006.
35. \$23,000, "BlackFin Research," (PI) Analog Devices, Norwood, MA., (PI), September 2005.
36. \$10,000, "Parallelization of Segmentation Codes," (co-PI) Massachusetts General Hospital, September 2005.
37. \$50,000, "BlackFin Research," (PI) Analog Devices, Norwood, MA., (PI), October 2004.
38. \$500, "Undergraduate Research," (PI) NU Provosts Office, Northeastern University (PI), October 2004.
39. \$12,107, "Developing Power-Aware Compilation Strategies For the Blackfin Platform," (PI) Analog Devices, Norwood, MA., (PI), July 2004.
40. \$300,000 "Collaborative Research: Tuning Libraries to Effectively Exploit the Memory Hierarchy," National Science Foundation, Advanced Computational Research Program, (PI), January 2004.
41. \$1,000 "Boston Area Computer Architecture Research Workshop," (PI), Intel Corporation, Santa Clara, CA, January 2004.

42. \$22,400 “NSF REU Grant,” (PI), December 2003.
43. \$30,673, “Partitioning of Multimedia Applications on a Multi-core Blackfin Platform,” (PI), Analog Devices, Norwood, MA., October 2003.
44. \$23,546 “Developing Power-Aware Compilation Strategies For the Blackfin Platform,” (PI) Analog Devices, Norwood, MA., October 2003.
45. \$241,043 “Architectural Features for Virus Detection and Recovery,” (PI), National Science Foundation, Computer Systems Architecture Program, Aug. 2003.
46. \$681,674 “Institute of Complex Software Science, (co-PI), ICSS, 5 years, 2002.
47. \$19,463 “Software-Defined Radio,” (PI), Mercury Computer Systems, January 2002.
48. \$25,000 “Foreign Visitors Program,” (PI), Spanish Ministry of Education and Sports, September 2001.
49. \$9,734 “Research at UPC Barcelona, Spain,” (PI), NSF Supplemental Award - NSF International Program, July 2001.
50. \$74,961 “Profile-Guided Optimization and Parallelization Targeting Mercury Dataflow Architectures,” (PI), Mercury Computer, December 2000.
51. \$500,000 “Mercury RACE-system Grant,” (PI), Mercury Computer, December 2000.
52. \$45,243 “FRIO Processor Performance,” (PI), Analog Devices, May 2000.
53. \$10,000 “NSF REU Grant,” (co-PI), September 2000.
54. \$43,000 “Compaq Corporation Funding,” (PI), October 2000.
55. \$16,500,000(estimated) “An Engineering Research Center for Subsurface Sensing and Imaging System,” NSF (Senior Investigator, many PIs), NSF ERC Program, September 2000.
56. \$143,000 “A Memory Intensive Compilation Environment Targeting VLIW and DSP Architectures, NSF MRI Program, (co-PI), September 2000.
57. \$21,000 “IBM Partnership Award,” (PI), IBM Corporation, August 1999.
58. \$255,427 “Interprocedural Value-Based Program Optimization,” National Science Foundation, (co-PI) July 1999.
59. \$5,000 “Undergraduate Research Fellowship,” Sun Microsystems, (PI), June 2000.
60. \$32,000 “Compaq Research Grant,” (PI), Compaq Corporation, May 1999.
61. \$25,778 “Shared University Research Grant,” IBM Corporation, (PI), September 1998.
62. \$329,794 “A High-Performance, Low-Cost Testbed for Network-based Research,” NSF Major Research Instrumentation Program, (co-PI), August 1998.

63. \$30,000 “Data/Knowledge Bases for Image Generation,” Northeastern Pre-ERC Funding, (PI with R. Futrelle), Northeastern University, June 1998.
64. \$35,000 “Prototype Low-cost Parallel/Distributed Testbed,” Northeastern Pre-ERC Funding, (PI with D. Brooks), Northeastern University, June 1998.
65. \$30,000 “ IBM Partnership Award,” (PI), IBM Corporation, August 1998.
66. \$22,000 “EMC/NUCAR Joint Research Program,” (PI), EMC Corporation, December 1997.
67. \$84,198 “Development of a DSP Compilation Testbed,” Proposal Number: NCRI: 97-29856, (PI with W. Meleis and J. Proakis), National Science Foundation, 1997-1998.
68. \$35,000 “Compiler Research,” (PI), Microsoft Research, August 1997.
69. \$12,000 “Design in the 3rd Dimension,” (PI), Design Automation Conference, June 1997.
70. \$59,000 “Research on Plasma Etching of Vias for 3-D Microelectronics,” (co-PI), Office of Naval Research, April 22, 1996.
71. \$79,946 “Three-Dimensional Electronics Using Transferred SOI Films,” (co-PI), Kopin Corporation, 1994.
72. \$200,000 “Three-Dimensional Electronics Using Transferred SOI Films,” (co-PI), Kopin Corporation, 1994-1997.
73. \$131,995 “CAREER Program: Research and Education Plan,” NSF CAREER Program, Grant Number 95-01172, (PI), 1995-1998.
74. \$25,000 “Open Systems I/O Characterization,” (PI), EMC Corporation, June 1996.
75. \$21,708 “Autobahn Research,” Data General Corporation, (PI), July 1996.
76. \$21,000 “Tools and Techniques for Open System I/O Tracing,” (PI), EMC Corporation, Oct. 1996.
77. \$5,000 “Studying the Characteristics of I/O Database Mining,” (PI), Northeastern University College of Engineering, 1996.

### **Equipment/Software Donations**

1. \$10,000, “Developing a GPU Teaching and Research Testbed,” NVIDIA, January 2008.
2. \$14,000, “VI3 ESX Server Licenses,” VMWare, November 2007.
3. \$38,585, “BlackFin BF561s with FPGAs,” Analog Devices, January 2006.
4. \$1,500 “EEMBC Benchmark Consortium Membership,” EEMBC, June 2004.
5. \$3,400 “Power Measurement Equipment,” Analog Devices, May 2004.
6. \$8,000 “BlackFin BF533 Easykits,” Analog Devices, August 2003.

7. \$5,200 “RTExpress Licenses,” Integrated Sensors Incorporated, May 2001.
8. \$5,319,050 “Synopsys Software Licenses Renewal,” Synopsys Corp., January 2000.
9. \$15,683 “Alpha Miata Machines,” Compaq Corporation, May 1999.
10. \$20,000 “EDG Compilation Toolset,” Edison Design Group, April 1997-2000.
11. \$15,610 “Microsoft Software Licenses,” Microsoft Corporation, August 1997.
12. \$10,740 “Alpha PC-164 Gift,” Digital Equipment Corporation, April 1997.
13. \$300,000 “EMC Centriplex Donation,” EMC Corporation, December 1996.
14. \$6,000 “SCSI-bus Analyzer,” EMC Corporation, June 1996.
15. \$6,144,013 “Synopsys University Program,” April 1996.
16. \$77,688 “Hewlett Packard Equipment Grant,” January 1995.

### **Panels, Program Chairs and Committees**

- **Committee Member** - IEEE Computer Society Fellows Selection Committee, 2010, 2011.
- **Panel Member** - Natural Sciences and Engineering Research Council Strategic Project Grants Program, 2010, 2011.
- **Panel Member** - Austrian Science Fund Program, 2009.
- **Panel Member** - NSF CAREER Awards, November 1998, October 2003, October 2005, October 2006, October 2007.
- **Panel Member** - NSF CyberTrust PI Meeting, August 2004.
- **Panel Member** - NSF ITR Panel, May 2004.
- **Panel Member** - NSF Next Generation Software Program, 2001.
- **General Co-Chair** - ACM ICPE, 2012, Boston, MA.
- **General Chair** - ACM/IEEE ISCA, 2006, Boston, MA.
- **General Co-Chair** - ACM/IEEE PACT, 2003, New Orleans, LA.
- **General Co-chair** - IEEE HPCA-8, 2002, Cambridge, MA.
- **General Co-chair** - High Performance Embedded Architectures and Compilers, 2007.
- **Program Chair** - IEEE CGO 2010.
- **Program Chair** - SPEC 2009 Workshop.
- **Program Chair** - IEEE International Symposium on Workload Characterization, 2005.

- **Program Vice-Chair** - IEEE Frontiers, 2007.
- **Program Vice-Chair** - IEEE International Symposium on Parallel and Distributed Systems (IPDPS), 2008.
- **Program Vice-Chair** - IEEE International Conference on Parallel and Distributed Systems (ICPADS), 2006.
- **Benchmark Chair** - IEEE Symposium on Workload Characterization, 2006.
- **Program Committee Member** - ACM/IEEE ISCA, 2008, 2011.
- **Program Committee Member** - ACM/IEEE MICRO, 2001, 2003, 2004, 2005, 2008, 2011.
- **Program Committee Member** - ICCD, 2010, 2011.
- **Program Committee Member** - FGC , 2010, 2011.
- **Program Committee Member** - AINA , 2011.
- **Program Committee Member** - AMAS-BT , 2010, 2011.
- **Program Committee Member** - NaBIC , 2011.
- **Program Committee Member** - NPC , 2011.
- **Program Committee Member** - SAAHPC , 2009, 2010, 2011.
- **Program Committee Member** - VALID, 2011.
- **Program Committee Member** - WACY, 2011.
- **Program Committee Member** - GPGPU, 2008, 2009, 2010, 2011.
- **Program Committee Member** - ACM International Conference on Scientific and Statistical Database Management, 2004.
- **Program Committee Member** - IEEE HPCA, 1999, 2002, 2004, 2007, 2008, 2011.
- **Program Committee Member** - MEDEA Workshop, 2000, 2003, 2004, 2006.
- **Program Committee Member** - MTEAC Workshop, 2000-2002, 2007.
- **Program Committee Member** - WMPI Workshop, 2004, 2005.
- **Program Committee Member** - ICPP-HPSEC04, 2004.
- **Program Committee Member** - IEEE ISPASS, 2002-2006.
- **Program Committee Member** - IEEE Frontiers, 2004, 2007, 2008.
- **Program Committee Member** - IEEE PACT, 2000.

- **Program Committee Member** - SBAC-PAD, 2004, 2005, 2006, 2007.
- **Program Committee Member** - CGO 2008.
- **Program Committee Member** - ICPP, 2002.
- **Program Committee Member** - IPDPS, 2004.
- **Program Committee Member** - Workshop on Storage Networks Architecture and Parallel IO, 2003, 2004.
- **Program Committee Member** - Conference on Communication Networks and Distributed Modeling and Simulation, SCS, 2002.
- **Program Committee Member** - IEEE Workshop on Workload Characterization, 2000-2004.
- **Program Committee Member** - Annual Simulation Symposium, 2000-2006.
- **Program Committee Member** - 9th IASTED International Conference on Parallel and Distributed Computing and Systems, 1997.
- **Program Committee Member** - Interaction between Compilers and Computer Architectures, 2000-2001.
- **Program Committee, Technical Committee** - SHARC, Boston, MA, September 2000.
- **Program Committee Member** - Workshop on Embedded Fault-Tolerant Systems, Dallas, TX, 1996.
- **Program Committee Member** - International Conference on Parallel and Distributed Processing Techniques and Applications, Sunnyvale, CA., 1996.
- **Registration Chair** - ACM ASPLOS, 2004.
- **Tutorial Chair** - IEEE HPCA-10, 2003.
- **Panel Member** - Canada Foundation for Innovation, Ottawa, Ontario, February 2002.
- **Organizer** - Workshop on Architecture and System Support for Improving Software Dependability, 2006.
- **Organizer** - Workshop on Architectural Support for Security and Anti-virus, 2004.
- **Co-Organizer** - Workshop on Memory Performance Issues, May 2002, Alaska.
- **Co-Organizer** - Workshop on Memory Performance Issues, July 2001, Goteborg, Sweden.
- **Program Committee Member** - International Symposium on Performance Analysis of Software and Systems, 2001.
- **Co-Organizer** - Workshop on Binary Instrumentation and Applications, 2005, 2006.

- **Co-Organizer** - 3rd Workshop on Binary Translation, September 2001.
- **Local Arrangements Chair** - ACM Sigmetrics, Cambridge, MA, June 2001.
- **Local Arrangements Chair** - ACM ASPLOS, Cambridge, MA November 2001.
- **Local Arrangements Chair** - 9th ACM Conference on Architectural Support for Programming Languages and Operating Systems, November 2000.
- **Co-Organizer** - 1st Workshop on Solving the Memory Wall, June 2000.
- **Co-Organizer** - 2nd Workshop on Binary Translation, Philadelphia, PA, 2000.
- **Co-Organizer** - 1st Workshop on PC-based System Performance Analysis, Santa Clara, CA, October, 1998.
- **Organizer** - 4th International Workshop on Computer Architecture Education, Las Vegas, NV, February 1998.
- **Co-Organizer** - Workshop on Computer Architecture Education, Barcelona, Spain, June 1998.
- **Tutorial and Workshop Chair** - 8th ACM Conference on Architectural Support for Programming Languages and Operating Systems, San Jose, CA, October 1998.
- **Co-organizer** - 3rd Annual Workshop on Fault-Tolerant Parallel and Distributed Systems, in conjunction with the 12th International Parallel Processing Symposium, Orlando, FL, April 1998.
- **Co-Organizer** - 2nd Annual Workshop on Fault-Tolerant Parallel and Distributed Systems, in conjunction with the 11th International Parallel Processing Symposium, Geneva, Switzerland, April 1997.
- **Organizer** - 3rd International Workshop on Computer Architecture Education, San Antonio, TX, February 1997.
- **Tutorial and Workshop Chair** - 3rd International Conference on High Performance Computer Architecture, San Antonio, Texas, February 1997.
- **Co-Organizer** - Workshop on Fault-Tolerant Parallel and Distributed Systems, in conjunction with the 10th International Parallel Processing Symposium, Honolulu, HA, April 1996.
- **Organizer** - 2nd International Workshop on Computer Architecture Education, San Jose, CA, February 1996.
- **Organizer** - Workshop on Undergraduate Computer Architecture Education, Santa Margherita, Italy, June 1995.
- **Workshop Chair** - IEEE/ACM PACT, 2004.

- **Organizer** - 1st International Workshop on Computer Architecture Education, Raleigh, N.C., January 1995.

### **Professional Activities:**

- **Chair** - IEEE Technical Committee on Computer Architecture, 2009-present.
- **Chair** - IEEE Technical Committee on Microarchitecture and Microprogramming, 2007-2010.
- **Vice-Chair** - IEEE Technical Committee on Computer Architecture, 2006-present.
- **Member** - NSF TeraGrid Scientific Advisory Board, 2007-present.
- **Member** - CRA Computing Community Consortium, 2007-present.
- **Member-at-Large** - ACM SIGMICRO - 2006-present.
- **Executive Committee** - IEEE Technical Committee on Computer Architecture, 2000-present.
- **Chair** - IEEE Technical Committee on Microprogramming and Microprocessors, 2007-2009.
- **Treasurer** - ACM SIGMICRO - 2006-2008.
- **Director** - ACM SIGMICRO Awards Program, November 2001-2005.
- **Chair** - Sigmetrics Corporate Sponsor Program - 1994-95.

### **Other Honors:**

- **Teaching Award** - Student Speaks Award, 2011.
- **IEEE Fellow** - 2010.
- **Outstanding Service Award** - SPEC, 2009.
- **Outstanding Researcher Award** - Northeastern University College of Engineering, 2009.
- **Mentorship Award** - Northeastern University College of Engineering, 2007.
- **Distinguished Researcher Award Program** - Northeastern University Provost's Office, 2004, 2005, 2006.
- **Most Outstanding ECE Professor Award** - Northeastern University Eta Kappa Nu Award, 1996
- **Eta Kappa Nu Engineering Honor Society**
- **Sigma Xi Honor Society**
- **Who's Who in Teaching in America, 1996**

- **Nominated for University-wide Faculty Teaching Award, 1996, 1997**

#### **Consulting and Textbook Reviews:**

- **CTO of NUIC Technologies, 2007-present**
- **Consultant for Akorri Networks, Littleton, MA, 2005-present**
- **Consultant for InCert Corporation, Cambridge, MA, 2000**
- **Motorola Paging Systems, Boynton Beach, FL, 1997-98**  
Course developer for the Motorola Architecture Leadership Program
- **Intel Corporation, Santa Clara, CA, 1997**  
Expert witness in the Intel-DEC patent lawsuit case
- **Dynamics Research Corporation, West Newton, MA 1994**  
Education on Object-oriented Design and C++ Programming
- **Modular Computing Technology, Concord, MA 1993**  
Performance modeling and simulation of client-server platforms
- **Various publishers including: Morgan Kaufmann, CRC, Elsevier, Weste, McGraw Hill**  
Reviewing textbooks and proposals for texts

#### **Graduate Students:**

##### **Defended Ph.D. Theses**

1. Dr. Amir Hooshang Hashemi, *Efficient Procedure Mapping for Improved Cache Performance*, PhD, May 1996.
2. Dr. John Kalamatianos, *Microarchitectural and Compile Time Optimizations for Performance Improvement of Procedural and Object Oriented Languages*, PhD, January 2000.
3. Dr. Alireza Khalafi, *Exploring Multipath Execution on a Distributed Microarchitecture*, PhD, June 2003.
4. Dr. Jennifer Black, *Multi-criteria Data Flow Testing*, PhD, August 2003.
5. Dr. Marcos de Alba, *Exposing Instruction Level Parallelism in the Presence of Loops*, PhD, December 2003.
6. Dr. Morteza Fayyazi, *Fault-Tolerant and Efficient Cluster Switch Architecture*, PhD, April 2005.
7. Dr. Huanmei Wu, *Time-based Indexing of Multidimensional Databases*, PhD, May 2005.
8. Dr. David Morano, *Exploring Instruction Level Parallelism Using Resource Flow Execution*, PhD, April 2006.

9. Dr. Yijian Wang, *Modeling and Acceleration of File-IO Dominated Parallel Workloads*, PhD, December 2006.
10. Dr. Ke Ning, *System-Level Memory Power and Performance Optimization for System-on-a-Chip Embedded Systems*, PhD, May 2007.
11. Dr. Micha Moffie, *Investigating the Utility of Software Semantics for Host-based Intrusion Detection Systems*, PhD, August 2008.
12. Dr. Vilas Sridharan, *The System Vulnerability Stack: Abstraction for Vulnerability Assessment*, PhD, May 2010.
13. Dr. Byunghyun Jang, *Evaluation and Enhancement of Memory Efficiency Targeting General-Purpose Computations on Scalable Data-Parallel GPU Architectures*, PhD, December 2010.

### **Defended MS Theses**

1. Angela Sampogna, *Architectural Implications of C and C++ Programming Models*, MSEE 1995
2. Yue Liu, *Analysis of Branch Directed Data Cache Prefetching*, MSEE 1995
3. Samson Belayneh, *The Effect of Balanced Instruction Scheduling on the Performance of Non-Blocking Caches*, MSEE 1996
4. Himanshu Sinha, *Non-blocking Caches in Shared Memory Multiprocessors*, MSEE 1996
5. John Fraser, *Cache Analysis in a Multiprocess Environment Using Execution Driven Simulation*, MSEE 1996
6. Mona Dimitri, *Cache Pointer-Based Prefetching for Complex Data Structures*, MSCSE 1997
7. Svetlana Sokolova, *Static Branch Prediction Using High-Level Control Structure*, MSEE 1997
8. Tracy Tao, *Branch Prediction With Branch History Chain Table for Wide-Issue Superscalar Processors*, MSEE 1998
9. Jason Casmira, *Operating System Rich Workload Characterization*, MSEE 1998
10. Mekalu Teshome, *I/O Cache Structures and System Performance*, MSEE 1998
11. Kyle Bowers, *Characterization of the Java Virtual Machine*, MSEE 1999.
12. Hua Huang, *A Buffering Scheme for Improved BSD Fast File System Performance*, MSEE 1999.
13. Ying Liu, *A Channel Routing Algorithm for 3-D VLSI*, MSEE 1999.
14. Manpreet Singh, *Scalable Interconnects and Topologies for High Performance ICDSs*, MSEE 1999.

15. Philip Sailer, *YIFAN is a Pure RISC in a Three-Dimensional Integrated Circuit*, MSEE 2000.
16. Hakan Aydin, *Exploring the Effects of Cache Line Coloring and Procedure Inlining*, MSEE 2000.
17. Efe Yardimci, *Profile-guided Heap Layout*, MSEE, 2001.
18. Songqing Zhang, *BDSPTune: Binary-level Instrumentation of the SHARC DSP*, MSEE, 2001.
19. Murat Bicer, *A Software Communications Architecture Compliant Software Defined Radio Implementation*, MSEE 2002.
20. Deniz Balkan, *Side-Effects of Value Speculation on Branch Resolution and Performance in Out-of-Order Superscalar Microprocessors*, MSEE 2003.
21. Stephen VanderSanden, *Developing Power-Aware Strategies for Embedded DSPs*, MSEE 2004.
22. Anita Thomas, *Value Prediction with Perceptrons*, MSEE 2004.
23. Darren Ng, *Aspect Oriented Garbage Collection*, MSEE 2005.
24. Kaushal Sanghai, *A Code Layout Framework for Embedded Processors with a Configurable Memory Hierarchy*, MSEE 2005.
25. Vilas Sridharan, *Soft Errors in Cache Memories*, MSEE 2006.
26. Diego Rivera, *Accelerating Sparse Matrix Computations*, MSCSE 2007.
27. Brian Mullins, *Soft Errors in Storage Systems*, MSECE 2007.
28. Michael Benjamin, *A Study of Video Processing using Stream Computing on Blackfin Processors*, MSECE 2007.
29. Fatemeh Azmandian, *The Chart Checker: Applying Data Mining Techniques to Detect Major Errors in Radiotherapy Treatment Charts*, MSECE 2008.
30. Seth Molloy, *Energy Conservation Techniques for the Blackfin Processor*, MSEE, 2008.
31. Burak Erem, *Interactive Deformable Registration Visualization and Analysis of 4D Computed Tomography*, MSEE 2008.
32. Derek Uluski, *Real Time Anti-virus for a Virtualized Environment*, MSECE 2008.
33. Wassim Bassalle, *Optimization of Cryptographic Algorithms on an Embedded Architecture*, MSECE 2008.
34. Zhaoqian Chen, *Performance Evaluation and Characterization of Virtual Appliances*, MSECE 2008.
35. Dana Schaa, *Multi-GPU Performance Modeling*, MSECE 2009.

36. Jenny Mankin *Embedded System Transactional Memory*, MSECE 2009.
37. Yungho Yang *Memory Forensics on Embedded Linux*, MS Project 2009.
38. Sarmad George *Multi-core Reliability*, MS Project 2009.
39. Tong Pan *Mapping Decision Tree Algorithms to GPUs*, MSECE 2010.
40. Roberto Cabral *Upgrading a Fieldable Air Traffic Control Interrogator*, MSECE 2010.
41. Joshua Hodosh *Memory System Introspection*. MSECE 2010.
42. Kin Kone Kito *Power profiling on Embedded Processors*, MSECE 2010.
43. Kevin McKinley *GPU Acceleration in a Gordon Challenge Project*, MS Project 2010.
44. Kulin Seth *Heterogeneous System Modeling*, MSECE 2011.
45. Stephen Maresh *Using HAsim to Model a Re-Order Buffer*, MS Project 2011.

#### **University/College/Department Service**

- Associate Dean for Undergraduate Programs - 2010-present.
- University Intellectual Property Committee - 2007-present.
- University Retention Taskforce - 2010-present.
- Co-director of the Institute for Information Assurance - 2005-present.
- ECE Undergraduate Study Chair, 2005-2010.
- NU Academic Research Computing Users Group Chair, 2006-present.
- ECE Graduate Admissions Chair, 1995-2000.
- ECE Undergraduate Study Committee Member, 1999-present.
- College of Engineering Computer Committee, 1994-2000, 2002-2003.
- ECE Faculty Search Committee Chair - 1994-1998.
- ECE Faculty Search Committee Member - 1998-2000, 2005, 2009.
- ECE Tenure and Promotion Committee - 1999-2000, 2002-2006, 2009(chair).

#### **Courses Taught**

- Computer Architecture (both undergraduate and graduate)
- Parallel Computing (undergraduate)
- Computer Security (graduate)

- Software Engineering (both undergraduate and graduate)
- Profiling and Instrumentation (graduate)
- VLSI Design (undergraduate)
- Digital Design (undergraduate)
- Introduction to Programming (undergraduate)
- Engineering Programming Models (undergraduate)

#### **Present Ph.D. Students**

- Emmanuel Arzuaga, Malak Alshawabkeh, Fatemeh Azmandian, Zhongliang Chen, Benjamin Cordes, Rodrigo Dominguez, Navid Farazmand, Xinagyu Li, Amer Malki, Jenny Mankin, Perhaad Mistry, Dana Schaa, Enqiang Sun, Yash Ukidave, Dong Ye, Ayse Yilmazer, Esra Yolacan

#### **Present MS Students**

- Matthew Sellitto, Kristy Casella, Allan Lee