

In-Place Averaged Switch Models That Include Commutation Dynamics

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Abstract—This paper presents general averaged models for switches in dc-dc converters that incorporate the dominant effects of switch commutation and delays. The newly proposed circuit-averaged switch models are modifications of conventional models and are suitable for simulation environments such as SPICE, SABER, or MATLAB. Specific details are given for switches that display linear commutation.

I. INTRODUCTION

The method of state space averaging, originally proposed by Middlebrook and Cuk [1], has long been used in the analysis for dc-dc converters. For PWM dc-dc converters the three most popular approaches of averaging are known as 1) the state space averaging method [1,2], 2) the circuit averaging method [2], and 3) the injected-absorbed-current method [3]. The recent work of Bass *et al.* [4,5,6] has provided rigorous mathematical justification for the widely used averaging methods in dc-dc converters and has slightly modified the methods using KBM averaging to include parasitic effects and dependence on the switching frequency [6].

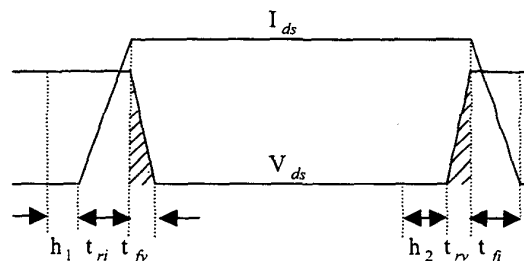
Although many improvements have been made in averaging methods to make them more accurate, it has been noted [7] that there still remain shortcomings. Specifically, with the exception of the recent work of Allard *et al.* [7] and Erickson [8,9], averaging methods assume ideal switches, i.e., the switches are either open or closed and have no delay between the driving control signal and the duty ratio of the switch. Actually there are commutation transients in the switches due to internal capacitance and resistance. Therefore, the implied assumption when using averaging methods is that switch commutation transients and delays have little influence on the dynamic input/output behavior of the dc-dc converter. However, as the switching frequency of dc-dc converters increases, commutation effects and delays do, in fact, affect the averaged dynamic performance as well as power efficiency [7].

The purpose of this paper is to present simple and general averaged models for switches that incorporate the dominant effects of linearly approximated switch commutation. The paper presents new in-place circuit averaging methods that are modifications of conventional in-place averaged models, and are suitable for simulation environments such as SPICE, SABER or MATLAB. The new methods characterize the

effects of commutation on large signal transients, small signal transients and steady states.

Averaged models specifically for switches that display linear commutation approximations are developed. Section II presents the new switch models that include commutation dynamics. The Appendix gives a detailed derivation of the commutation intervals in the models. Section III presents an example and Section IV gives conclusions. Overall, the proposed averaged models are more accurate approximations of the switching circuit, but they are more complicated than conventional averaged models.

II. AVERAGED SWITCH MODELS THAT INCLUDE COMMUTATION DYNAMICS



h_1, h_2 : V_{gs} charge/discharge delays

t_{rx}, t_{fx} : rising/falling time for x waveform

Figure 1. Switching Waveforms of Switch Current and Voltage

The new models are based on physical understanding of the switching behavior of MOSFETs that are generally utilized in PWM dc-dc converters (Fig. 1). In continuous conduction mode the proposed modeling method makes a connection between the datasheet of a real MOSFET component and its commutation-included model. By checking the datasheet and using certain component parameters, such as C_{iss} , C_{rss} and V_{th} , the commutation intervals (including the charge and discharge delay between the gate voltage (V_g) and the gate-source voltage (V_{gs}), the rising/falling time of

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current through/voltage across the switch, etc.) can be parameterized.

For example, from $0 \sim h_1$, the switch remains off. V_{gs} charges up with a time constant $C_{iss} R_g$ from 0 to V_g . At $t = h_1$, V_{gs} equals V_{th} . Then h_1 can be calculated. Other commutation intervals are derived in a similar way in the Appendix. A summary of the derived commutation intervals is given in Table 1.

A) A LOOK-BACK AT CONVENTIONAL AVERAGED SWITCH MODELS

In most canonical averaging methods for DC-DC converters [1,2], instantaneous switching is assumed. Switches are idealized as voltage-control switches, with only 'on' and 'off' states. When the switch is in 'on' state, it fully conducts. When it is 'off', it behaves like an open circuit. In many cases, ESR and other parasitics in the switching circuit are not taken into account.

Figure 2 illustrates the ideal conventional model for averaging a switch cell in a dc-dc converter. In Fig. 2(b) instantaneous commutation is assumed and the voltage across the transistor is assumed to change from high to low discontinuously at $t = \text{mod}(T)$ and from low to high at $t = dT \text{ mod}(T)$. Likewise, the current through the switch also changes instantaneously. The equivalent average circuit for the switch cell is shown in Fig. 2(c). Here $\langle x \rangle$ represents the average value of variable $x(t)$. The duty ratio d corresponds to a value between 0 and 1.

B) NEW AVERAGED SWITCH CELLS

In the proposed method, there are three different types of duty ratios. First, there is the Ideal Duty Ratio that represents the duty ratio of an instantaneous PWM chip. Next, there is

the Voltage Duty Ratio, labeled as d_V , which includes the non-linear commutation effects on the averaged voltage across the switch. Finally there is the Current Duty Ratio, given as d_I , which includes the averaged non-linear current losses through the switch. When commutation effects become prevalent, $d_{ideal} \neq d_V \neq d_I$. Furthermore d_V and d_I depend non-linearly on the inductor current and the output voltage of the converter. Hence these commutations will affect dynamic transients. The representations of equivalent duty ratios d_V and d_I in terms of the commutation intervals are obtained as:

$$d_V = d_{ideal} - \frac{h_1 + t_{ri} - h_2}{T_s}$$

$$d_I = d_{ideal} + \frac{1}{T_s} (h_2 + t_{rv} + \frac{t_{fi} - t_{ri}}{2} - h_1).$$

For simplicity we also define

$$d_q = d_V - t_{ri} / T_s.$$

Now based on lengthy area calculations of Fig. 1:

$$\langle i_{ds} \rangle_{T_s} \equiv d_I I_L$$

$$\langle V_{ds} \rangle_{T_s} \equiv V_{ds_off} (1 - d_V) + V_{ds_on} d_q.$$

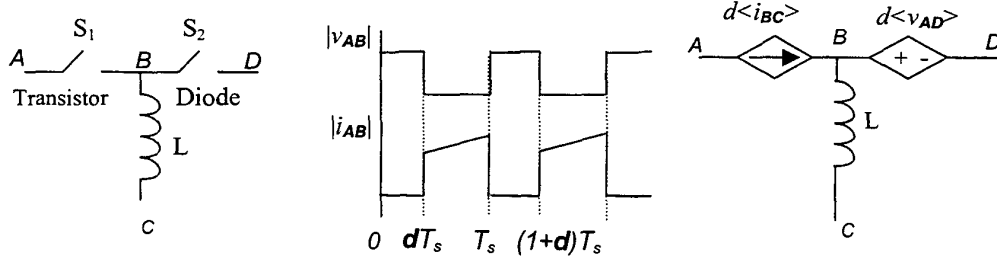
The averaged switch cell can, therefore, be given as in Fig. 3. Derivation of the averaged cell is best justified through example.

III. EXAMPLE: BOOST CONVERTER

The switching circuit of a boost converter is shown in Fig. 4. The equivalent averaged circuit is given in Fig. 5 with the values of VCVS (Voltage-Control-Voltage-Source) and CCCS (Current-Control-Current-Source) in Fig. 5.

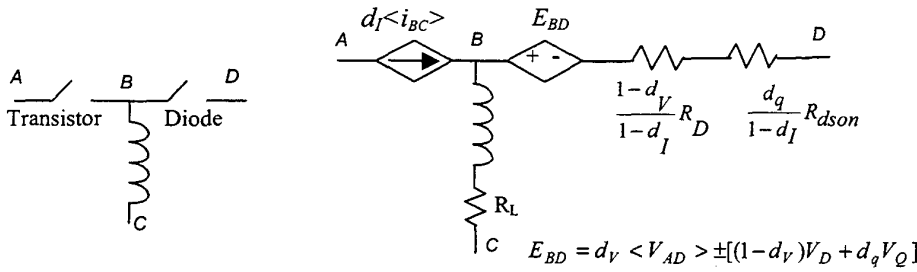
PARAMETERS TO OBTAIN FROM DATA SHEET	COMMUTATION INTERVALS	
Capacitance: C_{iss}, C_{rss}	h_1 : V_{gs} charge delay	$C_{iss} R_g \ln(V_g / (V_g - V_{th}))$
Threshold Voltage: V_{th}	h_2 : V_{gs} discharge delay	$C_{iss} R_g \ln(V_g / (V_{th} + I_L / g_{fs}))$
Forward Transconductance: g_{fs}	t_{ri} : rising time of I_{ds}	$C_{iss} R_g \ln((V_g - V_{th}) / (V_g - V_{th} - I_L / g_{fs}))$
Drain-Source On-State Resistance: R_{dson}	t_{fi} : falling time of I_{ds}	$C_{iss} R_g \ln(1 + I_L / (g_{fs} V_{th}))$
Note: V_{dd} : Supply Voltage for Drain in PWM dc-dc converters; V_g : Supply Voltage for Gate; R_g : Norton equivalent Resistance of V_g ; I_L : Constant Current Source (Inductor Current in PWM dc-dc converters)	t_{rv} : rising time of V_{ds}	$C_{rss} R_g (V_{dd} - I_L R_{dson}) / (V_g - V_{th} - I_L / g_{fs})$
	t_{fv} : falling time of V_{ds} (same value as t_{rv})	$C_{rss} R_g (V_{dd} - I_L R_{dson}) / (V_g - V_{th} - I_L / g_{fs})$

Table 1. Commutation Intervals Derived in the Appendix



(a) PWM Switching Cell (b) Ideal Switching Waveforms (c) Ideal Equivalent Switching Cell

Figure 2. Conventional Averaged Switching Cell for Buck and Boost Derived DC-DC Converters



(a) Switching Cell (b) Equivalent Switching Cell

Figure 3. Proposed Averaged Switching Cell for Buck and Boost Derived DC-DC Converters

We justify the equivalent averaged circuit by detailed derivation. First, the differential equations of the switching circuit in terms of i_{s1} and v_{s1} are:

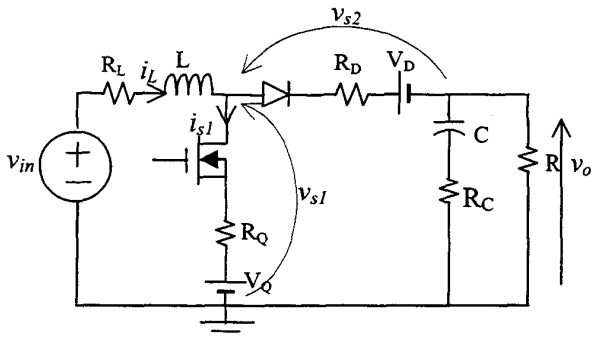


Figure 4. Boost Converter

$$\frac{di_L}{dt} = (-R_L \cdot i_L - v_{s1} + v_{in}) \frac{1}{L}$$

$$\frac{dv_c}{dt} = (i_L - i_{s1} - \frac{v_o}{R}) \frac{1}{C}$$

$$\text{where } v_o = (i_L - i_{s1}) \cdot (R // R_c) + v_c \left(\frac{R}{R + R_c} \right)$$

Then the averaged differential equations are derived by averaging the time-varying terms in the differential equations:

$$\frac{d \langle i_L \rangle}{dt} = (-R_L \cdot \langle i_L \rangle - \langle v_{s1} \rangle + v_{in}) \frac{1}{L}$$

$$\frac{d \langle v_c \rangle}{dt} = (\langle i_L \rangle - \langle i_{s1} \rangle - \frac{\langle v_o \rangle}{R}) \frac{1}{C}$$

where

$$\langle v_o \rangle = (\langle i_L \rangle - \langle i_{s1} \rangle) \cdot (R // R_c) + \langle v_c \rangle \left(\frac{R}{R + R_c} \right)$$

From previous results, d_I , d_V and d_q can be obtained, and $\langle i_{s1} \rangle$ and $\langle v_{s1} \rangle$ can be calculated as:

$$\langle v_{s1} \rangle = \langle V_{ds_off} \rangle (1 - d_V) + \langle V_{ds_on} \rangle d_q$$

$$\langle i_{s1} \rangle = d_I \langle i_L \rangle$$

$$\text{where } V_{ds_off} = v_o + V_D + i_L R_D, V_{ds_on} = V_Q + i_L R_Q$$

To simplify the equivalent circuit, $\langle v_{s1} \rangle$ can be rewritten as:

$$\langle v_{s1} \rangle = [\langle v_o \rangle + V_D] \cdot (1 - d_V) + d_q V_Q + (1 - d_V) \langle i_L \rangle R_D$$

$$+ d_q \langle i_L \rangle R_Q$$

$$\text{Since } \langle v_o \rangle = \langle v_{s1} \rangle - \langle v_{s2} \rangle, \langle i_L \rangle = \langle i_{s1} \rangle + \langle i_{s2} \rangle,$$

$$\langle i_{s1} \rangle = d_I \langle i_L \rangle, \langle i_{s2} \rangle = (1 - d_I) \langle i_L \rangle$$

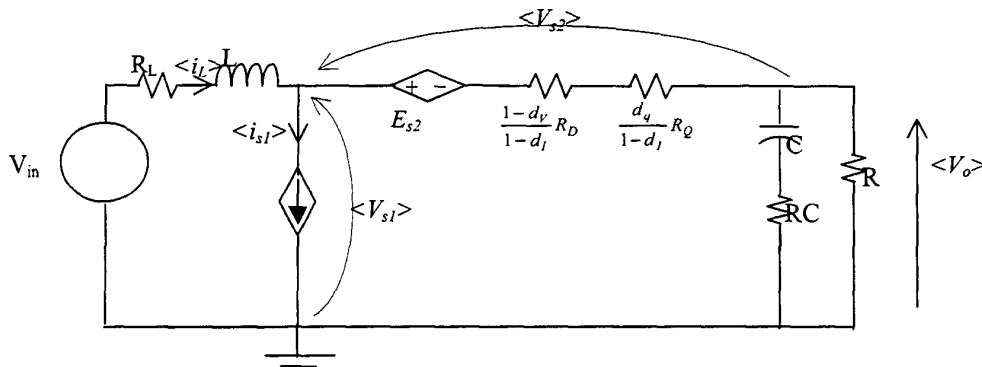


Figure 5. Equivalent Circuit for the Boost Converter

$$\begin{aligned} \langle v_{s2} \rangle &= [-d_V \langle v_o \rangle + (1-d_V)V_D + d_q V_Q] \\ &+ [(1-d_V) \langle i_L \rangle R_D + d_q \langle i_L \rangle R_Q] \\ &= [-d_V \langle v_o \rangle + (1-d_V)V_D + d_q V_Q] \\ &+ (\langle i_{s2} \rangle \frac{1-d_V}{1-d_I} R_D + \langle i_{s2} \rangle \frac{d_q}{1-d_I} R_Q) \end{aligned}$$

The last term in the round parenthesis can be represented in the averaged equivalent circuit by two resistors in series with the diode ($\langle V_{s2} \rangle$, $\langle i_{s2} \rangle$) branch. E_{s1} takes the value of the terms in the square brackets:

$$E_{s2} = -d_V \langle v_o \rangle + (1-d_V)V_D + d_q V_Q.$$

Hence, the equivalent averaged circuit in Fig. 5 is derived, since it is given by the above averaged differential equations. We remark that in a similar way, the new averaged switch cell can be justified for Buck and Buck-Boost topologies.

The averaged circuit is simulated in SPICE and compared with SPICE switching model. The simulations are performed in open loop with fixed duty ratio. The switching frequency is 400 kHz. The MOSFET used in the circuit is based on the N-channel 30-V (D-S) rated MOSFET of Si4410DY. The results of transient responses (Fig. 6) show an obvious power loss in steady state. The ideal duty ratio is given by the equation $d_{ideal} = 1 - 3.3/5 = 0.34$. On the other hand, when $d_{ideal} = 0.34$, the new averaged models predict commutation and conduction losses.

Figure 6 illustrates that the output voltage does not reach the ideal 5 V level: instead the output voltage switches between (approximately) 4.49 V and 4.40 V. The predicted averaged output voltage is given as 4.486 V. The circuit averaged models predict an averaged inductor current of 2.733 A. Figure 6 shows the accuracy of this prediction. The actual averaged switching value is (approximately) 2.70 A. The averaged circuit accurately has predicted the power efficiency of the converter to be 91%.

IV. CONCLUSIONS

This paper shows that it is possible to include commutation and conduction losses in averaged switch cells when performing in-place circuit averaging. Parameters can be read from a manufacturer's datasheet for switches and used in SPICE code assuming linear commutation. The methodology for applying the technique is the same as when applying conventional in-place circuit averaging. However, with the proposed method, the duty ratios depend non-linearly on commutation times.

Future work will focus on applying the method for SEPIC, Cuk, and isolated converters. Due to lack of space, these results could not be included but have already been derived.

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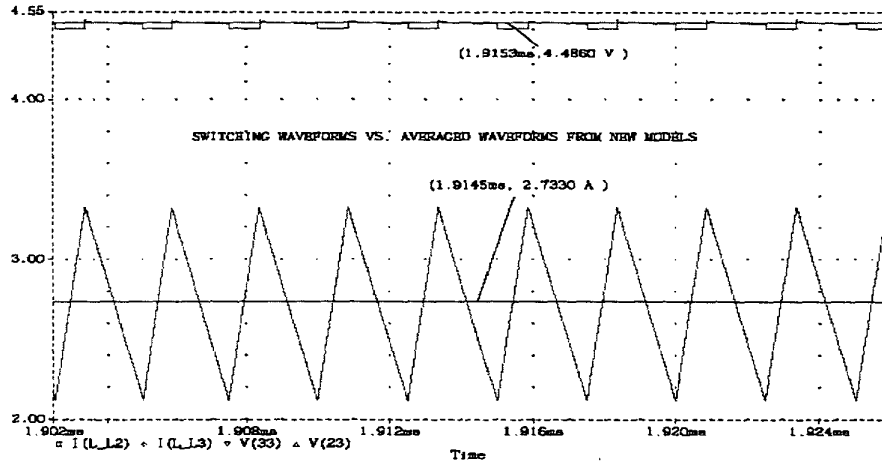


Figure 6. Comparison of Switching and Averaged Waveforms of Inductor Current and Output Voltage

APPENDIX - Derivation of Commutation Intervals (Table 1)

Assume the ripple change in inductor current can be considered small compared to its average value. Then the one-cycle variance of the inductor current can be neglected. Also ripples on capacitor voltages can be neglected. Finally, the gate drive of the MOSFET switch also affects the switching dynamics of the MOSFET switch. In our case, this influence is not considered yet. We assume that the gate drive provides the switch with perfect square-wave voltage supply.

Thus a typical circuit [9] (as shown in Fig. A.1) can be used to analyze the switching behavior of a MOSFET switch when the below conditions are satisfied:

1. The switching transient dynamics are substantially faster than the switching frequency;
2. When the transistor is fully conducting, the current going through it can be assumed constant;
3. When the transistor is off, the voltage across it can be assumed constant;
4. The gate drive signal is a series of square pulses.

After making the above assumptions, we can analyze the switching behavior of the MOSFET switch by modeling it with appropriate parasitic capacitors (C_{gd} , C_{ds} and C_{gs} , or in other forms, C_{iss} , C_{rss} and C_{oss} , $C_{iss}=C_{gd}+C_{ds}$; $C_{rss}=C_{gd}$; $C_{oss}=C_{ds}+C_{gd}$). Since the parasitic capacitors are non-linear voltage-dependant, the MOSFET model based on a set of

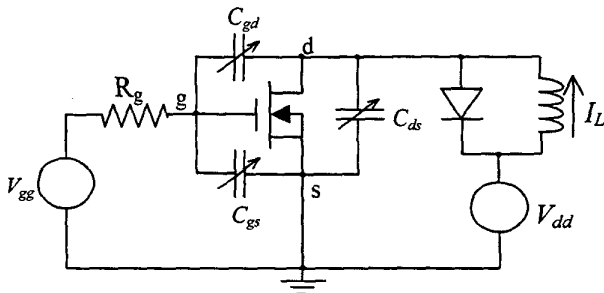


Figure A.1 Equivalent Circuit for Physical Explanation of Switching Dynamics

constant parasitic capacitors is by no means precise. Also, the effects that the diode (or synchronous rectifier) in the circuit may have on the MOSFET switch are not taken into account in our modeling. As we already know, the diode reverse recovery can cause a spike in the current, as well as affect the switching dynamics of the MOSFET switch. Snubber circuits also have certain effects on switching, such as the turn-on/turn-off delays, etc.

In the typical circuit of Fig. A.1, there is an inductive load in parallel with a diode. The inductor is large enough so that I_L will be assumed constant. Referring to Fig. A.2, turn-on and turn-off transients have been divided into eight different intervals denoted as Phases I~VIII.

A. Turn-on

- (1) *Phase I*: Charging the gate-source capacitance C_{gs}

V_{gs} rises exponentially to the gate threshold voltage V_{th} and $I_{ds} = 0$. In this period, the gate drive source V_{gg} charges the input capacitance C_{iss} of the MOSFET through R_g . C_{iss} equals C_{gd} in parallel with C_{gs} . The dynamic equations become:

$$V_{gs} = V_{gg} [1 - \exp(-\frac{t}{R_g \cdot C_{iss}})]; \quad C_{iss} = C_{gd} + C_{gs}$$

The charge-up time h_1 is the turn-on delay and can be

$$\text{calculated by solving } V_{th} = V_{gg} [1 - \exp(-\frac{h_1}{R_g \cdot C_{iss}})]. \text{ So}$$

$$\text{we have } h_1 = -R_g C_{iss} \ln(1 - \frac{V_{th}}{V_{gg}}).$$

- (2) *Phase II*: Drain-source current I_{ds} rising

V_{gs} continues rising exponentially. I_{ds} starts to increase from 0A until it reaches I_L , according to:

$$I_{ds} = g_{fs} \{V_{gg} [1 - \exp(-\frac{t}{R_g \cdot C_{iss}})] - V_{th}\}.$$

At time $t = h_1 + t_{ri}$, we have $I_{ds}(t = h_1 + t_{ri}) = I_L$, and therefore

$$t_{ri} = R_g C_{iss} \ln \left(1 - \frac{V_{th}}{V_{gg}} - \frac{I_L}{g_{fs} V_{gg}} \right)^{-1} - h_1.$$

(3) *Phase III*: Falling of V_{ds} from V_{ds_off} to V_{ds_on}
 $I_{ds} = I_L$, V_{gs} remains unchanged at the level of $V_{th} + \frac{I_L}{g_{fs}}$ with a constant load current. V_{ds} falls to V_{ds_on}

with a constant slope:

$$\frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}}$$

where $I_g = \frac{V_{gg} - V_{gs}}{R_g}$. The voltage fall-time is:

$$t_{fv} = \frac{V_{dd} - V_{ds_on}}{V_{gg} - V_{th} - I_L / g_{fs}} C_{gd} R_g.$$

(4) *Phase IV*: V_{gs} charging up to V_{gg}
 V_{ds} continues to rise until it reaches V_{gg} .

B. Turn-off

(5) *Phase V*: Discharging of C_{iss} before current rising
 V_{gs} decreases exponentially from V_{gg} to $V_{th} + \frac{I_L}{g_{fs}}$.

After h_2 time, V_{gs} reaches $V_{th} + \frac{I_L}{g_{fs}}$. Therefore:

$$V_{gs} = V_{gg} \exp\left(-\frac{t}{R_g \cdot C_{iss}}\right) = V_{th} + \frac{I_L}{g_{fs}}$$

The turn-off delay h_2 can be calculated as:

$$h_2 = R_g C_{iss} \ln \left(\frac{V_{th} + I_L / g_{fs}}{V_{gg}} \right)^{-1}.$$

Phase VI: Rising of V_{ds}

V_{ds} rises to V_{dd} , while I_{ds} remains constant. V_{gs} maintains the lowest possible level that enables current to maintain at I_L :

$$I_{ds} = I_L; \quad V_{gs} = V_{th} + \frac{I_L}{g_{fs}}$$

I_g is needed to discharge C_{gd} at a constant rate:

$$I_g = \frac{V_{gg} - V_{gs}}{R_g} = \frac{V_{gg} - (V_{th} + I_L / g_{fs})}{R_g}$$

$$\frac{dV_{ds}}{dt} = \frac{I_g}{C_{gd}} \rightarrow V_{ds_on} + t_{rv} I_g / C_{gd} = V_{dd} \rightarrow$$

$$t_{rv} = \frac{V_{dd} - V_{ds_on}}{I_g} C_{gd} = \frac{(V_{dd} - V_{ds_on}) R_g \cdot C_{gd}}{V_{gg} - (V_{th} + I_L / g_{fs})}$$

(6) *Phase VII*: Falling of I_{ds}

I_{ds} drops from I_L to 0, and the load current is diverted to the parallel diode. First, V_{gs} falls exponentially from $V_{th} + \frac{I_L}{g_{fs}}$ to the gate threshold voltage V_{th} .

$$V_{gs} = (V_{th} + \frac{I_L}{g_{fs}}) \exp\left(-\frac{t}{R_g \cdot C_{iss}}\right)$$

$$I_{ds} = g_{fs} (V_{gs} - V_{th}) = g_{fs} \left((V_{th} + \frac{I_L}{g_{fs}}) \exp\left(-\frac{t}{R_g \cdot C_{iss}}\right) - V_{th} \right)$$

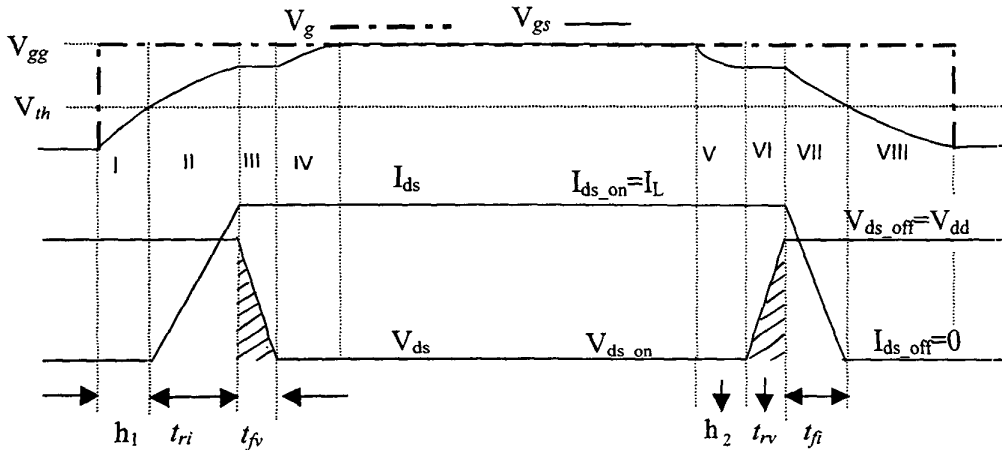
$$I_{ds} = 0 \rightarrow t_{fi} = R_g C_{iss} \ln \left(1 + \frac{I_L}{g_{fs} \cdot V_{th}} \right)$$

Thus the voltage rise-time is obtained.

(7) *Phase VIII*: Total discharging of C_{iss}

V_{gs} falls exponentially from V_{th} to 0, according to:

$$V_{gs} = V_{th} \exp\left(-\frac{t}{R_g \cdot C_{iss}}\right).$$



h_1, h_2 : V_{gs} charge/discharge delays

t_{rx}, t_{fx} : rising/falling time for x waveform

Figure A.2 Switching Waveforms for Analysis