# A Simple Design for Paralleling Current-Mode Controlled DC-DC Converters

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***Abstract*- This paper proposes a new current sharing method. It utilizes the inner current loops of current mode controlled converters to achieve the current sharing, and decouples control loops from the voltage regulation and current-sharing regulation instead of adding control loops as in traditional master-slave methods. Therefore, the performance is guaranteed in both the large and small signal sense. This is verified by experimental results.**

## I. INTRODUCTION

Paralleled power systems have seen widespread applications due to their benefits in redundancy, thermal management, efficiency and modularity. Typically, parallel power systems are designed so that the stresses among the paralleled DC-DC converters are balanced. This is commonly achieved by current-sharing control.

Among the many proposed schemes [1-6], the master-slave method is widely utilized [3-6] because of its good voltage regulation, modularity and simplicity. In this approach, the paralleled converters share information on output current through a current sharing bus; one converter is chosen as the master converter to ensure the voltage regulation, and others, the slave converters, try to keep their output currents to be the same as the master's by regulating their voltage reference through the current-sharing control loops.

However, the parallel system with master-slave method is actually a multi-input, multi-output system. As a result, the design and analysis is more advanced [7,8]. Therefore, in system design, the bandwidth of the current-sharing control loop is kept much lower than that of the voltage control loop of the converter to guarantee the stability of the parallel system [3,7]. However, this design rule results in a slow dynamic performance of the current sharing, and ongoing research is attempting to address these problems [9,10].

On the other hand, it is widely known that the current source behavior of the inner current loops of current mode controlled (CMC) DC-DC converters can be used to obtain current sharing. For example, it is possible to make all inner current loops share one voltage loop. However, this approach has the disadvantage of losing the modularity of the parallel system. Alternatively, [4] uses the source/sink capacity imbalance of UC3843 to force all converters to share the same inner current reference. However, the UC3843's on the slaves are saturated, and therefore, so are their voltage control loops.

This paper recognizes both the limitations of master-slave methods and the inherent current source properties of CMC converters. We propose a new master-slave current sharing design using the inner current source of CMC converters. It includes two parts: loop design and saturation prevention. In the loop design procedure, all inner current references are sent to a current sharing bus, and one reference is chosen as the master. Then all inner current loops take the master value as their reference to achieve current sharing by modifying the sensed current signal. Therefore, only the voltage control loop of the master is active in voltage regulation while those in slaves are decoupled from the system. However, those voltage control loops in slaves will saturate because of different voltage references, and this implies performance degradation when the master fails. Therefore, the second part of the method is saturation prevention: to make those voltage loops have the same inner current reference as the master. Hence, the voltage loops of slaves become backups for the master voltage loop.

Specifically, the current sharing approach in this paper has the following features:

- The implementation achieves current sharing by modifying the sensed current signal.
- The current sharing bus is minimum-master bus.
- The method is implemented using off-the-shelf DC-DC converters with current mode PWM controllers, UC3843.

The implementation of the method is presented in Section II based on current mode PWM controller, UC3843. The operation of master and slave converter is shown in Section III. A small signal model is presented and analyzed in Section IV. This method is implemented using off-the-shelf DC-DC converters in Section V. Experimental results verify the proposed design. Conclusions are given in Section VI.

## II. IMPLEMENTATION DESCRIPTION

The implementation of the method is shown in Fig. 1. The DC-DC converter used is a peak current mode controlled converter with UC3843, and the amplifiers used are rail-to-rail single supply op amps. Specifically, each block has function as follows:

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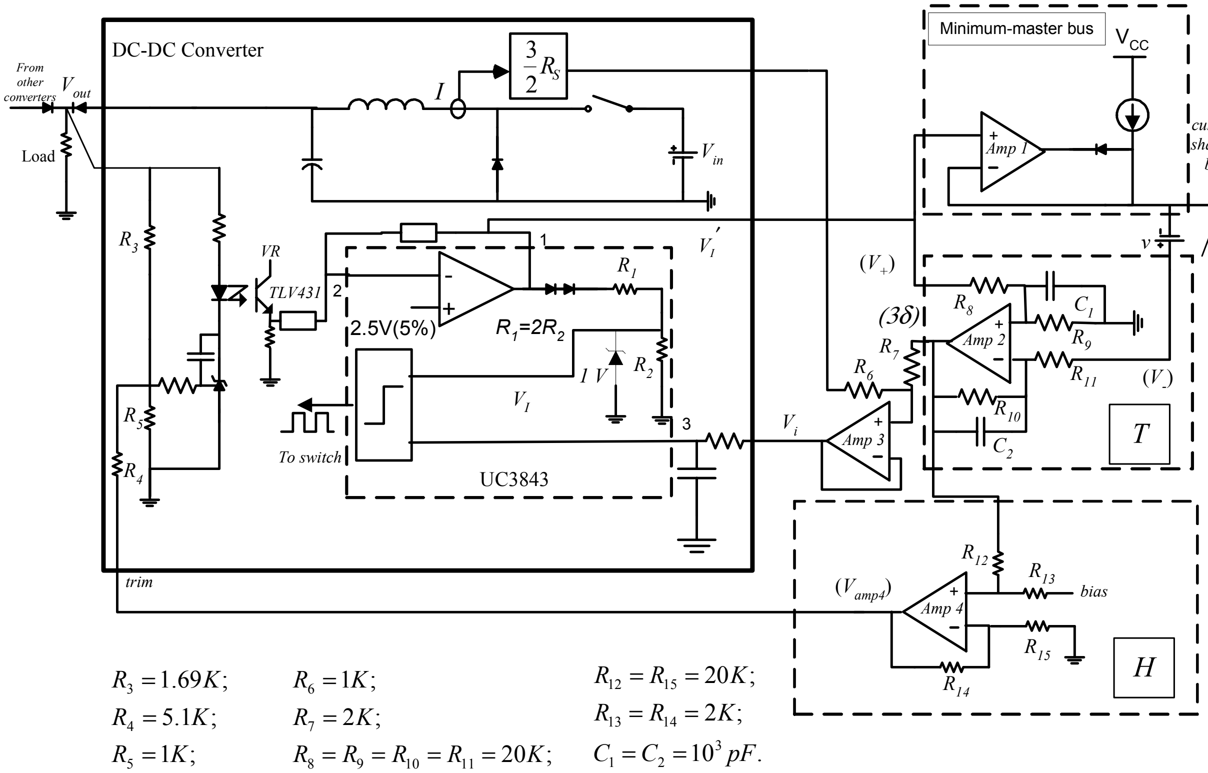


Figure 1. Simplified schematic of proposed current sharing method

### *DC-DC converter*

The solid box represents a peak current mode controlled DC-DC converter with input voltage, $V_{in}$, and load. A buck converter is shown as the power train. A barrier diode is placed between the output and the load, and remote sense is used to compensate the voltage drop on the barrier diode. $R_4$ is the voltage trim resistor. Later we will show that the knowledge to the converter is not critical to the system design.

The inductor current $I$ is sensed, and $R_S$ is the gain of the current sensing function. (Usually, it is the value of the current sensing resistor or the sample resistor at the output of the current transformer.) Originally, the output of $R_S$ is connected to $V_i$ and used as an input to UC3843, which is represented in a dashed box. $V_I$ is the inner current reference while the output of *pin 1* of UC3843, $V_I'$, is proportional to $V_I$ with the bias of the voltage drop on the two diodes [11]. Therefore, in normal operation, the output of *pin 1* can be viewed as the current reference. Specifically,

$$V_I' = 3V_I + 2V_{diode} \tag{1}$$

where $V_{diode}$ is the forward voltage drop on the diode, and the number of 3 comes from the ratio of $R_1$ and $R_2$ in Fig. 1.

However, (1) is only true in normal operation because $V_I$ is limited to 1V by the Zener diode paralleled with $R_2$.

Originally, the sensed current signal is $I \cdot R_S$. In this circuit, the current sensing gain is modified to $\frac{3}{2}R_S$ in order to maintain the current signal at $V_i$, which will be shown later.

### *Minimum-master bus*

The minimum-master bus consists of *Amp 1*, the diode at its output, the current sharing bus and the current source. Therefore, the minimum voltage to *Amp 1* will appear on the bus. In Fig. 1, the converter with the minimum current reference is the master. That is

$$V_{bus} = V_{I,master}' \tag{2}$$

where $V_{bus}$ is the voltage of the current sharing bus and $V_{I,master}'$ is $V_I'$ of the master.

The small voltage bias, given as $v$, is used to improve the noise immunity and to prevent bus competition. $v$ is connected between the current sharing bus and function block $T$ in Fig. 1. Details of the minimum-master bus can be found in [6], which also includes hot-swap circuits.

### *Function block T*

If the positive input of *Amp 2* is larger than its negative input, *Amp 2* works in the linear region. Therefore, function

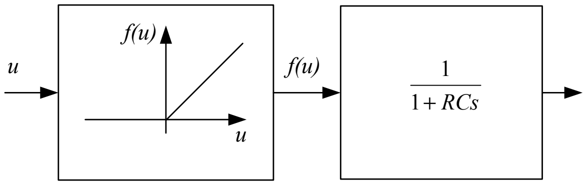


Figure 2. Function of *T*

block *T* is simply a low-pass filter. However, all amplifiers in Fig. 1 are single supply op amp, and their lowest output voltage is zero. Therefore, *T* is a nonlinear function, as shown in Fig. 2.

The function *f(u)* in Fig. 2 is a piecewise-linear function (the nonlinear part of *T* ) and can be represented as:

$$f(u)=\begin{cases} u & u>0 \\ 0 & else. \end{cases} \tag{3}$$

where $u=V_+-V_-$. $V_+$ and $V_-$ are the inputs to the positive and negative input of *Amp 2*, respectively.

On the other hand, because in Fig. 1, $R_8 \sim R_{11}$ have the same value and $C_1 = C_2$, the low-pass filter is the right block in Fig. 2 where $R=R_8$ and $C=C_1$.

Finally, the inputs to *T* are the outputs of *pin 1*, $V_I'$, of UC3843's, and (1) shows its relation with inner current reference $V_I$. Specifically, the positive input to *Amp 2* is

$$V_+ = 3V_I + 2V_{diode} \tag{4}$$

where $V_I$ is the inner current reference of the converter. From (1) and (2), the negative input to *Amp 2* is

$$\begin{aligned} V_- &= V_{bus} + v \\ &= 3V_{I,master} + 2V_{diode} + v \end{aligned} \tag{5}$$

where $V_{I,master}$ is the inner current reference of the master and $v$ is a small DC bias.

Therefore, if $V_+ > V_-$ and $v$ is ignored, at steady state,

$$\begin{aligned} Output\ \ of\ \ T &= V_+ - V_- \\ &= 3\delta - v \approx 3\delta \end{aligned} \tag{6}$$

Here, δ is defined as the difference between $V_I$ of the converter and $V_{I,master}$.

<u>*Amp 3*</u>

*Amp 3* with $R_6$ and $R_7$ is an addition function. With the values in Fig. 1, there is

$$V_i = I \cdot R_S + \delta \tag{7}$$

where $I \cdot R_S$ is the current signal in the original converter.

<u>*Function block H*</u>

Function block *H* is a proportional function. With the value of resistors in Fig. 1, there is

$$V_{amp4} = \frac{R_{14}}{R_{15}} 3\delta + bias \tag{8}$$

where *bias* is for maintaining the output voltage.

Therefore, *H* will adjust the output voltage of the converter by regulating *trim* pin based on the output of δ. It will prevent the voltage loops of the slaves from saturation, as explained later.

## III. OPERATION

### *A. Operation of the master*

When the converter is master, its output of *pin 1*, $V_I'$, appears on the current sharing bus. On the other hand, because the small voltage bias *v,* for function block *T*, its positive input will be always smaller than its negative input. Therefore, its output is always zero,

$$\delta = 0 \tag{9}$$

Then (7) for the master is,

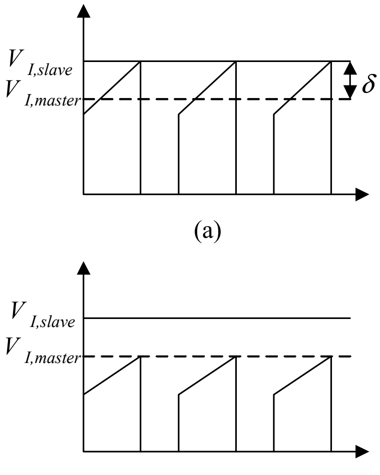
$$V_i = I \cdot R_S \tag{10}$$

Therefore, the operation of the master will be the same as the original converter.

### *B. Operation of the slave*

Fig. 3 shows how the slave works. In Fig. 3(a), the rectangular waveform train is the output current signal, $V_i$, of a slave, which is fed to the *pin 3* (*CS*) of UC3843. The solid line is the current reference of the slave, while the dashed line is that of the master. The difference between the two references is δ, see (6).

On the other hand, (7) shows that $V_i$ is the sum of the current signal of the output inductor and δ. Therefore, the true current signal of the output inductor is shown in Fig. 3(b), which has the same peak value as that of the master, and then current sharing is achieved when the inductors are the same among the converters.



(a)

(b)

Figure 3. Current signals in the slave

$V_{I,master}$ : current reference of the master;

$V_{I,slave}$ : current reference of the slave

Therefore, this method forces all inner loops to have the same output current peak value by modifying the sensed current signal. As a result, only the voltage control loop of the master converter is working effectively. However, those decoupled control loops will saturate if they are left alone, and the function block *H* is utilized to prevent this from occurring.

The output of *H,* which is connected to the *trim* pin of the converter, regulates the voltage reference of the converter to reduce $\delta$. $V_{bias}$ is a constant voltage to set the DC point of the output. Therefore, *H* prevents the voltage control loops of the slave converters from saturating. We call this control loop the minor loop. The minor loop does not participate in current-sharing control directly in normal operation. Meanwhile, if the bandwidth of the minor loop is sufficiently lower than that of the voltage control loop of the converter, the reference regulation is decoupled from the voltage regulation. That is, voltage loop bandwidth/ regulation is unaffected if *H* is properly selected.

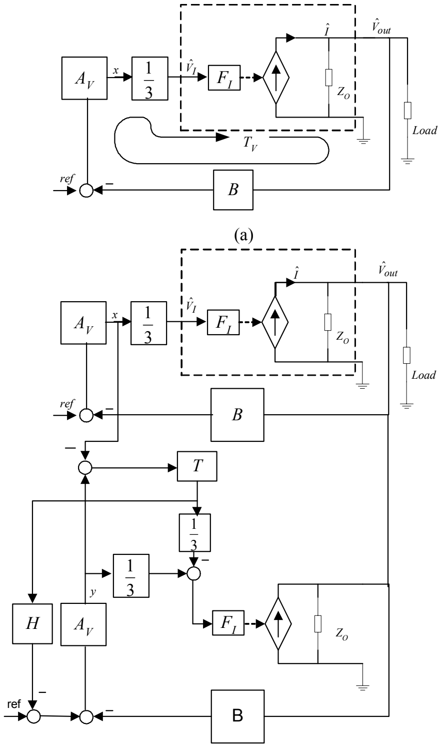
This method "removes" the voltage loops of slaves to achieve current sharing instead of adding another current-sharing loop. Therefore, there is no tradeoff between the stability and bandwidth of current sharing loop design, and the parallel system will have an excellent large signal performance.

On the other hand, because the design for saturation prevention is not directly related to the current sharing, the proposed method divides the parallel design procedure into two <u>independent</u> and easier solved problems. The first is to maintain current sharing. The second, independent, problem is to keep all control loops in the system working normally. As a result, system design becomes simple. Meanwhile, the inner current sources have higher crossover frequencies than that of the voltage loops. It implies that the parallel system will have fast voltage and current sharing dynamic response.

## IV. ANALYSIS

A DC-DC converter can be modeled as a controlled voltage source with output impedance [8]. Further, the inner loop of the current mode controlled DC-DC converter can be modeled as a current source, and then the small signal model of a current mode controlled DC-DC converter is shown in Fig. 4(a). Using the notation of [8], $B$ is the transfer function from the voltage sense point to the comparison point with *ref.* In the simplest case, $B$ is a scaling factor from a resistor network. $A_V$ is the transfer function of the voltage controller in the converter. The block 1/3 is the proportion between $V_I'$, and $V_I$.

The output of transfer function $A_V$, given as *x*, is the inner current reference, which corresponds to *pin 1* of UC3843. The dashed box represents the inner current loop and it is a voltage controlled current source. $F_I$ is the transfer function from small signal inner current reference $\hat{V}_I$ to small signal inductor current $\hat{I}$ when the current loop is closed. (For peak current mode control, the inner current reference $V_I$ in Fig. 1 is the peak value of the output current. So is *I*. Therefore, although they correspond to $\hat{V}_I$ and $\hat{I}$, respectively, there is difference between the variables.)



(a)

(b)

Figure 4. The model of (a) a current mode controlled DC-DC converter (b) proposed method

$Z_O$ is the output impedance of the inner current loop and is sometimes approximated as the impedance of the output capacitor bank. Therefore, for a single module, the transfer function of the voltage loop, $T_V$, is

$$T_V = \frac{1}{3} A_V B F_I Z \tag{11}$$

where $Z = Z_O \,//\, Load$. In most cases, the impedance of the load can be ignored compared with that of $Z_O$. That is,

$$T_V \approx \frac{1}{3} A_V B F_I Z_O \tag{12}$$

Based on the current source model, the model of the proposed method is shown in Fig. 4(b). For simplicity, only two converters are shown, and the effects of the barrier diode and impedance of the distributed lines are ignored. Because this method modifies the current signal at the comparison point with the (peak) inner current reference $V_I$, from the point of view of small signal, it can also be viewed as modifying $\hat{V}_I$. Meanwhile, this method is a master-slave method, and any module can obtain the current sharing bus and be the master module. However, when the master position is established and the system is in steady state, from the point of view of small signal, the system is the same as the dedicated master-slave system. Therefore, dedicated master-slave structure is used in system modeling. In Fig. 4(b), the upper converter is the master module, and the lower is the slave module.

Therefore, the current reference to the inner current source of the slave module is *[y-T(y-x)]/3*, and equals to *x/3* when *T=1*.

However, this model in Fig. 4 can only be directly used for small signal analysis when the operating point of $T$ is greater than zero (see Fig. 2). Then, $f(u)$ operates in the linear region, i.e., $f(u)=u$ when $u>0$. Therefore, to operate the minor loop in the linear region, there should be a (small) DC bias at the input of $T$. Then there will be steady state error on the output of *T*. On the other hand, the output of *T* is not critical to the performance of the system as far as (7) is not saturated. In order to meet the requirement, *H* can simply be a small gain. In fact, if *H* is a sufficiently small gain, the resulted minor loop will have both low DC gain and low bandwidth, and it will be decoupled from the voltage control loop. That is, *H* can be ignored in subsequent small signal analysis.

Further, assume $T \approx 1$. Therefore, the outer voltage loop gain of the master is

$$T_{V,master} \approx \frac{1}{3} A_V B F_I N \frac{Z}{N} = T_V \tag{13}$$

where *N* is the number of paralleled DC-DC converters. The outer voltage loop gain of the slave is

$$T_{V,slave} \approx 0 \tag{14}$$

Therefore, in this ideal case, the voltage control loops of slaves are decoupled from voltage control, and only the master participates in the voltage regulation by adjusting its inner current reference. In fact, this resulting system is similar to a multi-phase converter, which has only one voltage control loop [12,13].

However, in real applications, it is desired that the noise on the current sharing bus be filtered out, and *T* is usually designed as a low-pass filter in the linear region. For example, capacitors $C_1$ and $C_2$ are added to behave as a low-pass filter in Fig. 1. As a result, the performance of the system will deviate from the ideal case. However, the experimental results will show that the designed system still has good dynamic performance when the assumption of $T \approx 1$ holds up to the crossover frequency of the outer voltage loop.

## V. EXPERIMENTAL RESULTS

In order to evaluate the performance of the proposed method, a parallel system with two DC-DC converters is built. The DC-DC converters are commercially available 36~72V/3.3V converters. They are peak current mode controlled forward converters using the UC3843 each with output current rating of 15A. The converters are isolated. However, for simplicity, the grounds of the primary side and the secondary side are connected in the built system. Meanwhile, the *trim* pin has been intentionally regulated to have a severe current imbalance if the converters are directly paralleled.

The bandwidth of the outer voltage control loop of each converter is around 7 KHz. Therefore, the capacitors $C_1$ and $C_2$ are selected as $1000pF$ so that the –3 dB frequency in Fig. 2 is higher than 7KHz.

On the other hand, in Fig. 1,

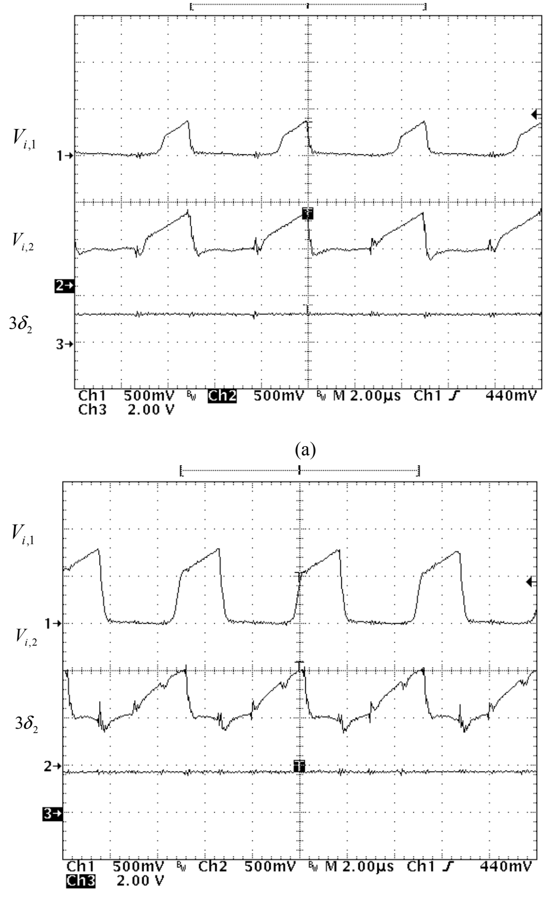
$$H \approx \frac{R_{14}}{R_{15}} \frac{R_3}{R_4} = 0.033 \tag{15}$$

which is sufficiently small for the design.

### Two-step design

In order to show that this method consists of two relatively independent tasks, first *H* is disconnected from the system. The experimental results are shown in Fig. 5.

In Fig. 5(a), the load is 10 A. The output current of Module 1 is 4.9A, and that of Module 2 is 5.1A. $V_{i,2}$ is the current signal (see Fig. 1) of Module 2. It has a DC bias, which equals to 1/3 of the output of its *Amp 2*, $3\delta_2$. It shows that current sharing is achieved by modifying the current signal, as explained in Fig. 3.



(a)

(b)

Figure 5. Measured waveform

(a) Output current: total, 10A; Module 1, 4.9A; Module 2, 5.1A

(b) Output current: total, 22A; Module 1, 14.5A; Module 2, 7.5A

Channel 1: current signal of Module 1, $V_{i,1}$;

Channel 2: current signal of Module 2, $V_{i,2}$;

Channel 3: output of *Amp 2* of Module 2, $3\delta_2$

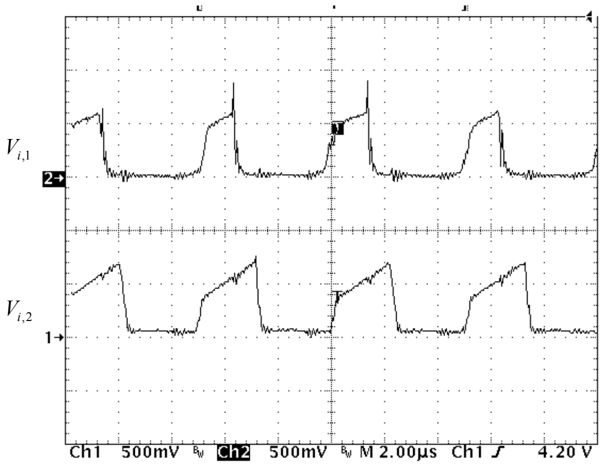


Figure 6. Measured waveform

Output current: total output 22A;

Module 1,10.7A(master); Module 2, 11.3A (slave)

Channel 2: current signal of Module 1, $V_{i,1}$;

Channel 1: current signal of Module 2, $V_{i,2}$;

However, without *H*, the voltage control loop of the slave will try to regulate the inner current reference to meet its own voltage reference. Therefore, at high load, the DC bias will become so high that its current reference $V_I$ will be locked at 1 V because of the Zener diode (see Fig. 1).

Fig. 5(b) shows the voltage limit. In this case, the load is 22 A. The output current of Module 1 is 14.5 A, and that of Module 2 is 7.5 A. The peak value of current signal of Module 2 is locked at $1V$. Meanwhile, its DC bias equals to 1/3 of the output of its *Amp 2*, $3\delta_2$.

In this case, the current sharing is lost due to the Zener diode in UC3843. Therefore, specifically in this application, minor loop is necessary not only to prevent voltage control loops of slaves from saturating but also to guarantee the current sharing at high load.

Fig. 6 shows the waveform after *H* is connected. The load current is still 22 A. The output current of Module 1, the master, is 10.7 A, and that of Module 2, the slave, is 11.3 A. It shows that the DC bias in Fig. 6 is reduced to around 50 *mV* due to the regulation of the minor loop, and both modules are working normally. Meanwhile, the DC bias is the result of low gain of *H*.

### Large signal performance

In order to test its large signal performance, a load stepping from 0 to 20A is applied, as shown in Fig. 7. The time scale is 50 $\mu s/div$. Therefore, the dynamic response of the current sharing is very fast for a parallel system: less than 150 $\mu s$ for this experiment. For comparison, in the benchmark circuit we built with UC3907, the current sharing setting time is more than 2 *ms*, which is more than ten times slower.

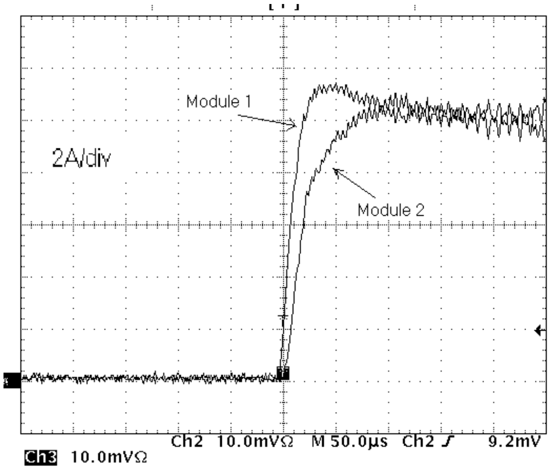


Figure 7. Step response (0-20A) of the output current

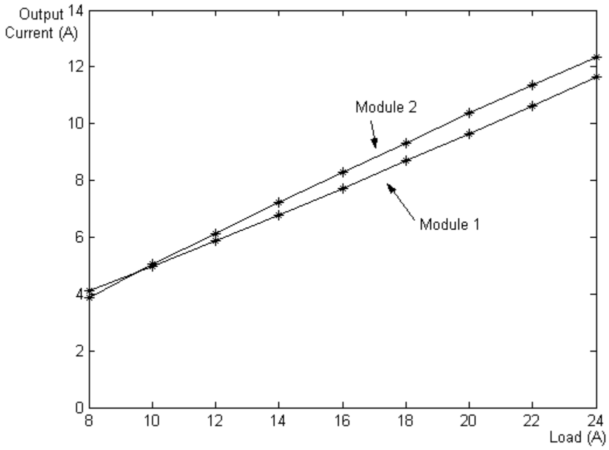


Figure 8. Steady state current sharing for different loads

### Steady state current sharing

Fig. 8 shows the current sharing at steady states. This method obtains current sharing by equalizing the reference to the inner current sources of converters. For the peak current mode control, the parameter tolerance, such as the inductance difference of the output filter, will result in current sharing error [14]. However, such error is normally acceptable from the point view of system design.

Finally, the analysis above shows that only the current sensing gain $R_S$, voltage feedback resistor network, the trim resistor of the converter and the loop gain are needed for system design. Therefore, this method is simple and can be easily used by system designers.

## VI. CONCLUSIONS

This paper proposes a new current sharing method. The method utilizes the inner current source properties of CMC DC-DC converters to achieve the current sharing. Meanwhile, the modularity of the converter is maintained, and the control loops within all DC-DC converter work normally. The system design is simple because the method decouples control loops from the voltage regulation and current-sharing regulation, instead of adding additional control loops as in the traditional methods. As a result, the performance is guaranteed in both the large and small signal sense. This is supported by experimental results.

Finally, this method uses minimum-master bus in order to incorporate the structure of UC3843. In fact, maximum-master bus can also be implemented with the same methodology. Meanwhile, in the proposed method, the control loop and the inner current source can work separately. That is, even when the power train of the master converter fails, its control loop can still be active. It implies that the redundancy of the parallel system is improved.

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