

# Control Loop Design For Two-stage Dc-Dc Converters With Low Voltage/High Current Output

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**ABSTRACTS**— This paper presents a general analysis framework for control loop design of two-stage converters. The results yield a thorough explanation of various loop design approaches. A three-loop method to extend the system bandwidth is proposed. The new control design algorithm is applied to a 48V/3.3V two-stage converter. Experiments verify the effectiveness of the control loop design approach.

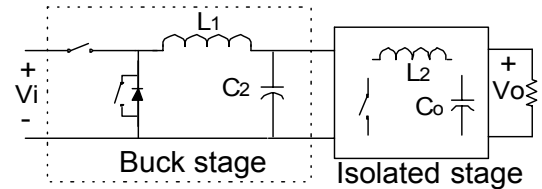


Fig. 1 Two-stage dc-dc converter

## I. INTRODUCTION

Two-stage dc-dc converter topologies have recently begun to receive interest in high input voltage, low voltage/high current output dc-dc conversion [1-4]. In general, the two-stage topologies for these applications have a buck converter as the first stage, which regulates output voltage. The second converter is an isolated converter, which operates with 50% duty cycle like a “DC transformer” to step down the voltage, as Fig. 1 shows. The second stage converter can be either a forward, push-pull, half-bridge or full-bridge converter, as shown in Fig. 2.

These topologies have several benefits: Secondary synchronous rectification (SR) can be optimized. That is, since transformer secondary voltage is minimized, SRs with low  $R_{ds(on)}$  can be used to improve the efficiency [1-4]. Also, the efficiency of the isolated converter can be improved with use of low  $R_{ds(on)}$  transformer switches since transformer primary voltage is reduced and regulated as constant. Furthermore, with transformer winding voltage, a simple and high efficiency self-driven SR can also be implemented [1-4]. Although the buck stage adds in extra losses, the overall efficiency could still be higher than its single-stage counterpart [1]. Additionally, the main inductor  $L_1$  on high voltage side has less ripple current and associated ac losses. So it is more feasible to design a small  $L_1$  to carry a bi-directional current, allowing ZVS for buck switches to reduce the switching losses. Also, housekeeping power supply can be taken directly from the transformer since transformer voltage is regulated.

However, two-stage converters have associated disadvantages too. Besides the extra cost, space, and losses brought by the additional switches, control design becomes more difficult. Unlike the cascaded converters, where the control loops are implemented in each converter separately, a

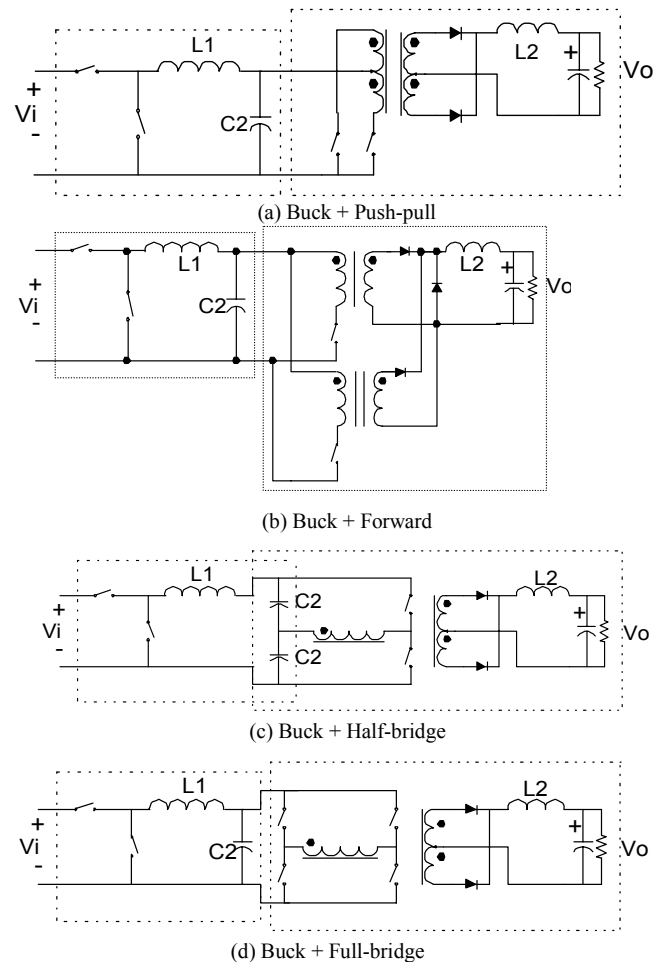


Fig. 2 Various two-stage topologies for low voltage and high current output applications

two-stage converter attempts to regulate voltage with one PWM chip. The two stages are viewed as one system. Therefore, the pole-characteristic (Appendix) of a two-stage

converter is ideally modeled as a fourth order system with two system resonances. As a result, the overall system bandwidth is usually kept conservatively low to assure no interaction with the resonant poles. Such a design significantly limits the transient response and degrades the dynamic regulation. In fact, there has been little published on high performance control loop design for two-stage converters to date. [2] discusses its open-loop small signal modeling, but it does not address closed-loop control algorithm. Several open issues have yet to be addressed. For example, how many ways are available to implement the control loops? What are the criteria for each control loop design? When should multi-loop control be used? How should each loop be implemented? The control design is still a major problem that impedes the application of two-stage topologies in fast transient dc-dc conversions.

This paper investigates general control loop design strategies for two-stage converters and begins to answer the above questions. The small signal average model of two-stage topology is first analyzed in Section II. Then,

- Various control schemes for two-stage converters are examined and comparisons of their advantages and disadvantages are given in Section III. Such a discussion has been lacking in the literature and should be useful to the practicing engineer. Clear and simple guidance on how to design control loops for two-stage converters is presented.

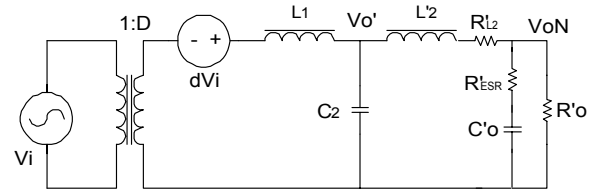
- In Section IV a simple two-loop design algorithm is presented. Its benefits and bandwidth limitations (below the first resonance frequency) are discussed.

- In Section IV, a new, general three-loop design algorithm is proposed to facilitate the loop design of two-stage converters and to achieve a system bandwidth beyond the first resonant frequency. This high bandwidth had not yet been previously reported with the traditional control loop design. The algorithm is applicable to most two-stage topologies.

Experimental verifications of the proposed controllers are presented in Section V. Conclusions are given in Section VI. The Appendix presents necessary small signal transfer functions for reference.

## II. MODELING AND ANALYSIS OF TWO-STAGE TOPOLOGIES

Since two-stage converters regulate output of the buck stage in PWM and convert a constant DC voltage to the output through an equivalent “DC transformer,” they can usually be described with the same small signal model as Fig. 2 shows.  $R'_{ESR}$  is the equivalent series resistance of the output capacitor reflected in the primary side.  $R'_{L2}$  is the total series resistance of the secondary side windings and output inductor reflected in the primary side. Since  $R'_{L2}$  has a strong damping effect in small signal behavior of the topology [2], it is neglected in the following analysis for the worst case. Because the transformer operates with 50% duty cycle, the magnetizing inductance does not affect the small signal behavior theoretically [5] and is also neglected.



$$(L'_2 = L_2 N^2, C'_o = C_o / N^2, R'_o = R_o N^2, N = V'_o / V_o)$$

Fig. 2 Small signal equivalent model of two-stage topologies

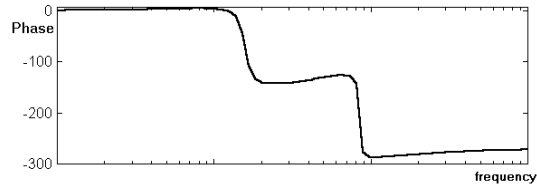
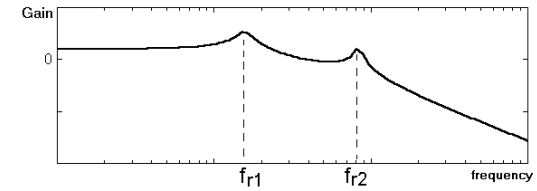


Fig. 4 Open-loop transfer functions  $V'_o/d$

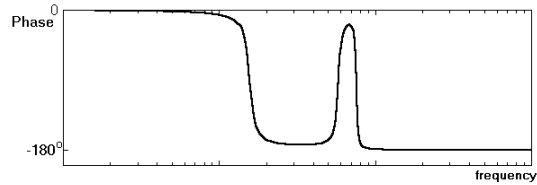
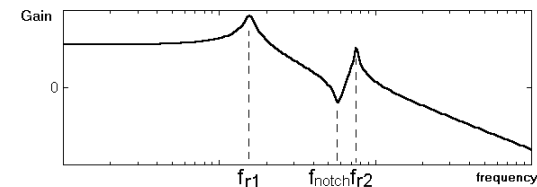


Fig. 5 Open-loop transfer functions  $V'_o{}^2/d$

The resulting control-to-output transfer function (Appendix) exhibits a fourth order system with two pairs of conjugate poles, which result in two system resonances. A zero caused by  $R'_{ESR}$  is assumed to be located between the two resonant frequencies. As a result, the phase shift extends up to  $-270^\circ$  after the second resonance, as Fig. 4 shows. Since typical compensators normally add phase up to  $180^\circ$ , the maximum achievable system bandwidth is restricted by the second resonant frequency (unless sophisticated compensators are used). Analysis shows that the first resonance frequency ( $f_{r1}$ ) is mainly determined by  $L_1$ ,  $C_o$  and  $C_2$ , while the second resonance frequency ( $f_{r2}$ ) is mainly determined by  $L_2$ ,  $C_2$  and  $C_o$ . So from aspect of power stage design, in order to help extend the closed-loop bandwidth,  $L_2$ ,  $C_2$  and  $C_o$  should be designed small to move the second resonant frequency as high as possible [2].

### III. GENERAL CONTROL LOOP DESIGN FOR THE TWO-STAGE CONVERTERS

This section begins with an overview of the different possible control approaches. The advantages and disadvantages of each control approach are discussed. Technical justification of the limitations in each control method is also presented. These summaries and discussions should prove useful to the practicing engineer when deciding which control approach to adopt for their two-stage converter.

Two possible control approaches are recommended, although numerous others are theoretically possible. First, there is a two-voltage-loop approach, as shown in Fig. 6(c). This approach is simple and regulates the transformer voltage as well as the output voltage. Because constant transformer voltage is maintained, housekeeping is simple since it can be taken directly from the transformer. Perhaps more importantly, though, is that there is no deadtime and self-driven SR can be efficiently implemented on the secondary side. A simple step-by-step control design algorithm is given for the two voltage loop approach in Section IV.

However, the two-voltage-loop control scheme has bandwidth limited by the first resonant frequency. Hence, this control design may not be suitable for applications that require fast transient response. An alternate control approach that adds an  $I_{L1}$  current loop is presented in Section V. This scheme eliminates the effects of the first resonant pole, and as a result, has wider bandwidth that is no longer limited by the first resonant frequency. Because the approach requires three

loops, as shown in Fig. 6(e), it becomes more complicated to theoretically understand. However, it is still simple for the practicing engineer to implement: a step-by-step design procedure is presented, and is (we believe) only a little more difficult to implement than the two loop approach. The benefits of the approach are that it maintains all the advantages of the two-voltage-loop control scheme but has faster response speed due to the wide bandwidth.

#### A. General discussions of control schemes

Since there are four state variables in the two-stage converter, control loops can generally be constructed with one loop, two loops or three loops according to the specific requirements as Fig. 6 (a)-(e) shows. However, the features of these approaches have not been thoroughly investigated. (Note that this paper only discusses average current feedback. Peak current control will be investigated in future papers.)

Table II summarizes the advantages and disadvantages of various control loop approaches. Technical explanations of the conclusions given in Table 2 are given below.

#### B. Discussions on Control Schemes in Figure 6

##### 1. Control schemes without $V_o'$ loop (Fig. 6 (a), (b))

These approaches are less desirable since a primary advantage of two-stage converters is that the transformer voltage is regulated. Without constant  $V_o'$ , housekeeping cannot be taken directly from the transformer and there is deadtime, which causes efficiency drops if self-driven SR is

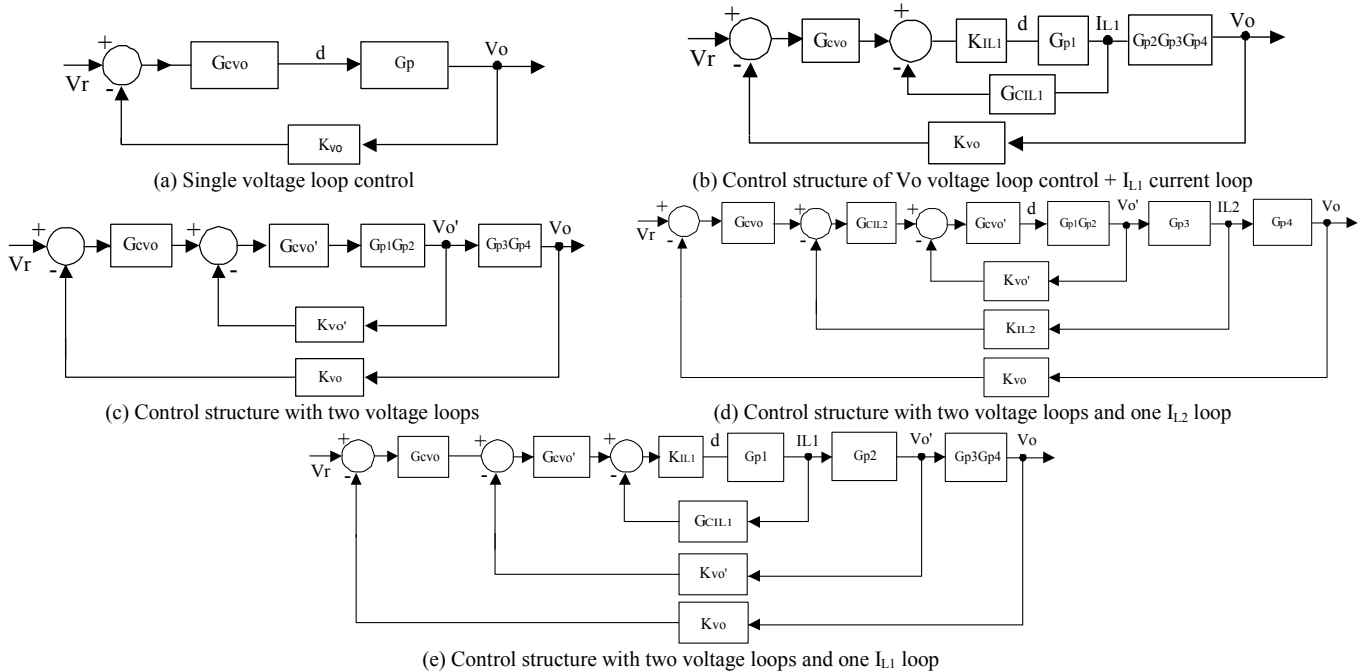


Fig. 6 Control schemes for two-stage converters

TABLE I. DEFINITIONS OF THE TRANSFER FUNCTIONS IN FIG. 6

$G_p$	d-to- $V_o$ transfer function	$G_{p4}$	$I_{L2}$ -to- $V_o$ transfer function
$G_{p1}$	d-to- $I_{L1}$ transfer function	$G_{cvo}, G_{cvo'}, G_{CIL1}, G_{CIL2}$	Compensators of $V_o$ loop, $V_o'$ loop, $I_{L1}$ loop, $I_{L2}$ loop
$G_{p2}$	$I_{L1}$ -to- $V_o'$ transfer function	$K_{vo}, K_{vo'}, K_{IL1}, K_{IL2}$	Scaling factors of $V_o, V_o', I_{L1}$ and $I_{L2}$
$G_{p3}$	$V_o'$ -to- $I_{L2}$ transfer function		

TABLE II. COMPARISON OF THE ADVANTAGES AND DISADVANTAGES OF VARIOUS LOOP IMPLEMENTATIONS

	Advantages	Disadvantages
Single $V_o$ voltage loop	The simplest way	Slow transient response, inefficient self-driven synchronous rectification, no simple house-keeping power supply
$V_o$ loop + $I_{L1}$ loop	Fast transient response	Inefficient self-driven synchronous rectification, No simple house-keeping power supply
$V_o$ loop + $V_o'$ loop	Self-driven synchronous rectification, simple house-keeping power supply	Slow transient response
$V_o$ loop + $V_o'$ loop + $I_{L2}$ loop	Self-driven synchronous rectification, simple house-keeping power supply	Slow transient response, complicated design
$V_o$ loop + $V_o'$ loop + $I_{L1}$ loop	Fast transient response, Self-driven synchronous rectification, simple house-keeping power supply	Complicated design

utilized.

### 2. Two voltage loops, Fig. 6(c)

Since  $V_o'$  is kept constant, the transformer voltage can be directly taken to drive the synchronous rectifiers and provide housekeeping power supply. This is a reasonable approach, but it is difficult to extend loop gain crossover frequencies (of either voltage loop) beyond  $f_{r1}$ . This is easily understood for conventional (PI, lag, or K-factor controllers), but is also true for even more sophisticated controllers (PI+lead, lag-lead, etc.):

*Traditional PI, lag or K-factor controllers:* These controllers always have phase angle less than zero. Since the first system resonance at  $G_{p1}G_{p2}$  causes an abrupt phase roll-off down to  $-180^\circ$  (see Fig. 4 and Fig. 5), in order for the phase margin to be sufficient it is necessary that the crossover frequency of the two loop gains be less than  $f_{r1}$  or else the system is not stable. In fact, to assure stability from possible modeling inaccuracies it is common that the crossover frequency of each of the voltage loops be smaller than  $0.1f_{r1} \sim 0.3f_{r1}$ . Despite this limitation, the two-voltage loop approach with these conventional controllers is still a reasonable approach, especially when speed of response (bandwidth) is not as vital. They are extremely simple to design.

### 3. Two voltage loops + $I_{L2}$ loop, Fig 6(d)

For this approach,  $V_o'$  loop must be designed in the same way as in the preceding scheme. The typical resulting  $I_{L2}$

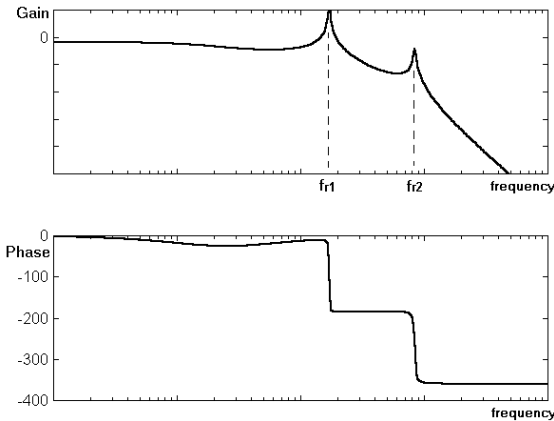


Fig. 7 Bode plot of  $I_{L2}$  open-loop transfer function with  $V_o'$  loop closed

open-loop transfer function (with  $V_o'$  loop closed) is shown in Fig. 7. From Fig. 7, it can be found that the phase quickly drops to  $-180^\circ$  at  $f_{r1}$  and  $-360^\circ$  at  $f_{r2}$ . Hence, for the similar reasons as mentioned before for the two voltage loops, conventional compensators remain unable to add sufficient phase at  $f_{r1}$  to allow the crossover frequency above  $f_{r1}$ . The achievable crossover frequency of  $V_o$  loop is still below  $0.1f_r$ .

### 4. Two voltage loops + $I_{L1}$ loop, Fig 6(e)

Introducing  $I_{L1}$  loop with  $V_o'$  loop (Fig. 6(e)) can effectively eliminate the resonance at  $f_{r1}$ . If the inner current loop can be designed to satisfy a certain loop gain condition, the crossover frequency of outer voltage loops can be extended above the resonance frequency  $f_{r1}$ , as a result of disappearance of the system resonance in the open-loop transfer functions with current loop closed. The detailed technical explanation is presented in Section IV.

## IV. TWO-VOLTAGE-LOOP AND THREE-LOOP (TWO VOLTAGE LOOPS + $I_{L1}$ LOOP) CONTROL DESIGN

This section presents specific control design algorithms for two-stage converters. Technical derivation of the algorithms is omitted, due to lack of space.

### A. Two voltage loop design

The below design algorithm for the two voltage loop controller gives:

- Inner loop gain  $T_{cvo'} = K_{vo'} G_{cvo'} G_{p1} G_{p2}$  to have a phase margin of approximately  $90^\circ$  and a crossover frequency of  $f_{cvo'} \approx 0.1f_{r1}$ .
- Outer loop gain,  $T_{cvo} = K_{vo} G_{cvo} T_{cvo'} G_{p3} G_{p4}$ , to have an arbitrary phase margin of  $\phi_{mvo}$  (we select it to be  $45^\circ$ ) and a crossover frequency of  $f_{cvo} = 0.1f_{r1} = f_{cvo'}$ .

**Step 1** Inner loop: Let  $G_{cvo'} = A_1/s$ , where  $A_1 = 2\pi f_{cvo'}/K_{vo'} V_{imax}$ .  $V_{imax}$  is the maximum rated input voltage and  $f_{cvo'} = 0.1f_{r1}$ .

**Step 2** Outer loop: Using the K-factor approach [8], specifically, let  $G_{cvo} = \frac{A(s + \omega_z)}{s(s + \omega_p)}$ . Suppose it is desired to

have phase margin  $\phi_{mvo}$  ( $\phi_{mvo} > 45^\circ$ ) at crossover frequency. Then parameters of  $G_{cvo}$  can be selected as:

$$\omega_z = \frac{\omega_{cvo}}{M} \quad \omega_p = M\omega_{cvo} \quad A = \frac{K_{vo}\omega_{cvo}MN}{K_{vo}}$$

where  $M = \tan(25^\circ + \phi_{mvo}/2)$

The above formulas should achieve a phase margin approximately equal to  $\phi_{mvo}$ , perhaps a little larger.

### B. General three-loop design (two voltage loops + $I_{L1}$ loop)

As discussed above, the control loop scheme in Fig. 6(e) has the advantage of extending the outer voltage loop crossover frequency beyond  $f_{r1}$  (To our knowledge this is the first reported method that has this capability). However, because there are three loops, it is more complicated to design. This research has developed simple step by step design algorithm for this case. The general design approach of two voltage loops +  $I_{L1}$  loop scheme is briefly described below.

•  **$I_{L1}$  current loop:** The inner  $I_{L1}$  loop is first designed. Let  $f_{notch}$ ,  $f_{r1}$ , and  $f_{r2}$  be as in Fig. 4 and Fig. 5. Let  $f_{p1} = p/2\pi$ , where  $p$  is the single real pole of the third order plant  $G_{p2}$ , which generally takes the form of

$$G_{p2} = \frac{K(s^2 + b_1s + b_0)}{(s+p)(s^2 + a_1s + a_0)} \text{ (see Appendix). A pair of}$$

conjugate zeros and a pair of conjugate poles correspond to  $f_{notch}$  and  $f_{r2}$  respectively. Controller  $G_{CIL1}$  is selected as a first order, lag compensator with a pole at  $p$ . The gain and zero of  $G_{CIL1}$  are chosen so that: 1) the phase margin is greater than  $45^\circ$ , and 2) the magnitude of loop gain  $|K_{IL1}G_{CIL1}G_{p1}| \geq 10$  in the frequency range of  $f_{p1} \leq f \leq f_{notch}$ . To secure that the second condition hold at  $f_{r1}$ , which eliminates the resonance of  $G_{p1}$ , the crossover frequency of the loop gain normally has to be set higher than  $f_{r1}$ .

Selecting  $G_{CIL1}$  in this way allows the inner  $I_{L1}$  closed-loop transfer function  $H_{IL1C}$  in Fig 6(e) to be approximated by  $1/G_{CIL1}$  in the range  $f_{p1} \leq f \leq f_{notch}$ , since

$$|H_{IL1C}| = \left| \frac{K_{IL1}G_{p1}}{1 + K_{IL1}G_{p1}G_{CIL1}} \right| \approx \left| \frac{1}{G_{CIL1}} \right| \text{ and,}$$

$$\angle H_{IL1C} = \angle \frac{K_{IL1}G_{p1}}{1 + K_{IL1}G_{p1}G_{CIL1}} \approx -\angle G_{CIL1} \text{ when } |K_{IL1}G_{CIL1}G_{p1}| \geq 10$$

•  **$V_o'$  loop:** The  $V_o'$  loop is now designed. Using the above  $I_{L1}$  loop controller, the resulting  $V_o'$  open-loop transfer function  $H_{IL1C}G_{p2}$  can be approximated as  $G_{p2}/G_{CIL1}$  when  $f_{p1} \leq f \leq f_{notch}$ . Notice that there is a pole-zero cancellation at  $p$ , which produces a constant magnitude of  $H_{IL1C}G_{p2}$  from  $f_{p1}$  up to  $f_{notch}$ , making the design of  $G_{cvo'}$  simple. A Type-1 controller (integration) is used. The loop gain of the  $V_o'$  loop can be approximated as  $K_{vo'}G_{cvo'}G_{p2}/G_{CIL1}$  in the frequency range of  $f_{p1} \leq f \leq f_{notch}$ . The block diagram is redrawn as Fig.

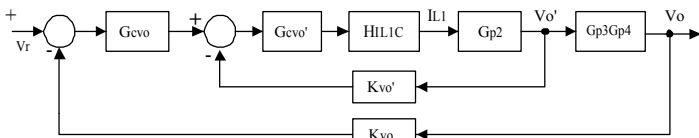


Fig. 9 Control block diagram for the inner voltage loop design

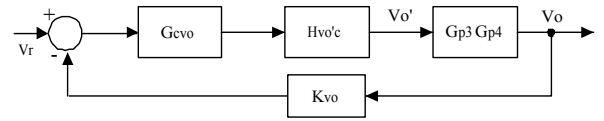


Fig. 10 Control block diagram for outer voltage loop design

9. Controller  $G_{cvo'}$  is selected so that the phase margin is greater than  $45^\circ$ . The crossover frequency can be arbitrarily selected at any frequency between  $f_{p1}$  and  $f_{notch}$ .

•  **$V_o$  loop:** Using the above design procedure, the resulting  $V_o'$  closed-loop transfer function  $H_{vo'c}$  in Fig. 10 will not exhibit noticeable resonance at  $f_{r1}$ , and so does the resulting  $V_o$  open-loop transfer function  $H_{vo'c}G_{p3}G_{p4}$ . However,  $H_{vo'c}G_{p3}G_{p4}$  still exhibits resonance at the second resonant frequency  $f_{r2}$ . So the crossover frequency,  $f_{cvo}$ , of the final  $V_o$  loop is normally selected to be less than  $f_{r2}$  but can be greater than  $f_{r1}$ . The controller  $G_{cvo}$  should be a Type-1 controller so that steady state error is zero. The controller should also keep the phase margin to be greater than  $45^\circ$ . Finally, there should be sufficient roll-off in the loop gain at high frequencies to assure noise rejection above the switching frequency  $f_s$ .

### C. Specific three-loop design algorithm

Following the general design rules of scheme (e), the design algorithm is specifically derived as below. In order to further simplify the engineering design, a few system frequencies are also presented for typical two-stage converter.

$$\omega_{r1} \approx 1/\sqrt{L_1(C_2 // C_o')}, \quad \omega_{r2} = 1/\sqrt{L_2' C_o' C_2 / (C_o' + C_2)},$$

$$\omega_{p1} \approx 1/R_o(C_o' // C_2), \quad \omega_{notch} = 1/\sqrt{L_2' C_o'}$$

#### • Step 1 Current loop compensator:

The current loop compensator can be designed as

$$G_{CIL1} = \frac{K_1(s + \omega_{z1})}{s + \omega_{p1}}, \text{ where } K_1, \omega_{p1} \text{ and } \omega_{z1} \text{ can be}$$

$$\text{determined as: } \omega_{p1} \approx 1/[R_{omin}'(C_2 + C_o')] \quad (1)$$

$$K_1 = \frac{5\sqrt{2}}{K_{IL1} \sqrt{1 + \left(\frac{\omega_{z1}}{\omega_{p1}}\right)^2} \cdot |G_{p1}(j\omega_{p1})|} \quad (2)$$

where  $|G_{p1}(j\omega_{p1})| \approx V_{imin}/R_{o'max}'$  for conservative design.

$$\omega_{z1} = \frac{\omega_{r1}[\omega_{p1} - \omega_{r1} \tan(-90 + \phi_{mL1})]}{\omega_{p1} \tan(-90 + \phi_{mL1}) + \omega_{r1}} \quad (3)$$

( $\phi_{mL1}$  is the phase margin)

Also, the switching current ripple attenuation [7] should be satisfied too.

$$|G_{CIL1}(j2\pi f_s)| = K_1 \leq \frac{V_s(1 - D_{max})}{\Delta I_{L1}}, \quad (4)$$

( $V_s$  is the oscillator ramp p-p voltage.  $\Delta I_{L1}$  is the ripple current)

#### • Step 2 Inner voltage loop compensator:

The inner voltage loop compensator is designed as:

$G_{CVo'} = \frac{K_2(s + \omega_{z2})}{s}$ , where  $K_2$  and  $\omega_{z2}$  are determined as:

$$\omega_{z2} = \omega_{cvo'} / \tan[-90^\circ + \phi_{mvo'} + \angle G_{CIL1}(j\omega_{cvo'}) - \angle G_{p2}(j\omega_{cvo'})] \quad (5)$$

$$K_2 \approx \frac{10}{K_{Vo'} K_{IL1} V_i \sqrt{1 + \left(\frac{\omega_{z2}}{\omega_{cvo'}}\right)^2}} \quad (6)$$

Where  $\phi_{mvo'}$  is the phase margin of inner voltage loop and should be chosen in the range defined by (6).

$$45^\circ \leq \phi_{mvo'} \leq 90^\circ - \angle G_{CIL1}(j\omega_{cvo'}) + \angle G_{p2}(j\omega_{cvo'}) + \tan^{-1} \left( 0.95 \omega_{cvo'} / \sqrt{\frac{1}{10\omega_{cvo'}^2} - \frac{1}{\omega_{r2}^2}} \right) \quad (7)$$

Finally, sufficient switching ripple and noise attenuation should also be secured by checking if,

$$|K_{IL1} K_{vo'} G_{cvo'}| < (0.1 \sim 0.2) V_s / \Delta V_o' \text{ at } f_s.$$

### • Step 3 Outer voltage loop compensator:

The outer loop compensator is designed as:

$$G_{Cvo} = \frac{K_3(s + \omega_{z3})}{s(s + \omega_{p3})}, \text{ where } K_3, \omega_{z3}, \omega_{p3} \text{ are determined as:}$$

$$\omega_{z3} \approx \omega_{cvo'} / \tan[-90^\circ + \phi_{mvo'} + \tan^{-1}(\omega_{cvo'} / \omega_{p3}) + \angle G_{CIL1}(j\omega_{cvo'}) - \angle G_{p2}(j\omega_{cvo'}) - \angle G_{cvo'}(j\omega_{cvo'}) - 5^\circ] \quad (8)$$

$$K_3 \approx \frac{10N \sqrt{\omega_{cvo'}^2 + \omega_{p3}^2}}{K_2 K_{Vo'} K_{IL1} V_i \sqrt{1 + (\omega_{z2} / \omega_{cvo'})^2} \sqrt{1 + (\omega_{z3} / \omega_{cvo'})^2}} \quad (9)$$

$$\omega_{p3} \leq \sqrt{\frac{(J\omega_{r2})^2 - \omega_{cvo'}^2}{1 - J^2}},$$

$$J = \frac{0.0316 C_o' V_i}{C_2 |G_{p1}(j\omega_{r2})|} \sqrt{\left(1 + (\omega_{z2} / \omega_{cvo'})^2\right) \left(1 + (\omega_{z3} / \omega_{cvo'})^2\right)} \quad (10)$$

Where  $\omega_{cvo}$  is the desired crossover frequency, and  $\phi_{mvo}$  is the phase margin of outer voltage loop.

Since the direct solutions of  $\omega_{z3}$ ,  $\omega_{p3}$  and  $K_3$  is quite complicated. Iterative solution can be used.

Finally, sufficient switching ripple and noise attenuation should also be secured by checking if,

$$|K_{vo} K_{IL1} G_{cvo'} G_{cvo}| < (0.1 \sim 0.2) V_s / \Delta V_o \text{ at } f_s.$$

Using above design algorithm,  $V_o$  open-loop transfer function ( $G_{Vo} G_{p3} G_{p4}$ ) has no resonance peak and less phase lag around the first resonance frequency. So the crossover frequency of  $V_o$  loop can be achieved higher than  $f_{r1}$ . The bandwidth is therefore improved. It is also understood that the maximum achievable crossover frequency cannot exceed the second resonance frequency due to presence of a system resonance at  $f_{r2}$  in  $V_o$  open-loop transfer function.

## V. DESIGN EXAMPLE AND EXPERIMENTAL IMPLEMENTATION

Following the general design rules of scheme (e), three control loops are designed for a 36-75V input, 3.3V output two-stage converter with 30A output current. The buck stage switches at 270kHz with isolated stage switching at 135kHz.

Transformer turns ratio is 7.78.  $L_1=13\mu\text{H}$ ,  $L'_2=2.5\mu\text{H}$ ,  $C_2=4.67\mu\text{F}$ ,  $C_o=185\mu\text{F}$ . The relevant parameters are solved as:  $f_{r1}=13.6\text{kHz}$ ,  $f_{r2}=74.5\text{kHz}$ ,  $f_{p1}=1\text{kHz}$  and  $f_{\text{notch}}=56\text{kHz}$ .

Using the step-by-step design procedures for the three-loop algorithm presented in Section V, three compensators are designed.

Based on:  $\phi_{mIL1}=45^\circ$ ,  $V_{\text{imin}}/R'_{\text{omax}}=1.8$  and  $\Delta I_{L1}=2\text{A}$ ,  $V_s=2\text{V}$  for noise attenuation check, current loop compensator is

$$\text{designed as: } K_{IL1} G_{CIL1} = \frac{0.144(s + 1.7 \times 10^5)}{s + 6.28 \times 10^3} \quad (11)$$

Choosing  $f_{cvo'}=1.5\text{kHz}$ ,  $\phi_{mvo'}=95^\circ$ , inner voltage loop compensator is designed as:

$$K_{Vo'} G_{CVo'} = \frac{0.029(s + 8.91 \times 10^4)}{s} \quad (12)$$

Choosing  $f_{cvo}=20\text{kHz}$ ,  $\phi_{mvo}=45^\circ$ , outer voltage loop compensator is designed as:

$$K_{Vo} G_{C3} = \frac{7.56 \times 10^5 (s + 4.2 \times 10^4)}{s(s + 1.25 \times 10^5)} \quad (13)$$

The experimental circuits are implemented in Fig. 11. It is simpler than the traditional implementation (omitted for limited space) and saves one Op-amp. Its transfer function structure (omitted for limited space) is roughly same as the one we used above (Fig. 11) if  $K_{IL1}=1$ . One difference is that the gain of the outer voltage loop needs to be reduced by a factor of 0.62, that is,

$$K_{Vo} G_{C3} = \frac{467647(s + 6.29 \times 10^4)}{s(s + 1.25 \times 10^5)} \quad (14)$$

The control principles are basically same.

The loop gains are measured and compared with the simulated results in Fig. 12 and Fig. 13. The crossover frequency of the outer voltage loop is achieved at 20kHz. Note that since the inner voltage is not required to be tightly regulated, its loop is not designed fast, while the outer voltage loop is expected to have a fast response.

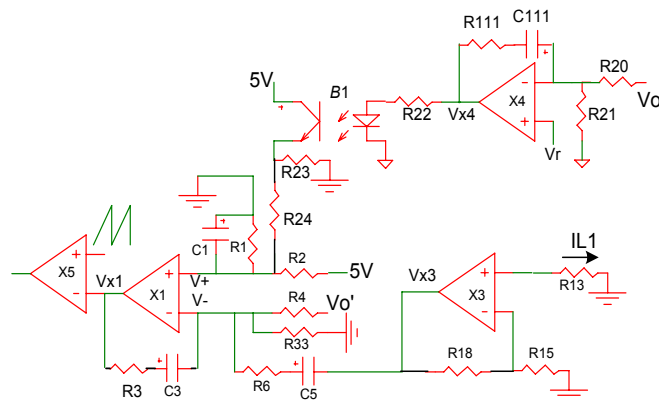


Fig. 11 Compensation circuits for the three loops

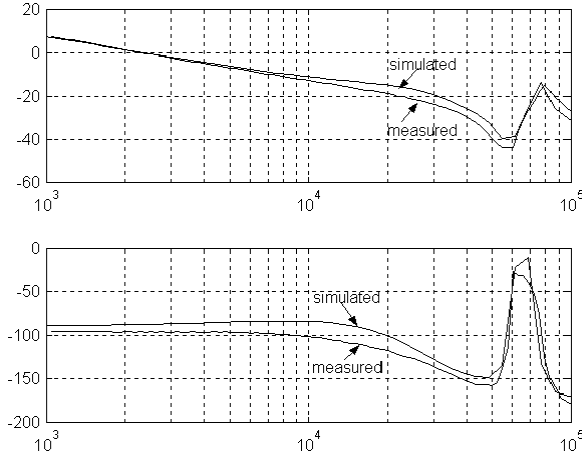


Fig. 12 Inner voltage loop gain

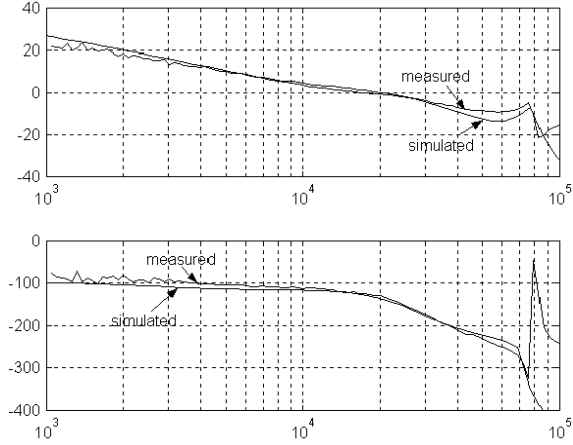


Fig. 13 Outer voltage loop gain

Also note that the phase angle spike and gain increase of the measured outer loop gain around 80kHz to 100kHz is caused by the high frequency characteristic of the optocoupler used in the loop. However, it does not affect the stability of the loop gain at high frequency. In general, it can be concluded that the simulated design results verify the experimental results. The design methodology is effective in achieving fast response for two stage dc-dc converters. Note

that the crossover frequency of the outer voltage loop is greater than  $f_{r1}$ , which is difficult to achieve using the traditional method.

## VI. CONCLUSIONS

This paper discusses the control design of two stage topologies for high voltage input, low voltage/large current output applications. Due to their inherent fourth-order small signal behaviors, the compensation loops design is relatively challenging. A complete generalized analysis of a multi-loop control design has been presented for the two-stage dc-dc converters. The proposed design methods are valid to general classes of two-stage topologies, and are able to achieve high system bandwidth. Simulations and experimental implementation further proved the effectiveness of the proposed multi-loop design.

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## Appendix:

$$\begin{aligned} \hat{V}_o &= \frac{V_i R'_o (1 + s C'_o R'_{ESR}) / N}{s^4 L_1 L'_2 C_2 C'_o (R'_o + R'_{ESR}) + s^3 (L_1 L'_2 C_2 + L_1 C_2 C'_o R'_o R'_{ESR}) + s^2 [L'_2 C'_o (R'_o + R'_{ESR}) + L_1 C_2 R'_o + L_1 C'_o (R'_o + R'_{ESR})] + s(L_1 + L'_2 + R'_o C'_o R'_{ESR}) + R'_o} \\ \hat{V}'_o &= G_{P1} G_{P2} = \frac{V_i [s^2 L'_2 C'_o (R'_o + R'_{ESR}) + s(L'_2 + C'_o R'_o R'_{ESR}) + R'_o]}{s^4 L_1 L'_2 C_2 C'_o (R'_o + R'_{ESR}) + s^3 (L_1 L'_2 C_2 + L_1 C_2 C'_o R'_o R'_{ESR}) + s^2 [L'_2 C'_o (R'_o + R'_{ESR}) + L_1 C_2 R'_o + L_1 C'_o (R'_o + R'_{ESR})] + s(L_1 + L'_2 + R'_o C'_o R'_{ESR}) + R'_o} \\ G_{P1} &= \frac{\hat{I}_{L1}}{\hat{d}} = \frac{V_i [s^3 L'_2 C'_o C_2 (R'_o + R'_{ESR}) + s^2 (L'_2 C_2 + C_2 C'_o R'_o R'_{ESR}) + s[C'_o (R'_o + R'_{ESR}) + C_2 R'_o] + 1]}{s^4 L_1 L'_2 C_2 C'_o (R'_o + R'_{ESR}) + s^3 (L_1 L'_2 C_2 + L_1 C_2 C'_o R'_o R'_{ESR}) + s^2 [L'_2 C'_o (R'_o + R'_{ESR}) + L_1 C_2 R'_o + L_1 C'_o (R'_o + R'_{ESR})] + s(L_1 + L'_2 + R'_o C'_o R'_{ESR}) + R'_o} \\ G_{P2} &= \frac{\hat{V}'_o}{\hat{I}_{L1}} = \frac{s^2 L'_2 C'_o (R'_o + R'_{ESR}) + s(L'_2 + C'_o R'_o R'_{ESR}) + R'_o}{s^3 L'_2 C'_o C_2 (R'_o + R'_{ESR}) + s^2 (L'_2 C_2 + C_2 C'_o R'_o R'_{ESR}) + s[C'_o (R'_o + R'_{ESR}) + C_2 R'_o] + 1} \\ G_{P3} &= \frac{\hat{I}_{L2}}{V'_o} = \frac{1 + s C'_o (R'_o + R'_{ESR})}{s^2 L'_2 C'_o (R'_o + R'_{ESR}) + s(L'_2 + C'_o R'_o R'_{ESR}) + R'_o} \\ G_{P3} G_{P4} &= \frac{\hat{V}_o}{\hat{V}'_o} = \frac{R'_o (1 + s C'_o R'_{ESR}) / N}{s^2 L'_2 C'_o (R'_o + R'_{ESR}) + s(L'_2 + C'_o R'_o R'_{ESR}) + R'_o} \end{aligned}$$

$$G_{P4} = \frac{V_o}{\hat{I}_{L2}} = \frac{R'_o (1 + s C'_o R'_{ESR}) / N}{1 + s C'_o (R'_o + R'_{ESR})}$$