

Dual-Bridge DC-DC Converter: A New Topology of No Deadtime DC-DC Converters*

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Abstract: Two new topologies characterized by no deadtime and small valued output inductor, the Dual-Bridge DC-DC converter and the Dual-Bridge converter with ZVS, are presented and analyzed. Simple self-driven synchronous rectification can be used in the new topology for high efficiency implementation. Prototype DC-DC converters have been tested for the verification of the principles. Both simulations and experiments verify the feasibility and advantages of the new topologies.

I. INTRODUCTION

In the past decade, the performance advances of computer, telecommunication and related fields have been bringing a serious challenge to the designer of the associated power processing networks. Especially, with the widespread use of low voltage microprocessors, digital processors, as well as various low-voltage ICs, research on DC-DC converters with low voltage and high current output has become increasingly important. Rigorous requirements of fast transient response, high power density, high efficiency, high reliability and low EMI property are the targets that modern DC-DC converter design has to face.

Historically, bridge topologies are used mainly in offline converters, i.e. when twice the rectified DC would be more

than the usual switching transistors could safely tolerate. The conversion power has historically been above 500W for the full-bridge topology. However, there is a trend to use the full-bridge topology in lower conversion power ranges of 100W to 300W and lower input voltages in the tens of volts.

A characteristic of the conventional full-bridge converter is that it (shown in Fig. 1 are its schematic diagram and key waveforms) has a deadtime during its operation. Besides preventing switches A and B (or C and D) from conducting simultaneously, this deadtime is essential for conventional dual-end (half- and full-bridge, push-pull, etc.) converters to obtain a regulated output voltage when the input voltage changes. During the deadtime, the input current becomes zero; this discontinuity causes a large input ripple current. Thus, large input filters must be used to satisfy the conducted EMC requirements. This deadtime also needs a large output inductor to smooth the output voltage and limit the ripple current through it. The large output inductor slows the output response time.

Certain topologies have no deadtime, which results in energy being continuously transmitted from the input DC source to the output load in the whole switching period. Because of the lower input ripple current in a no deadtime DC-DC converter, the conducted EMI filter is relatively

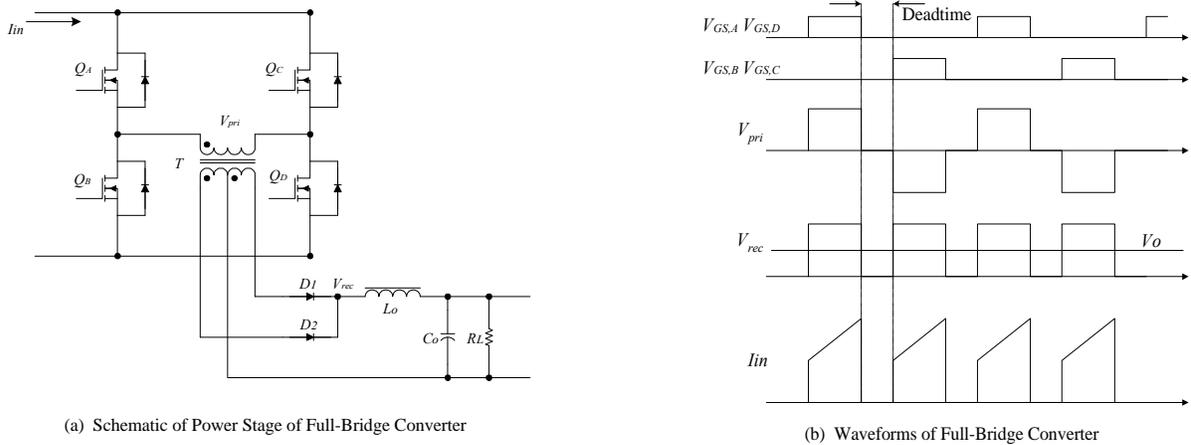


Fig. 1 Conventional Full-Bridge Converter

Patent pending.

smaller. Lower output inductance value (this will be explained later in the paper) improves the output transient speed and reduces the output filter size, thus improving power density (power-to-volume ratio) of the DC-DC converter. Several methods, for example, magnetic transformer tapping [1] and implementation with two transformers [2][3], can be used to realize no deadtime topologies. Figure 2 shows their typical waveforms of input current i_{in} and the voltage V_p across the primary winding of the transformer.

This research presents two topologies of no deadtime DC-DC converters. They are the Dual-Bridge DC-DC converter and the Dual-Bridge converter with ZVS. The new topologies are characterized by no deadtime property and have significantly reduced output filter inductors. Philips E14-3F3 cores (effective volume $V_e = 300 \text{ mm}^3$) are used as the output filter inductors in the prototype DC-DC converters with 48V input and 3.3V/30A output that are built for verifying the new topologies. Comparatively, E18 size core (effective volume $V_e = 960 \text{ mm}^3$) must be used in the DC-DC converter built with the conventional full-bridge topology. Because no deadtime is present at the secondary winding of the transformer, self-driven synchronous rectifiers can be used as output rectifiers to increase the power efficiency of the converter. This simplifies the design of rectification circuit.

Section II introduces the principle of the dual-bridge DC-DC converter. Sections III and IV present two implementations of the new topology. The analysis and comparison of the dual-bridge converter and conventional full-bridge converter are given in Section V. Section VI gives the experimental results of the dual-bridge with ZVS and Section VII concludes the paper.

II. PRINCIPLE OF DUAL-BRIDGE DC-DC CONVERTER

The principle diagram of the proposed new topology, Dual-Bridge DC-DC converter is shown in Figure 3. The idealized illustrative waveforms of voltages and currents are listed in Figure 4.

Switches SW_1 , SW_2 , SW_3 , and SW_4 consist of a full-bridge converter. Switches SW_1 , SW_2 and capacitors C_1 , C_2 consist of a half-bridge converter. Dual-Bridge converter is the combination of the full-bridge and the half-bridge. Unlike the (interesting) circuits in [2] [3], the two bridges are connected

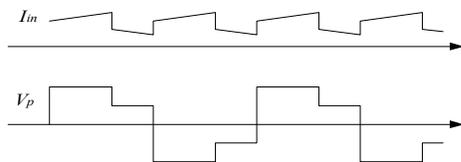


Fig. 2 Typical Waveforms of No Deadtime DC-DC Converter I_{in} is input current, V_p is the voltage across the primary winding of the transformer

by the fifth switch SW_5 , which eliminates the need of a second transformer required by [2] [3]. All components are assumed ideal for the convenience of description. V_1 and V_2 in Figure 3 are two 50% duty ratio complimentary control signals of switches SW_1 and SW_2 with frequency f . V_4 and V_3 are control signals of switches SW_4 and SW_3 with duty ratio of D and switching frequency f . V_5 drives switch SW_5 to operate at frequency $f_0 = 2f$. The switch SW_5 is turned on when both SW_3 and SW_4 are turned off.

Suppose the converter works in steady state and its output inductor current is under continuous conduction mode. Referring to Fig. 4, we now describe the operation of the dual-bridge converter: For $t_0 \leq t < t_1$, switches SW_1 and SW_4

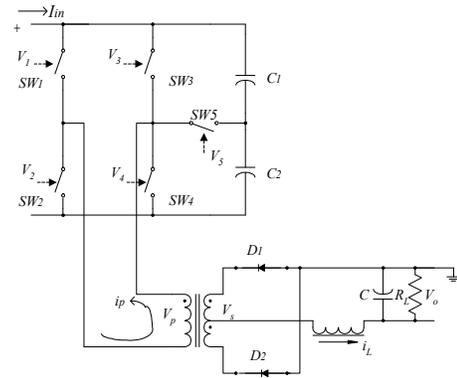


Fig. 3 Principle Illustration of Dual-Bridge Converter

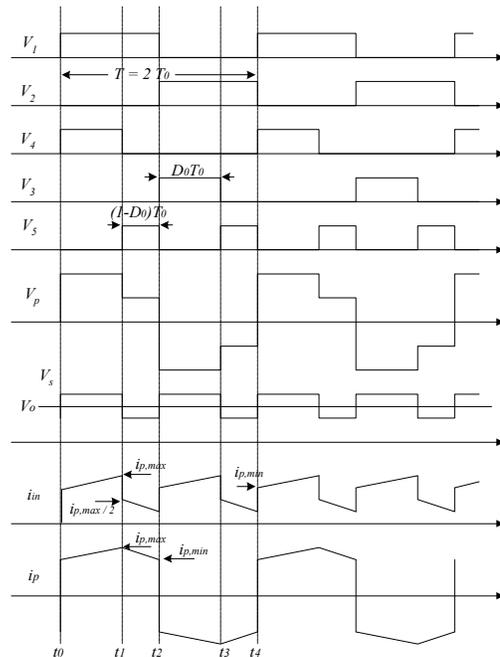


Fig. 4 Idealized Waveforms of Dual-Bridge Converter

are turned on. The voltage V_p of the transformer primary winding equals the input voltage V_i of DC source. During this period of time, the input current i_{in} increases and equals the primary winding current i_p and reaches to $i_{p,max}$ at time t_1 . At time t_1 , SW_4 is off and SW_5 is on. V_p equals $V_i/2$. From t_1 to t_2 , input current i_{in} decreases from $i_{p,max}/2$. Also, i_p , decreasing from $i_{p,max}$, is now supplied by i_{in} and the discharging and charging currents of C_1 and C_2 . At time t_2 , SW_1 and SW_5 turn off and SW_2 and SW_3 turn on. After a very short period of transient time, $V_p = -V_i$ changes polarity, and $i_p = -i_{p,min}$ changes direction. Then from t_2 to t_3 , i_p changes from $i_{p,min}$ to $i_{p,max}$. At t_3 , SW_3 is off, and SW_5 turns on. Then $V_p = -V_i/2$, $i_{in} = i_{p,max} / 2$, and i_p changes from $i_{p,max}$ towards $-i_{p,min}$, with $i_p(t_4) = -i_{p,min}$. From t_3 to t_4 , i_p is supplied by input current i_{in} and the charging and discharging currents of C_1 and C_4 . From t_4 , after a very short period of transient time, V_p and i_p change polarity, and the process repeats hereafter as stated above.

When the dual-bridge converter operates in the above-mentioned process, there is no deadtime in its operation mode. That is, energy is transmitted from the input source to the output load at any given time (switch transient time is negligible compared with the operation cycle time). In this case, the range of the input voltage change $V_{max} : V_{min}$ is limited to 2:1. When the input DC voltage is V_{min} , the duty ratio of SW_3 and SW_4 is 50%, and the duty ratio of SW_5 is 0 (SW_5 is off during the whole period T). Then the converter operates like a full-bridge converter with 50% duty ratio. When the input DC voltage is V_{max} , the duty ratio of SW_3 and SW_4 is 0, while the duty ratio of SW_5 is 100% (SW_5 turns on during T), and the converter operates like a half-bridge converter with 50% duty ratio. In these two situations, the voltage across the filter inductor L is zero, and the ripple current through L is also zero. When the input voltage changes between V_{min} and V_{max} , the duty ratio of SW_3 and SW_4 change between 50% and 0, and the duty ratio of SW_5 is from

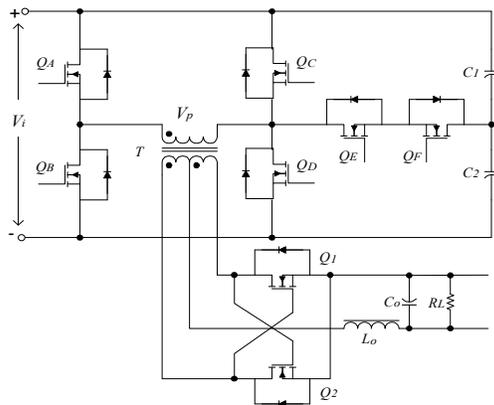
0 to 100%.

If the input voltage range is greater than 2:1, one of the schemes is, at the lower end of the input voltage range, the converter operates in full-bridge converter mode. That is, the dual-bridge converter is now a full-bridge converter consisting of switches SW_1 , SW_2 , SW_3 and SW_4 . Switches SW_1 and SW_2 operate with less than 50% adjustable duty ratio (which is the same as the duty ratio of SW_3 and SW_4), while SW_5 turns off all the time. At the upper end of the input voltage range, the dual-bridge converter operates in half-bridge converter mode. In this case, SW_1 , SW_2 , C_1 and C_2 consist of a half-bridge converter with SW_3 turns on, SW_3 and SW_4 turn off all the time, while SW_1 and SW_2 operate with less than 50% adjustable duty ratio. In the middle of the input voltage range, the dual-bridge converter operates in no deadtime mode as described above. For input voltage range wider than 2:1, it is possible for the dual-bridge converter to operate in no deadtime mode + half-bridge mode with deadtime or in full-bridge mode with deadtime + no deadtime mode.

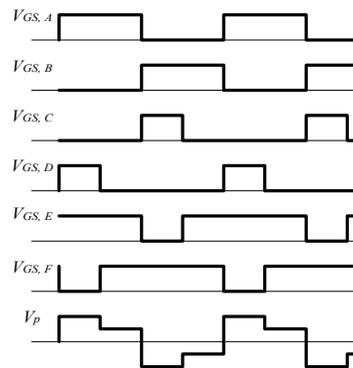
In this paper, the discussion to the dual-bridge converter is limited only to no deadtime mode with input voltage within 2:1 range.

III. IMPLEMENTATIONS OF DUAL-BRIDGE CONVERTER

Figure 5 shows the implementation of Dual-Bridge DC-DC converter. From the operation description of Dual-Bridge converter, it can be seen that SW_5 should be controlled bidirectionally. To realize this, two MOSFETs Q_E and Q_F are used to function SW_5 . Switches $Q_A \sim F$ operate at the same frequency. Q_E is off only when Q_C is on; Q_F is off during the conduction of Q_D . The time sequences of other control signals are the same as the above-mentioned description. When the Dual-Bridge converter has a low voltage output, MOSFETs are used to form synchronous rectifiers instead of using diodes D_1 and D_2 . Because the waveform of the



(a) Configuration of Dual-Bridge Converter



(b) Time Sequence of Control Signals

Fig. 5 Fundamental Implementation of Dual-Bridge Converter

secondary winding of the transformer has 50% duty ratio, simple self-driven synchronous rectification method can be used in design to improve power efficiency. This significantly simplifies the design of the rectification circuit. In the case of the conventional full-bridge converter, control-driven is often used to achieve the improvement of the conversion efficiency [4].

IV. DUAL-BRIDGE DC-DC CONVERTER WITH SOFT SWITCHING PROPERTY

Although the control signals of Dual-Bridge DC-DC converter are not phase shift signals, zero voltage turn-on switching (ZVS) property can be obtained by the correct time selection of the triggering control signals of switches Q_E and Q_F , as well as the proper design of other switch control signals' time sequence. ZVS for switches Q_E and Q_F is realized independent of load condition, whereas, for other switches, it is dependent on load condition and circuit parameters (as is generally the case for ZVS realization).

All capacitors in parallel with switches shown in Figure 6 are the switch output capacitance, C_{oss} . Inductor L_R , utilized as resonant inductance in transient process, may be the leakage inductance of the transformer. It may also be an external series inductance added to broaden the ZVS range.

The transfer from Q_A and Q_D on to Q_A and Q_F on (note that Q_E conducts all the time in and before this interval, see Fig. 7) is treated through monitored voltage $V_{DS,F}$. During the conduction of Q_D , $V_{DS,F}$ is positive and approximately equal to $V_{in} / 2$. At the end of this transfer interval, D_F , the body diode of Q_F , conducts and $V_{DS,F}$ goes to approximately zero. Then Q_F is enabled to conduct. Though the gate control signal of Q_F may have already arrived before D_F conducts, it is blocked until $V_{DS,F}$ approaches zero. The transfer from Q_B and Q_C on to Q_B and Q_E on experiences similar processes in which Q_E will not be enabled to conduct until $V_{DS,E}$ goes to approximately zero.

As stated in the implementation of the Dual-Bridge converter, this ZVS Dual-Bridge DC-DC converter can utilize the no deadtime characteristic to easily accomplish self-driven synchronous rectification at the output.

V. Dual-Bridge Converter vs. Conventional Full-Bridge Converter

The reduction of magnetic component size is an effective way of improving the converter power density of a DC-DC converter. In addition, the time to respond to a change in DC load current is dependent on the size of the output inductor (a smaller value permits more rapid current changes in it) and the bandwidth of the error amplifier [5]. Usually the inductance value of the output filter is the bottleneck of increasing transient speed. Hence, how to use smaller inductance value (thus, smaller inductor size) to meet design specifications is very important to improve the performance of DC-DC converters.

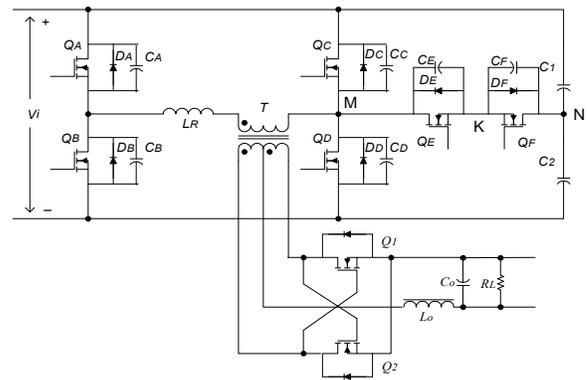


Fig. 6 Illustration of Dual-Bridge Converter ZVS Transition

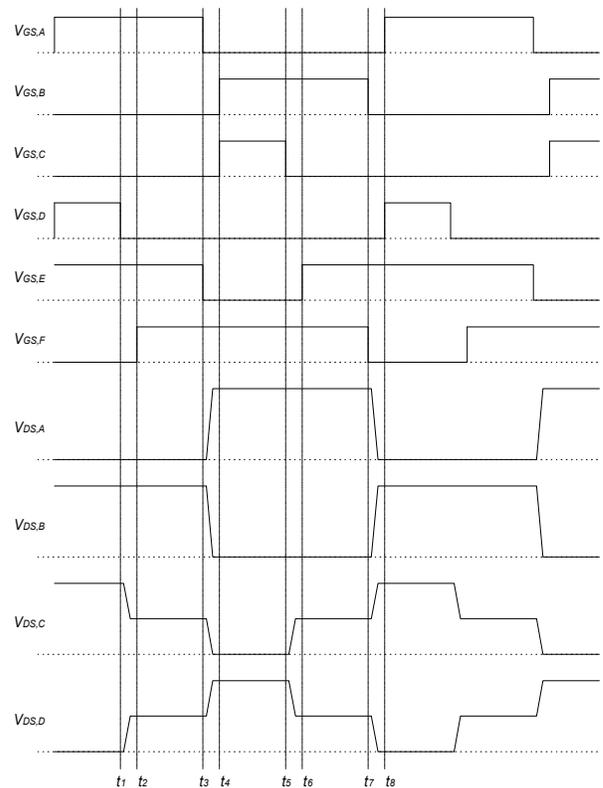


Fig. 7 Waveforms of ZVS Dual-Bridge Converter Operation

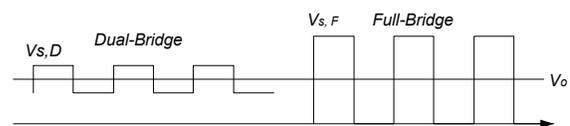


Fig. 8 Voltage Waveforms of Secondary Winding Center-tapped Point of Dual- and Full-Bridge DC-DC Converters

Figure 8 shows the voltage waveforms at the secondary winding center-tapped point for both full-bridge and dual-bridge converters. Obviously, with the same filter inductance value, the ripple current, which is proportional to the voltage difference $V_s - V_o$, of the dual-bridge converter is much smaller than that of the full-bridge converter. The quantitative analysis is given below.

The output filter inductance value of a conventional full-bridge is determined by the condition that under light load (usually, 5% ~ 10% of the full load current), the current through the inductor should keep continuous. Consider both a full-bridge converter (parameters denoted by subscripted F) and a Dual-Bridge Converter (denoted by subscripted D), with same input voltage range $V_{max} : V_{min} = 2:1$, and same output voltage V_o , same output current I_o , same switching frequency f and period T (on output rectification waveforms $f_0 = 2f$, $T_0 = T/2$), duty ratio D (primary side of transformer), $D_0 = 2D$ (secondary side), turn ratio of input winding to output winding $n:1$. Comparisons of the converter characteristics, based on idealized components are made below.

Full-bridge converter

At output, $V_{o,F} = D_{o,F} V_i / n$, The minimum input voltage (at $D_{o,F} = 1$) is $V_{i,min} = nV_o$, and we have

$$n = V_{i,min} / V_o \quad (1)$$

Peak-to-peak current on L for $0 < t < D_{o,F} T_0$ satisfies $V_s - V_o = L_F \frac{di_{p,F}}{D_{o,F} T_0}$, where V_s is the voltage of secondary winding, $\dot{A}i_{p,F}$ is the peak-to-peak current through the inductor. $D_{min,F} = nV_o / V_{i,max} = nV_o / (2 V_{i,min}) = 0.5$. Thus

$$i_{p,F} = \frac{T_0 V_{i,min}}{n L_F} \frac{V_i - V_{i,min}}{V_i} \quad (2)$$

And

$$i_{p,F,max} = 0.5 T_0 V_o / L_F \quad (3)$$

Dual-bridge converter

$$V_o = V_s D_0 + \frac{1}{2} V_s (1 - D_0) = \frac{1}{2} (1 + D_0) V_s = \frac{V_i}{2n} (1 + D_0).$$

$$\text{Or } D_{0,D} = \frac{2nV_o - V_i}{V_i}. \text{ For } D_{0,D} = 0, \text{ we have } V_{i,max} = 2nV_o.$$

For $D_{0,D} = 1$, $V_{i,min} = nV_o$ and this equation is the same as equation (1) of full-bridge converter. Therefore, we have

$$n_D = n_F = n. \text{ Also, } V_L = V_s - V_o = L_D \frac{di}{dt} = L_D \frac{i_{p,D}}{D_{0,D} T_0}.$$

Thus we have

$$i_{p,D} = \frac{D_{0,D} T_0}{n L_D} (V_i - nV_o) = \frac{V_o T_0}{L_D} \frac{(1 - D_{0,D}) D_{0,D}}{1 + D_{0,D}} \quad (4)$$

$$= \frac{T_0}{n L_D} \frac{1}{V_i} (V_{i,max} - V_i)(V_i - V_{i,min})$$

Let $\frac{d(i_{p,D})}{dV_i} = 0$, which is satisfied to obtain when

$$V_i \Big|_{i_{L,D,max}} = \sqrt{V_{i,min} V_{i,max}} \quad (5)$$

The peak-to-peak current through L_D has maximum value, which occurs for

$$D_{0,D} \Big|_{i_{L,D,max}} = \frac{V_{i,max} \sqrt{V_{i,min} V_{i,max}}}{\sqrt{V_{i,min} V_{i,max}}} = \frac{\sqrt{V_{i,max}} \sqrt{V_{i,min}}}{\sqrt{V_{i,min}}} \quad (6)$$

And for $V_{i,max} / V_{i,min} = 2$

$$V_i \Big|_{i_{L,D,max}} = \sqrt{2} n V_o \quad (7)$$

$$D_{0,D} \Big|_{i_{L,D,max}} = \sqrt{2} - 1 \quad (8)$$

$$i_{L,D,max} = (\sqrt{2} - 1)^2 \frac{T_0}{L_D} V_o \quad (9)$$

From equations (3) and (9), if the two converters have the same inductance value $L_D = L_F = L$, we have

$$\frac{i_{L,F,max}}{i_{L,D,max}} = \frac{0.5}{(\sqrt{2} - 1)^2} = 2.914. \text{ Thus, when using the same}$$

inductor as output filter, the peak-to-peak inductor current of dual-bridge converter is only approx one-third of that of conventional full-bridge converter.

If we let the two converters have the same peak-to-peak current value, that is $i_{L,F,max} = i_{L,D,max}$, then $L_D = 0.343 L_F$. So, in this case, the inductance of the dual-bridge converter is only about one-third of that of a conventional full-bridge converter. Then it can be expected that the inductor current of the dual-bridge converter has slew rate approx 3 times faster than that of the full-bridge converter.

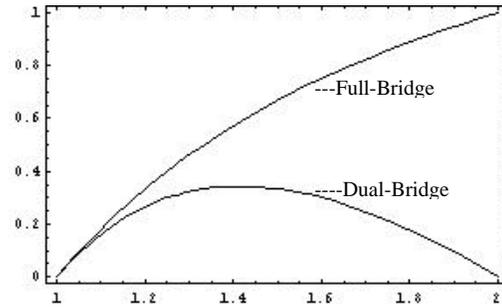


Fig. 9 Peak-to-Peak Inductor Current vs. V_i
Where $V_i: 1 \sim 2$

Figure 9 illustrates the normalized peak-to-peak current i_p vs. input voltage V_i (1~2) for full-bridge and dual-bridge converter with the same filter inductance value. The

maximum i_p of dual-bridge is 0.343 occurs at $V_i = 1.414$. For full-bridge, maximum $i_p = 1$ at maximum input voltage $V_i = 2$.

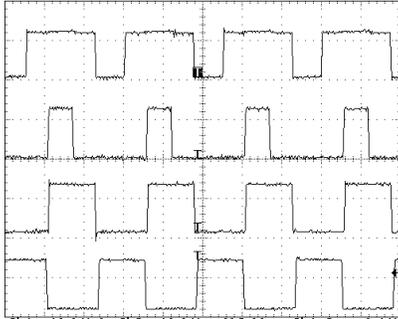


Fig. 10 Control Signals of Dual-Bridge DC-DC Converter with ZVS. From bottom trace to top trace: (10V/div)
1. $V_{GS,A}$ 2. $V_{GS,B}$ 3. $V_{GS,C}$ 4. $V_{GS,F}$. Time base: 2ns/div

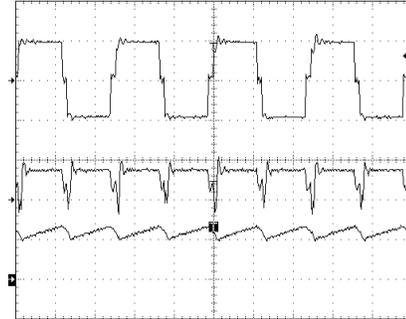


Fig. 11 Waveforms of Dual-Bridge DC-DC Converter with ZVS. $V_{in} = 37V$, $V_o = 3.30V$, $i_o = 30A$. From bottom trace to top trace: 1. i_L (25A/div) 2. V_s (5V/div) 3. $V_{DS,D}$ (20V/div). Time base: 2ns/div

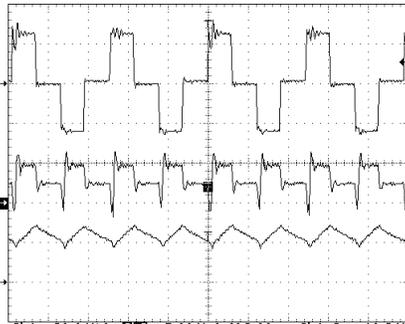


Fig. 12 Waveforms of Dual-Bridge DC-DC Converter with ZVS. $V_{in} = 48V$, $V_o = 3.30V$, $i_o = 30A$. From bottom trace to top trace: 1. i_L (25A/div) 2. V_s (5V/div) 3. $V_{DS,D}$ (20V/div). Time base: 2ns/div



Fig. 13 Waveforms of Dual-Bridge DC-DC Converter with ZVS. $V_{in} = 64V$, $V_o = 3.30V$, $i_o = 30A$. From bottom trace to top trace: 1. i_L (25A/div) 2. V_s (5V/div) 3. $V_{DS,D}$ (50V/div). Time base: 2ns/div

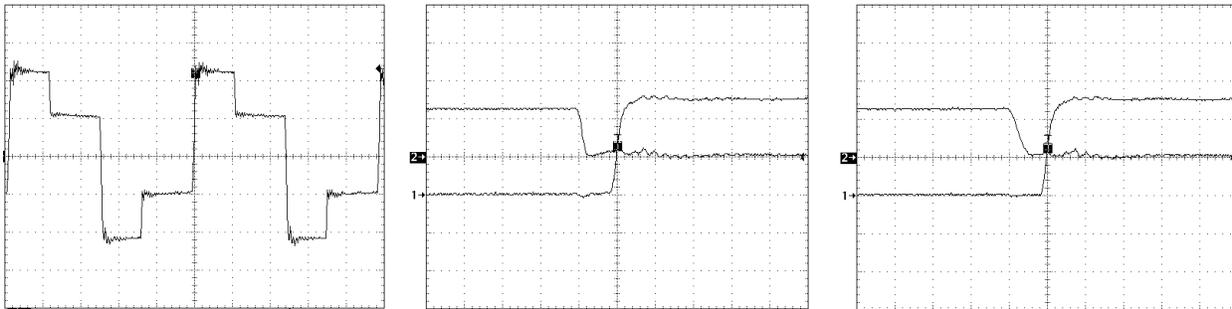


Fig. 14 Waveforms of Dual-Bridge DC-DC Converter with ZVS. $V_{in} = 48V$, $V_o = 3.30V$, $i_o = 30A$.
Left: V_p (20V/div). Time Base: 1ns/div. Middle: 1. $V_{GS,D}$ (5V/div) 2. $V_{DS,D}$ (20V/div). Time Base: 100ns/div. Right: 1. $V_{GS,C}$ (5V/div) 2. $V_{DS,C}$ (20V/div). Time base: 100ns/div

VI. SIMULATION AND EXPERIMENT

Prototypes of each of the two new Dual-Bridge topologies were built with specifications: Input voltage: $48V$ ($35\sim 64V$). Output voltage/current: $3.3V / 30A$, switching frequency: $200kHz$. The magnetic core used to make transformer is Philips planar E18 -3F3 core, and the cores used for inductors are Philips planar E14 -3F3 ($14\times 5\times 3.5\text{ mm}^3$, effective volume $V_e = 300\text{ mm}^2$) which is much smaller in size than E18 core ($18\times 10\times 4\text{ mm}^3$, effective volume $V_e = 960\text{ mm}^2$). For a conventional full-bridge converter with the same output power, E18 size core must be used for the filter inductor. Experimental results of the ZVS dual-bridge converter are shown in Figures 10 ~ 14. The results are consistent with simulations.

Figure 10 shows the control signal waveforms. Figures 11 ~ 13 show the waveforms of (from bottom to top) the current through the output inductor, the secondary winding voltage after rectification and $V_{DS,D}$, with $3.3V$ $30A$ output under $37V$, $48V$ and $64V$ input voltages, respectively. Fig. 14 illustrates the ZVS operation, in which the drain-source voltage falls to zero before the rising edge of the gate-source voltage of the corresponding switch arrives. Efficiencies under different load current ($20A$ and $30A$) are given in Fig. 15. The efficiency curves are for a prototype only, and the design is not yet optimized for power efficiency.

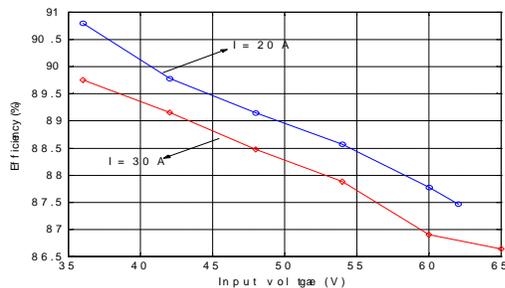


Fig. 15 Efficiency of Dual-Bridge Converter at $i_o = 20A$ and $i_o = 30A$

VII. CONCLUSION

Two new topologies of no deadtime DC-DC converters are presented and analyzed. The new topologies have been verified by both simulation and experiments (although experimental results are only presented for the dual-bridge with ZVS in this paper, due to lack of space). The output filter inductors were built with planar E14-3F3 core for 100 Watts output power and are significantly reduced in both size and inductance value, compared with the inductor of full-bridge DC-DC converter. For the latter, usually an E18 size core has to be used for the same output power.

REFERENCES

- [1] Rudolf P. Severns and Gordon (Ed) Bloom, "MODERN DC-TO-DC SWITCHMODE POWER CONVERTER CIRCUITS"
- [2] R. Ayyanar and N. Mohan, "A novel full-bridge dc-dc converter for battery charging using secondary-side control combines soft switching over the full load range and low magnetics requirement," in *Proc. IEEE Appl. Power Electron. Conf.*, 2000, pp. 340-346.
- [3] R. Ayyanar and N. Mohan, "A Novel Soft-Switching DC-DC Converter with Wide ZVS-Range and Reduced Filter Requirement," *IEEE Trans. Power Electron.*, vol. 16, pp.184-200.
- [4] W. Song and B. Lehman, "Driving Method for Synchronous Rectifier of Dual-ended DC/DC Converters", *HFPC*, 2000, pp. 446-451.
- [5] Abraham I. Pressman, "Switching Power Supply Design," Second Edition, McGraw-Hill, 1998, p158.