

A Lossless Active Clamping Circuit for Current Doubler Topologies

Yan Zhu, Liang Yan, and Brad Lehman

Abstract—This letter presents a new lossless clamping circuit on the secondary side for dc-dc converters with a current-doubler structure. This circuit reduces ringing on secondary-side rectifiers due to leakage inductance. The ringing loss is recovered to the load. As a result, efficiency is improved, and the voltage stress on secondary-side rectifiers is reduced significantly. These improvements allow dc-dc topologies with a current doubler to operate efficiently at high switching frequencies. The operating principle of the clamping circuit is detailed. Simulations and experimental results validate the proposed technique.

Index Terms—Clamping circuit, converter, current-doubler, dc-dc.

I. INTRODUCTION

TRANSFORMER-isolated dc-dc converters usually have leakage-induced, high-frequency ringing, and losses, making their operation at high frequencies less desirable. For example, conventional 48-V voltage regulator module (VRM) topologies operating at high switching frequencies have difficulty maintaining the efficiency required by the Intel performance requirements [1], [2]. One major reason for this difficulty is the parasitic oscillation between the transformer leakage inductance and the drain-source capacitance of the MOSFETs, which is caused by the reverse recovery of rectifiers [2]. In high-power converters, the associated loss of this oscillation is substantial and limits the switching frequency [17]. To reduce the oscillation, dissipative snubbers are sometimes added. Since the snubber loss increases with the switching frequency, efficiency decreases if the switching frequency is very high.

To date, many soft-switching, or snubber circuits focus on reducing the primary-side switching losses and parasitic oscillations [3]–[11]. With the primary-side switching losses reduced, the secondary-side losses also need to be eliminated, to further increase total efficiency, and the switching frequency. On the secondary side, when the rectifier diodes enter reverse recovery, the current flowing in the secondary winding exceeds the output current. Thus, extra energy is stored in the transformer leakage inductance. This part of the leakage energy resonates between the leakage inductance and the junction capacitance of the rectifier diodes after reverse recovery ends. The resonance causes ringing with a large voltage overshoot across the rectifiers.

Manuscript received November 7, 2003; revised October 8, 2004. Recommended by Associate Editor J. A. Cobos.

Y. Zhu and B. Lehman are with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115 USA (e-mail: yzhu@ece.neu.edu).

L. Yan is with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115 USA. He is also with ENI Technology, Rochester, NY 14623 USA (e-mail: Liang_Yan@mkinst.com).

Digital Object Identifier 10.1109/LPEL.2004.838776

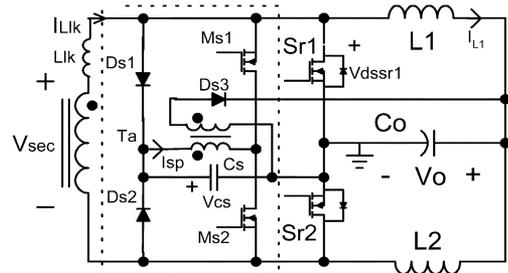


Fig. 1. Proposed active clamping circuit for current doubler, shown in dashed box.

Several lossless snubbers have been introduced to reduce the secondary-side switching losses and parasitic oscillations incurred from the reverse recovery of diodes [12]–[17]. However, most of these snubbers are designed for forward- or center-tapped winding output topologies [12]–[16] and not for circuits with a current doubler. Current doublers have been widely adopted in high-current dc-dc converters for their reduced conduction losses. An active snubber circuit has been proposed for a current-doubler topology in [17]. It recovers the oscillation energy to the load through an inductor. Like other snubber circuits [12]–[16], the snubber switch is hard-switched at turnoff when the regenerative current is at its peak. Also, the turnoff point of the snubber switch should be controlled precisely to maintain the normal voltage on the clamping capacitor for a wide-load operating range.

This letter proposes a new lossless clamping circuit for current doubler topologies, with the following features:

- effective reduction of the secondary-side oscillation of the *current doubler* output stage;
- *high efficiency energy recovery because of soft switching* of the snubber switches at both turn-on and turnoff, thus, snubber switching losses are approximately zero;
- turnoff point of the auxiliary switches is *not critical* to maintain the voltage on the clamping capacitor; can be simply synchronized to the main switches;
- *low voltage rating* synchronous rectifiers are utilized due to reduced voltage spikes, which further reduces the conduction loss on the rectifiers.

II. LOSSLESS ACTIVE CLAMPING CIRCUIT FOR CURRENT DOUBLER OUTPUT

The proposed active clamping circuit will be described based on a current doubler output stage with synchronous rectifiers (SRs), as shown in Fig. 1. The clamping circuit is encircled by the dotted line in Fig. 1. It consists of a clamping circuit D_{s1}, D_{s2}, C_s and a regeneration circuit: transformer

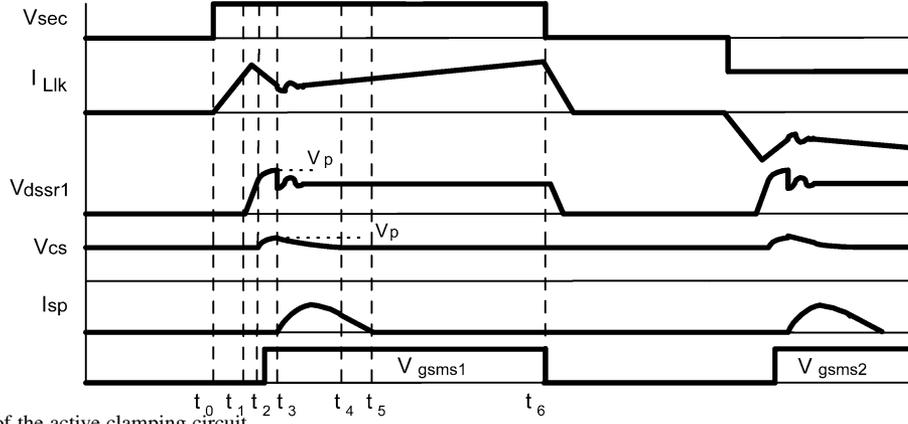


Fig. 2. Key waveforms of the active clamping circuit.

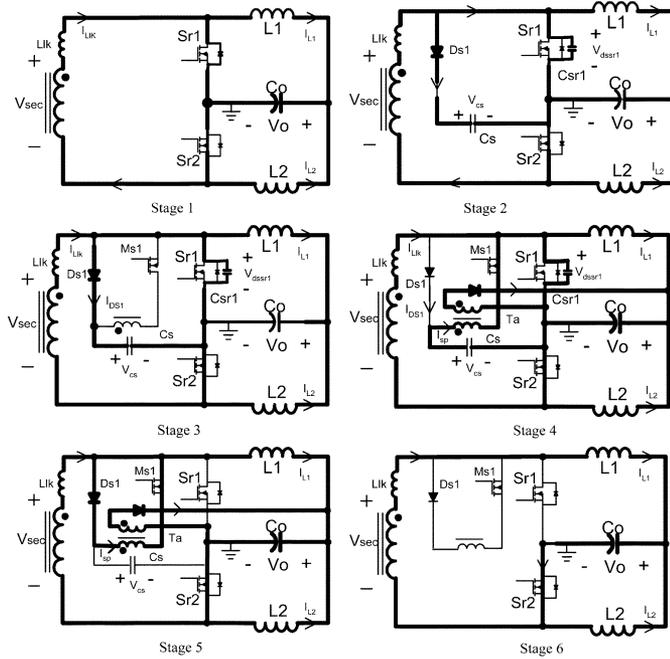


Fig. 3. Operation stages of the active clamping circuit.

T_a , T_{S1} , T_{S2} , and D_{S3} . The clamping capacitor C_S clamps the voltage across $Sr1$ and $Sr2$, eliminating oscillations and absorbing the leakage energy when the SRs are off. Then, the regeneration circuit is activated to deliver the stored energy in the clamping capacitor losslessly to the load. The auxiliary switches T_{S1} , T_{S2} , are turned on and off with zero current switching during the process. The key waveforms are shown in Fig. 2. The circuit operation includes six stages in a half switching cycle, as illustrated in Fig. 3.

Assume at the initial state t_0 , $Sr1$, and $Sr2$ are on; the currents in two inductors L_1 and L_2 are freewheeling through $Sr1$ and $Sr2$; and the voltage on capacitor C_S has been charged (shown as V_{CS} in Fig. 2). The operating principle is explained.

Stage 1: (t_0 - t_1): $Sr1$ is turned off when V_{sec} goes positive at t_0 . The current I_{Llk} in leakage inductance L_{lk} begins to increase. When I_{Llk} becomes equal to I_{L1} , the anti-paralleled body diode of $Sr1$ enters reverse recovery. I_{Llk} keeps increasing until the reverse recovery ends at t_1 .

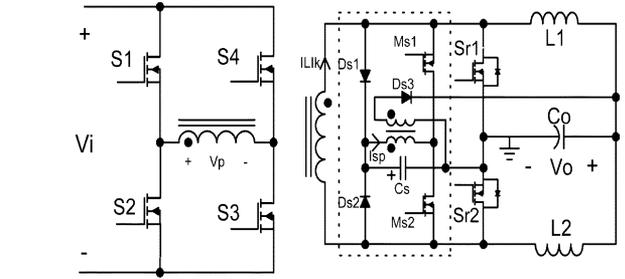


Fig. 4. Experimental phase-shift, full-bridge converter with an active clamping circuit

Stage 2: (t_1 - t_2): The extra energy stored in L_{lk} charges C_{sr1} , which is the junction capacitance of $Sr1$. The voltage across $Sr1$ (V_{dssr1}) increases until it reaches V_{CS} at t_2 . D_{s1} conducts and V_{dssr1} is clamped to the voltage on C_S .

Stage 3: (t_2 - t_3): After t_2 , L_{lk} , C_{sr1} , and C_S become a resonant path. Since C_S is chosen to be much larger than C_{sr1} , V_{dssr1} increases slowly and is clamped to V_{CS} . In the meantime, I_{Llk} decreases until it is equal to I_{L1} . Before $I_{D_{s1}}$ drops to zero, T_{s1} is turned on with zero voltage and zero current.

Stage 4: (t_3 - t_4): At t_3 , I_{Llk} is equal to I_{L1} . The current in D_{s1} is zero. L_{lk} begins to resonate with the junction capacitance of $Sr1$ until V_{dssr1} drops to V_{sec} . That amount of voltage by which V_{CS} exceeds V_{dssr1} is applied to the primary winding of the snubber transformer T_a . C_S is discharged and resonates with the leakage inductance of the snubber transformer. I_{sp} increases until $V_{CS} - V_{sec}$ is less than the reflected output voltage.

Stage 5: (t_4 - t_5): At t_4 , V_{CS} is equal to V_{sec} . D_{s1} freewheels the leakage current I_{sp} , which decreases linearly. The auxiliary transformer T_a is reset. I_{sp} drops to zero at t_5 .

Stage 6: (t_5 - t_6): After t_5 , the auxiliary circuit stops working. $I_{sp} = 0$. M_{s1} is turned off with zero current and zero voltage at t_6 . The current doubler stays with the traditional operation.

In summary, Stage 3 clamps the voltage on the synchronous rectifiers. Stages 4-5 recover the ringing energy to the load.

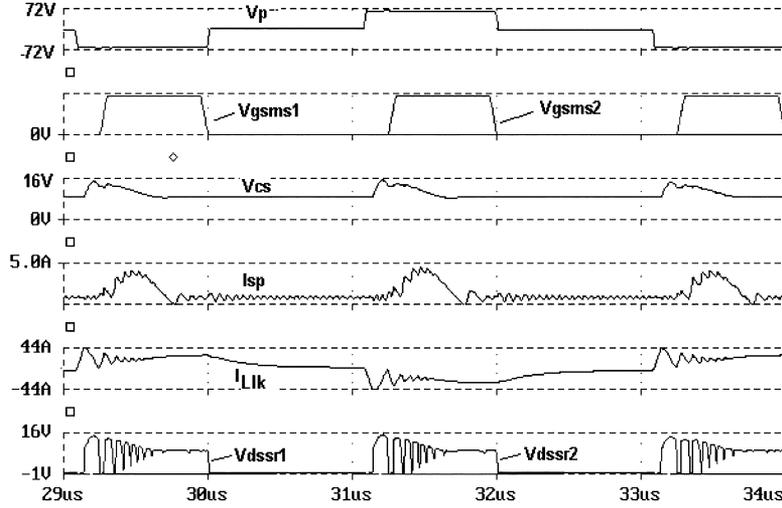


Fig. 5. Simulated waveforms of a phase-shift, full-bridge converter with an active clamping circuit.

After V_{sec} returns to zero, the $Sr1$ junction capacitance discharges. $Sr1$ is turned on again to freewheel the $L1$ current. When V_s becomes negative in the next half cycle, the snubber circuit resumes.

It is important to note that, unlike the auxiliary switch in [17] which must control the regenerative inductor current, the auxiliary switches in the proposed clamping circuit can be turned off at any time between t_5 and t_6 , with a charge balance on the clamping capacitor. Also, they are turned off with zero current since the regenerative current is zero between t_5 and t_6 . In this letter, the auxiliary switch is turned off at the same time as V_{sec} goes to zero for the convenience of timing. In the real circuit, the turn-off can be synchronized to the main switches at t_6 . Similarly, the turn-on can be synchronized at t_0 with a constant delay.

III. DESIGN EQUATIONS, SIMULATIONS, AND EXPERIMENTS

To ensure proper energy recovery, T_a leakage ($L_{lk}(T_a)$) and C_s should be chosen so that the energy recovery time (t_2-t_6) is smaller than the minimum power transfer time ($D_{min}T_s/2$). Also, the peak V_{cs} should be greater than the reflected voltage $N_{Ta}V_o$. Thus, (omitting detailed calculations) it can be derived that C_s and $L_{lk}(T_a)$ should satisfy

$$\sqrt{L_{lk}(T_a)C_s} \leq (D_{min}/2\pi f_s) - \sqrt{L_{lk}C_s}/2 \quad (1)$$

$$C_s \leq L_{lk}(I_{o\ min}/N_{Ta}V_o)^2 \quad (2)$$

where D_{min} is the minimum duty cycle; f_s is the switching frequency of the bridge switches; $I_{o\ min}$ is the minimum load current at CCM; N_{Ta} is the turns ratio of transformer T_a ; and L_{lk} is the leakage inductance on the secondary side of the (power) transformer, as shown in Fig. 1.

In most cases, the second term in the right-hand-side of (1) is small enough to be neglected. Then (1) reduces to the concept that the half resonance period of $L_{lk}(T_a)$ and C should be less than the minimum power transfer time: $\sqrt{L_{lk}(T_a)C_s} < D_{min}/2\pi f_s$.

The above analysis indicates that the leakage of transformer T_a should be made smaller when operating with a higher switching frequency. Further, to ensure energy recovery over a wide load range, N_{Ta} should not be chosen to be too large (consider 1:1 or 2:1), when maintaining a moderate peak current in M_{S1} and M_{S2} .

Simulations and experiments were performed on a full-bridge current-doubler dc-dc converter as shown in Fig. 4. The simulation result is shown in Fig. 5. The current overshoot in I_{Llk} is caused by the reverse recovery of the body diodes of the synchronous rectifiers. A prototype full-bridge current-doubler dc-dc converter with a clamping circuit was built. The converter is controlled by a UC3879 and employs the phase-shift technique. The input is 36–75 V and the output is 1.6 V/30 A. The primary-side switching frequency is 200-kHz. The primary switches use a Si4480. The SR uses three Si4466 s in parallel and utilizes control-driven SR techniques. Philips E22 and E18 cores are used for the transformer and inductors, respectively. Leakage inductance, L_{lk} , in (1) and (2), was measured to be $L_{lk} \approx 25$ nH, which is a typical value that can be used for common planar transformer coupling at this power level. Thus, using (1) and (2), the devices used in the auxiliary circuit are: M_{s1}, M_{s2} -Si4482; D_{s1}, D_{s2}, D_{s3} -BYV28-200; C_s -0.35 μ F film capacitor; T_a -E18 core/turns 3:3 with 300 nH primary leakage.

Experimental results are shown in Figs. 6 and 7. Fig. 6 shows the waveforms without clamping circuit, where a severe voltage overshoot and ringing on the synchronous rectifiers can be observed from Channels 2 and 3. This is caused by the resonance between the transformer leakage and the SRs junction capacitors. The voltage overshoot is more than 20 V, which is the typical voltage rating of synchronous rectifiers. Fig. 7 shows the waveforms with the clamping circuit. The voltage spike over the synchronous rectifiers is reduced by about half, i.e., from 24 V to 12 V, because of the effective voltage clamping. Ch3 and Ch4 show the lossless energy recovery. Experimental results agree with the theoretical expectations and simulations.

By adding the active clamping circuit to this experimental full-bridge converter with a current doubler, the power loss is reduced by about 0.64 W–1.1 W from a light load to heavy

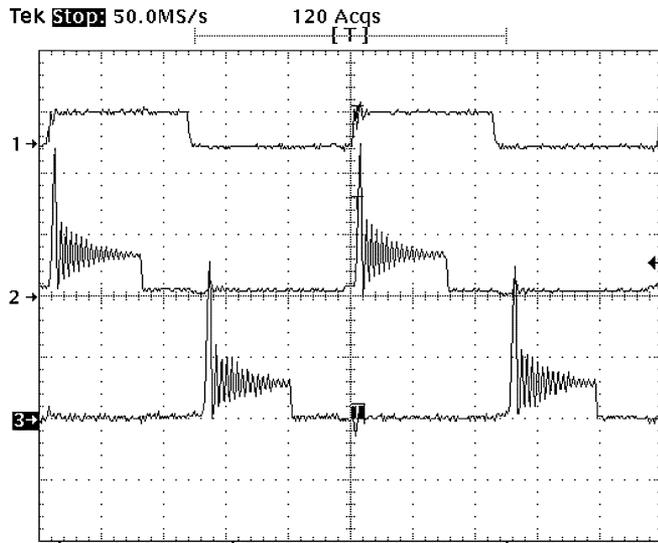


Fig. 6. Experimental waveforms of a phase-shift, full-bridge converter without a clamping circuit, Ch1: V_{gss1} , 20-V/div; Ch2: V_{dssr1} , 10-V/div; Ch3: V_{dssr2} , 10-V/div; time scale: 1 μ s/div.

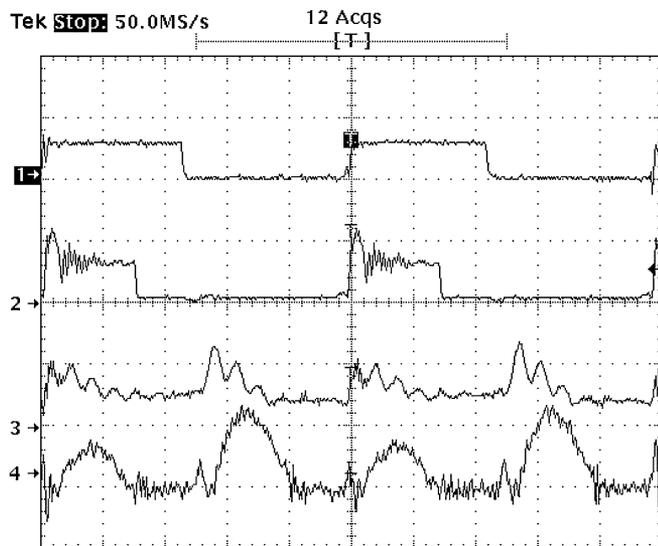


Fig. 7. Experimental waveforms of a phase-shift, full-bridge converter with a clamping circuit, Ch1: V_{gss1} , 20 V/div; Ch2: V_{dssr1} , 10 V/div; Ch3: V_{cs} , 10 V/div; Ch4: I_{sp} , 5 A/div; time scale: 1 μ s/div.

load. This corresponds to a 1% (heavy load) to a 9% (light load) efficiency improvement. Moreover, by reducing oscillation voltage across the rectifier devices, it is possible to use rectifier devices with a low voltage rating to further reduce their conduction losses. Although this clamping circuit was demonstrated on a low-power, low-voltage circuit, it can also be used in high-power dc-dc converters (where it would be more appropriate due to its circuit complexity).

It is possible to use the clamping circuit at higher switching frequencies above 200 kHz. However, the upper limit on the switching frequency depends directly on the leakage inductance of the auxiliary transformer. Too high a switching frequency will not allow the primary transformer current to complete its

half-resonant cycle. In our proof-of-concept experiment, an E14 core is used for the auxiliary transformer; this leads to a maximum switching frequency of about 200 kHz. Smaller auxiliary transformers with a lower leakage inductance should have higher maximum switching frequencies.

IV. CONCLUSION

This letter presents a new secondary-side lossless clamping circuit for dc-dc converters with a current-doubler structure. The secondary-side ringing is effectively reduced. The oscillation energy is recovered to the load losslessly due to the zero current switching of the auxiliary switches. The reduction of the voltage spike allows rectifiers to operate safely and to be used with devices of low voltage ratings, thus permitting further loss reduction. Simulations and experimental results validate the proposed technique. Of course, this clamping circuit requires additional components, thereby, adding to the circuit complexity and cost.

REFERENCES

- [1] Y. Ren and M. Xu, "A simple and high efficiency DC-DC transformer," in *Proc. VPEC Sem.*, vol. 1, 2001, pp. 173–177.
- [2] Y. Panov and M. Jovanovic, "Design and performance evaluation of low-voltage/high-current dc/dc on-board module," in *Proc. IEEE APEC*, 1999, pp. 545–552.
- [3] R. L. Steigerwald and K. D. T. Ngo, "Full-Bridge lossless switching converter," U.S. Patent 4 864 479, Sept. 5, 1989.
- [4] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. IEEE Applied Power Electronics Conf. Exhibition*, 1990, pp. 275–284.
- [5] I. Barbi and H. L. Hey, "A half-bridge zero-voltage switching pulse-width modulated DC-to-DC converter," in *Proc. IEEE Applied Power Electronics Conf. Exhibition*, Mar. 1991, pp. 140–145.
- [6] M. Shoyama and K. Harada, "Zero-voltage-switched push-pull dc-dc converter," in *Proc. IEEE Power Electronics Specialists Conf.*, 1991, pp. 223–229.
- [7] J.-G. Cho, J. A. Sabate, G. C. Hua, and F. C. Lee, "Zero-voltage and zero-current-switching full bridge PWM converter for high-power applications," *IEEE Trans. Power Electron.*, vol. 11, pp. 622–628, July 1996.
- [8] N. H. Kutkut, "Full bridge soft switched telecom power supply with a current doubler rectifier," in *Proc. IEEE Int. Telecommunications Energy Conf.*, 1997, pp. 344–351.
- [9] C. Iannello, S. G. Luo, and I. Batarseh, "Full bridge ZCS PWM converter for high voltage and high power applications," in *Proc. IEEE Annual Power Electronics Specialists Conf.*, vol. 2, 2000, pp. 1064–1071.
- [10] J. H. Liang, P.-C. Wang, and K.-C. Huang, "Design optimization for asymmetrical half-bridge converters," in *Proc. IEEE Applied Power Electronics Conf. Exposition*, vol. 2, 2001, pp. 697–702.
- [11] K.-W. Seok and B.-H. Kwon, "An improved zero-voltage-and zero-current-switching full-bridge PWM converter using a simple resonant circuit," *IEEE Trans. Indust. Electron.*, vol. 48, pp. 1205–1209, Dec. 2001.
- [12] J. A. Sabate, V. Vlatkovic, R. B. Ridley, and F. C. Lee, "High-voltage, high power, ZVS, full-bridge PWM converter employing an active snubber," in *Proc. IEEE Applied Power Electronics Conf.*, Dallas, TX, 1991, pp. 241–246.
- [13] F. S. Tsai and D. B. Dalal, "Lossless active snubber for half-bridge output rectifiers," U.S. Patent 5 351 179, Sept. 27, 1994.
- [14] A. P. Cosentino and K. Wetterquist, "Non-Dissipative Snubber Circuit for a Switched Mode Power Supply," U.S. Patent 5 615 094, Mar. 25, 1997.
- [15] J. W. Baek and C. Y. Jung, "Novel zero-voltage and zero-current-switching (ZVZCS) full bridge PWM converter with low output ripple," *Proc. IEEE INTELEC*, pp. 257–262, 1997.
- [16] H. Mao, *Snubber circuit for power converter and method of operation thereof*, July 13, 1999.
- [17] J. Dekter, N. Machin, and R. Sheehy, "Lossless active clamp for secondary circuits," *Proc. IEEE INTELEC*, pp. 386–391, 1998.