RISC-V Intro and Update

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These Guys

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Berkeley
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ASPIRE

RISC-V is an open instruction set **specification**

RISC-V

- **Modest Goal**: “Become the standard ISA for all computing devices”
  - Microcontrollers to supercomputers
- Designed for
  - Research
  - Education
  - Commercial use

RISC-V ISA

- **Fifth** RISC ISA from Berkeley, so RISC-**V**
- **Modular** ISA: Simple base instruction set plus extensions
- 32-bit, 64-bit, and 128-bit ISAs
- <50 hardware instructions in the base ISA
- Extensions: multiply/divide, single/double/quad floating point

Open Source RISC-V Cores

- Rocket Chip Generator, BOOM, and SODOR (Berkeley)
  - https://github.com/ucb-bar
- LowRISC (University of Cambridge)
  - https://github.com/lowrisc
- Shakti Cores (IIT-Madras)
  - https://bitbucket.org/casl/shakti_public
- YARVI (Yet Another RISC-V Implementation)
  - https://github.com/tommythorn/yarvi

Current Software Landscape

- Several OS ports in progress
  - Linux (Yocto/OpenEmbedded, Gentoo), FreeBSD, NetBSD, seL4
- Support primary open source toolchains
  - Binutils, GCC, clang/LLVM
- Multiple software simulators/emulators
  - Spike, QEMU, Angel, GEM5 (in progress)

Fourth RISC-V Workshop

- **Save the date**: July 12-13, 2016 at MIT CSAIL / Stata Center

Massachusetts Institute of Technology

Use RISC-V!

- RISC-V is an excellent platform for computer architecture research and education

- See you all at MIT for the 4th RISC-V Workshop (July 12-13, 2016)!

- Contact us if you want to talk RISC-V:

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