

Capacitive Low Power and High Speed PWAM Transceiver Design

Abstract

This paper presents a new signaling scheme called PWAM (pulse width and amplitude modulation) to obtain the optimum combination of bandwidth and performance of the serial link transceiver design by combining the conventional PWM (pulse width modulation) and PAM (pulse amplitude modulation) approach in the wire-line data transmission. For the number of voltage level M and the number of different pulse width N , the maximum bit rate of PWAM- $(M \times N)$ scheme improves to $\log_2 M + \log_2 N$ times the symbol rate while the maximum bit rate of PAM- M and PWM- N are $\log_2 M$ and $\log_2 N$ times the symbol rate, respectively. Novel techniques are proposed to reduce power and speed by using capacitive driven low swing transceiver. The proposed design saves 467% power and 300% higher data rate than conventional designs.

1. Introduction

In the past decade, the data processing speed of the computer systems has increased dramatically. On the other hand, the capabilities of data communication become a bottleneck of the whole system. Therefore, high-speed, low power wire-line communication is required by the modern computer systems, and the demand of more sophisticated input/output (I/O) transceiver design is increased accordingly. Serial link transceivers have a very wide application from chip-to-chip communications to the backplane and Ethernet.

However the environment of the communication channel and the semiconductor technology limit the maximum symbol rate of the serial data transmission. Therefore, many researches have been published to increase the data rate while keep the same symbol rate and sustain the signal integrity. Among them, pulse-amplitude modulation (PAM)[1] and pulse-width modulation (PWM)[2] are two advanced modulation schemes. [3] firstly introduced a transceiver that uses both PWM and PAM modulation to boost the data transmission rate. However its application is limited to the relatively low-speed data transmission (250M symbol/s) and it utilizes the conventional PWM and PAM symbol representations. The pulse width and pulse amplitude of each symbol are equally divided as shown in Fig. 1(a) and (b). This paper presents a novel and universal PAM and PWM combination scheme, where the unit pulse width and the basic pulse width are determined by the channel environment and the jitter specification instead.

Due to switched capacitances of interconnect, on-chip wires also present an increasing energy problem. A CMOS wire driver running at an effective frequency must switch a total wire capacitance C_w through the voltage, leading to a power cost proportional to $C_w V_{dd}^2 f$. Under technology scaling C_w , remains largely constant (for global wires spanning constant-sized die), voltage scales down only slowly, and f

scales up, leading to nearly constant power per wire. However, as chip's device integration level is increasing continuously, this constant power per wire gets multiplied by an ever-increasing number of wires. Novel techniques are also proposed in this paper to compensate the channel loss of different symbols.

Circuits using optimized low-voltage swings have shown a 10X energy savings, but at a 30% latency penalty and reduced noise margins [4]. More problematically, such low-swing systems typically require an expensive second power supply, which breaks up power distribution planes on the chip and in the package and necessitates additional voltage regulator modules at low target impedances.

To overcome these drawback of the low swing techniques, a coupling capacitor in line with the long wire pre-emphasis transitions is proposed in [5][6] to reduce wire delay and to reduce the load seen by the driver. In this paper, a new capacitive low power and high speed PWAM transceiver scheme is proposed to maximize the speed and to minimize the power by lowering the wire's voltage swing without additional power supply.

2. PWAM SCHEME

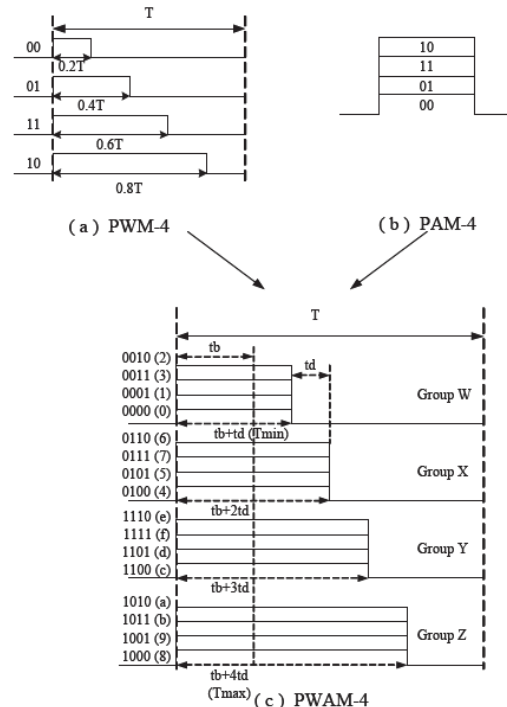


Figure 1: The PWAM Signaling (a) Conventional Symbols (b) Conventional PAM-4 Symbols (c)PWAM-(4x4) Symbols

PWAM-(M×N) scheme combines PAM-M (M is the number of different voltage levels) and PWM-N (N is the number of different pulse widths) together. With M different pulse amplitudes and N different pulse widths, there exist M ×N different symbol representations [8]. M×N symbols represent $\log_2 M + \log_2 N$ bit binary information. Therefore, the bit rate of PWAM-(M×N) is $\log_2 M + \log_2 N$ times the symbol rate. PWAM-(4×4) is illustrated in Fig. 1(c) as an example to show the symbol representations of PWAM. One PWAM-(4×4) symbol denotes 4-bit data. The 4-bit data have 16 different values, thus 16 PWAM-(4×4) symbols are used to stand for 16 different values (hereafter, 4-bit data are represented by hex 0, 1, ..., a, b, c, d, e, f). These 16 symbols are divided into four groups as shown in Fig. 1(c): Group W, X, Y, Z consists of symbol 0 1 2 3, symbol 4 5 6 7, symbol c d e f, and symbol 8 9 a b, respectively.

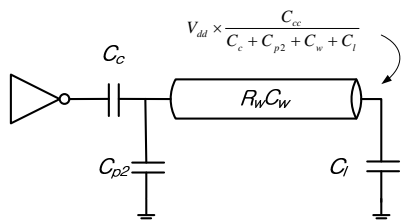


Figure 2: Driving a wire with a capacitor reduces voltage swing and provides pre-emphasis.

3. Capacitive Low-Swing Transceiver

Driving a long wire of capacitance C_w through a capacitor C_c reduces the signal swing on the wire through a capacitive voltage divider [7]. As shown in Fig. 2, including parasitic capacitance on the right side of the coupling capacitor and including the final load capacitance gives a final wire voltage swing of $V_{swing} = V_{dd} C_c / (C_c + C_w + C_{p2} + C_l)$. Typically, C_{p2} and C_l are both small compared to C_w .

The node immediately after the coupling capacitance will initially overshoot and then settle to V_{swing} , while the end of the wire will show a rapid rise to the final V_{swing} voltage.

Because it acts as a high-frequency short, the capacitor increases the 3-dB bandwidth of the long wire, allowing shorter cycle times and decreasing latency. Long wires have a low-pass frequency response that limits their operating speed. Capacitive coupling to a long wire creates a pole-zero pair, giving high-frequency emphasis that mitigates the low-pass wire response and increases performance

3.1 Transmitter end circuit

The PWAM transmitter is shown in detail in Fig. 5. It contains three main building blocks: a PWM modulator, a PAM modulator, and a pre-emphasis scheme. An 8 Phase PLL provides evenly spaced clock phases that are used to produce PWM-encoded signals. After processing Tx-bit0 and Tx-bit1 using the PWM technique, PAM signaling is used to modulate the information from Tx-bit2 and Tx-bit3. In addition to the PWAM modulator, the transmitter incorporates a pre-

emphasis block, generating pre-emphasis for both step-up and step-down code changes. Pre-emphasis compensates for the limited bandwidth of the package leads and channel medium [8].

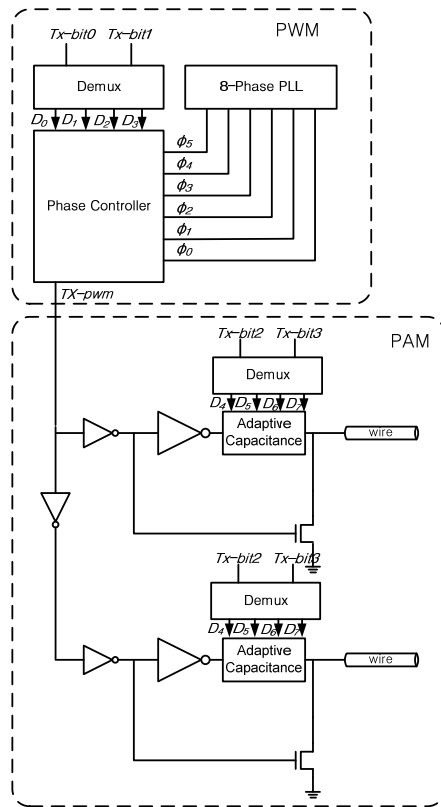


Figure 3: The block diagram of the transmitter end

3.1.1 Pulse width modulation

The pulse width modulation can be implemented by the 8 phase PLL and phase controller. 6 phase signals and control data D0~D3 are used as inputs. Based on their combinations, the pulse width is determined. The phase controller and its timing diagram are shown in Fig 4, 5.

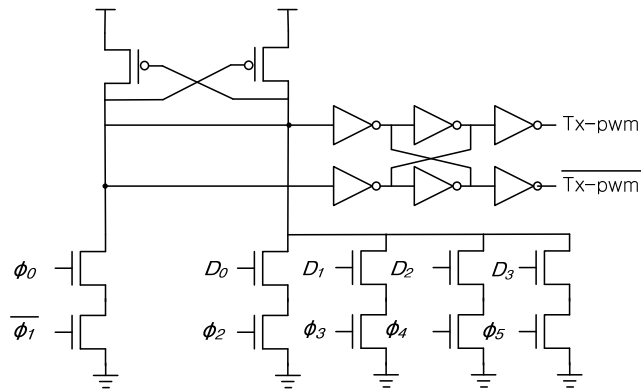


Figure 4: Phase controller

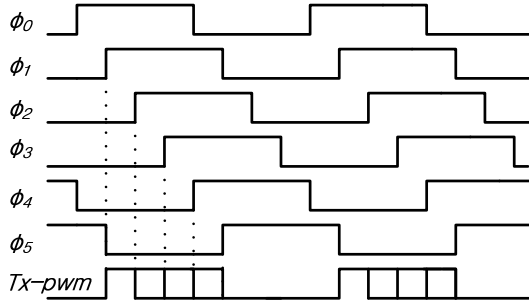


Figure 5: Timing diagram of Phase controller

3.1.2 Low swing capacitive pulse amplitude modulation

In order to realize low power PAM modulator, the low swing capacitive pulse amplitude modulation scheme was proposed in this paper.

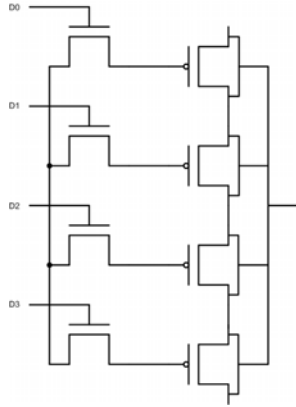


Figure 6: Adaptive Capacitance

The capacitive transmitter uses a series capacitance (C_{tx}) to drive the interconnect as shown in Fig 3. This capacitance, together with the wire capacitance, acts as capacitive divider which reduces the swing by a factor of $C_{tx}/(C_{wire}+C_{tx})$. The capacitive transmitter also increases the bandwidth of the interconnect [5][9] as C_{tx} emphasized each transition with an overshoot. The capacitive PAM driver can be implemented using adaptive capacitance which was shown in Fig. 6. The bit3, bit4 determine the output of the Demux $D1, D2, D3, D4$ which consequently decide the capacitance. By changing the capacitance, multiple V_{swing} can be obtained.

3.2 Receiver end circuits

Fig.8 shows the block diagram of the receiver. The receiver consists of 4 differential amplifier, 4 comparators, one PLL, the pulse width demodulation circuits, and some supplementary circuits. Bit2 and bit3 are recovered by PAM demodulator and bit1 and bit0 are generated from pulse width demodulation circuits. As shown in Fig 7. The architecture of the PWM demodulator is quite simple. It is composed of three D-latch and a 3bit to 2bit decoder. The PLL in the receiver end provides 8-phase clock required by the pulse width

demodulation circuit. The timing diagram of the PWM architecture is shown in Fig. 9.

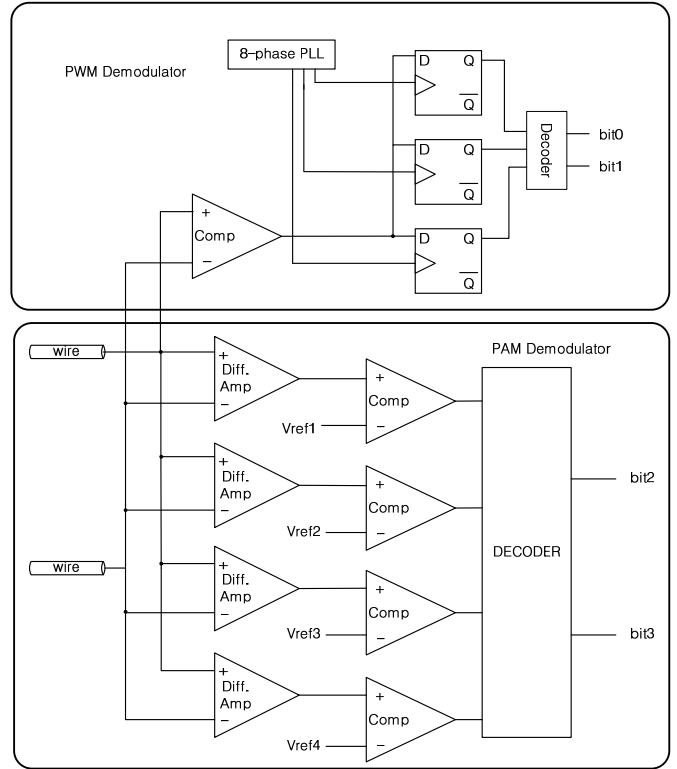


Figure 7: Receiver end circuits

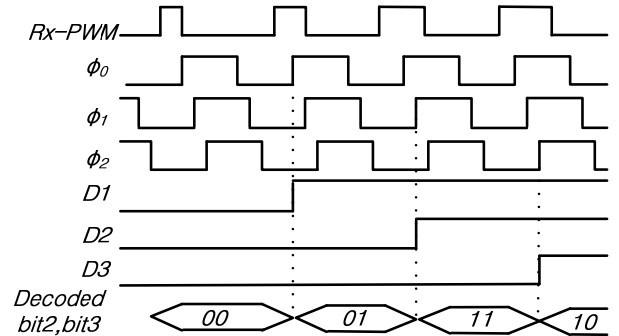


Figure 8: Timing diagram of PWM Demodulation

Because the voltage swing of signal which is received from the wire is small, it is amplified by differential amplifier ($\Delta V_{swing} = 100\text{mv}$). The different amplitude level of the received signal after amplification is 200mV. Accordingly, the reference voltages for comparators are $V_{ref1} = 1.5\text{V}$, $V_{ref2} = 1.3\text{V}$, $V_{ref3} = 1.1\text{V}$, and $V_{ref4} = 0.9\text{V}$. This multiple voltage references can be obtained from [10]. After amplification, the signal is fed into the comparator which determines digital output 0 or V_{dd} . The final bit2 and bit 3 are recovered by the

decoder based on comparator output. Table 1 shows the comparator out mapping with bit2 and bit3.

Table 1: Decoded bit2, bit 3 from comparator out

Comparator out:1,2,3,4				Bit2	Bit3
1	1	1	1	0	0
0	1	1	1	0	1
0	0	1	1	1	0
0	0	0	1	1	1

4. SIMULATION RESULTS

The circuit simulation has been done with 0.18 μ m CMOS technology, wire length of 2 mm, $C_{wire} = 560$ fF, $R_{wire} = 400\Omega$, $V_{DD} = 1.8$ V. Figure 9 shows waveform of the 4 different pulse widths and 4 different levels of voltage amplitudes. The voltage difference of each level is 100mV in the proposed design. For a fair comparison, [7] and [9] were implemented with 0.18 μ m CMOS technology and 1.8V supply voltage. The signal waveform of the proposed design is shown in Fig 9. The performance of the [7] [9] and this work are summarized in table 2.

Table 2 shows that this work's data rate is 300%~ 600% higher than others and energy per transmission is less than [7] and higher than [9]. Because the range of the voltage swing of this work is 100~400mV, it consumes more energy than [7]. However, it can save about 467% energy compared to [8] which has comparatively large voltage swing.

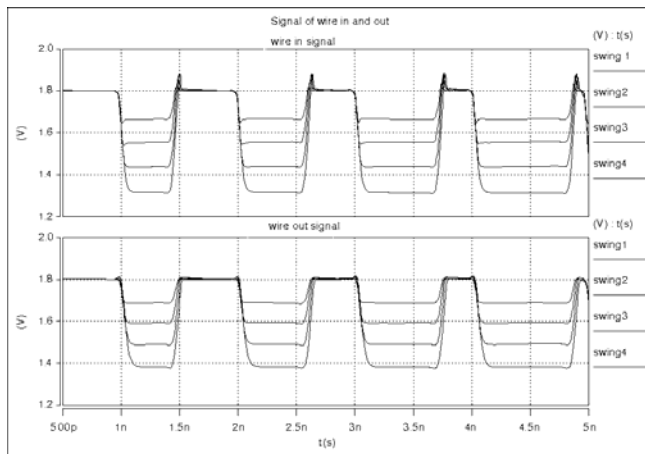


Fig 9. PWAM signals at wire ends

5. Conclusion

In this paper, capacitive PWAM transmitter architectures are proposed and its superior performances are demonstrated comparing [7][9]. Capacitive transmitter with low swing voltage can save a lot of power consumption comparing with the full swing one and other PAM scheme. Furthermore it can increase the bandwidth of the wire with pre-emphasis [5]. In this paper, proposed architecture of the transceiver shows

almost 467% power saving compared to [7] and 300% higher data rate than [9].

Table 2: Summary of the performances

Ref	[9]	[7]	This work
Data rate /channel	2Gb/s	1Gb/s	6Gb/s
Modulated Technique	N/A	PWAM	PWAM
Embedded Data/channel	1bit data	4bit data	4bit data
Transmit pre-emphasis	Yes	No	Yes
Energy/ Transmission	146fJ	780fJ	167fJ

6. References

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