

Investigation of the Performance of Carbon Nanotube FET for Analog Circuits

Abstract

Carbon Nanotube FET technology is a new promising technology for high speed digital applications. This paper investigates optimizing Analog Circuits architecture to take advantage of this technology in mixed mode ICs and point at the optimum topology for CNFETs for the first time. It was found through simulations that the optimum topology for high-bandwidth analog circuits is obtained by using architecture which avoids loading by the high CNFET gate capacitance in the main signal path at high impedance points. Low junction capacitances of CNFET and high transconductance (g_m) compared to silicon MOSFET indicates that high gain-bandwidth can be obtained by using CNFET. Simulations indicate low voltage operation (0.5V) is possible using CNFET technology and also high temperature operation ($> 200C$) is possible. Monte-Carlo simulations indicate that device matching of important CNFET parameters such as nanotube diameter, channel length, source/drain doping are important to get consistent results.

1. Introduction

As predicted by Moore's law, CMOS manufacturing technology has continued to scale to ever-smaller dimensions now reaching 32nm [1].

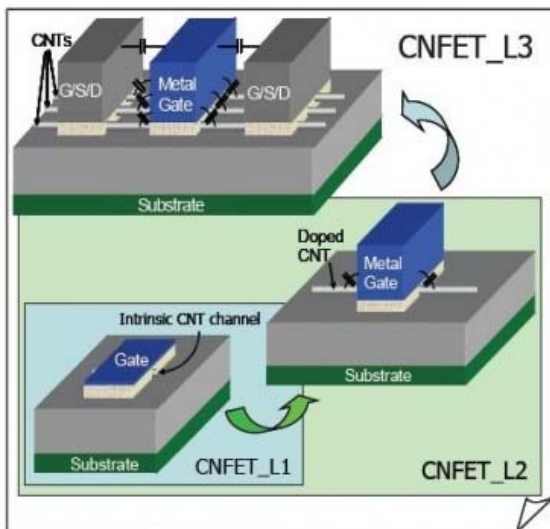


Fig. 1: Carbon NANOFET with multiple nanotubes (CNFET_L3) and with a single tube (CNFET_L2) as illustrated in [2].

At these dimensions several issues such as source to drain tunneling, device mismatch, random dopant fluctuations, mobility degradation, etc that impact its cost, reliability and performance making further scaling almost impossible. A candidate transistor that may allow for both the shrinking process to continue, and for the development of novel architectures, is the carbon nanotube field-effect transistor (CNFET) [2]. CNFET is similar to a conventional MOSFET except that its semiconducting channel is made up of carbon nanotubes (CNT) as shown in Fig. 1. Since the electrons are only confined to the narrow nanotube, the mobility goes up substantially on account of Ballistic transport as compared to the bulk MOSFET. Most attractive feature of CNTs is their near ballistic transport due to a limited carrier-phonon interaction because of larger mean free paths of acoustic phonons [3-4]. Additionally, CNFET shows higher electron mobility of the order of 10^4-10^5 cm^2/Vs [5] compared with 10^3 cm^2/Vs for bulk silicon and higher current densities, roughly three orders of magnitude greater than that reported for silicon nanowire. This indicates that CNFET is a high quality semiconducting material [6]. Major obstacles that remain are proper chirality control that decides the metallic or semiconducting nature of CNTs, specific nanotube separation with good precision and surface state control. CNFET shows the potential to sustain Moore's law in the nearby future because of its good similarity with CMOS and capability to reduce the leakage power with continued scaling [6]. Based on intrinsic CV/I gate delay, CNFET devices can be up to 13X and 6X faster than PMOS and NMOS devices of the same gate length, when local interconnect capacitances and CNT imperfections are not considered [7]. However, carbon nanotube have low on/off ratios and this problem is being considered in digital logic applications. This is not a big issue for analog circuits. Analog devices require linearity, and it has been demonstrated that CNFETs have the potential to provide linearity well beyond what is possible with silicon or III-V semiconductors [8]. The large values of g_m makes it useful for signal amplification.

$$g_m = C_g' \frac{abs(V_g - V_{g0})\mu}{L} \quad (1)$$

The ultimate limit for g_m for a ballistic nanotube transistor has been shown to be [8]

$$g_m = \frac{4e^2}{h} = 150 \frac{\mu A}{V} \quad (2)$$

However, CNFET gate capacitance may be greater than that of CMOS based on gate dielectrics currently used. This is due to high dielectric constant of commonly used insulating material ($\epsilon_{ox}=16$) and small dielectric thickness (4nm).

The differential amplifier is the basic building block in analog circuits. This paper provides the simulation and analysis of carbon nanotube FETs in differential amp/opamp circuits to point at the optimum topology when CNFETs are used with special emphasis on low-power applications. Some of the characteristics of analog/rf circuits using CNFETs were published [9-13], but to our knowledge this is the first study of optimization of CNFET circuit topology based on process parameter variations.

2. CNFET Differential Amplifier Design

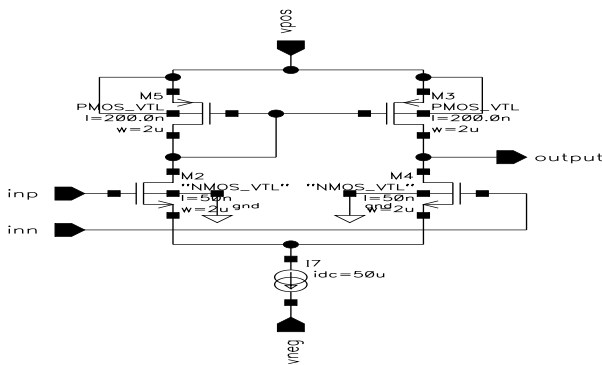


Fig 2: Basic Differential Amplifier for initial design

In this paper, Stanford models of CNFET have been used for simulation and investigation of Analog Circuits using HSPICE [8] which has been shown to account for CNFET practical non-idealities, such as scattering, effects of the source/drain extension region, and inter-CNT charge screening effects etc. apart from accurate predictions of dynamic and transient performance with more than 90% accuracy [7-8].

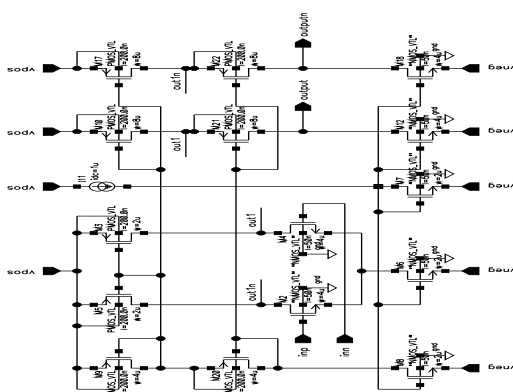


Fig. 3: Schematic of Fully Differential Amplifier used for CNFET to optimize bandwidth and power.

Top gated un-doped semiconducting (19, 0) CNFETs with 4nm thick HfO_2 , high-k dielectric ($\epsilon_{\text{ox}}=16$) was used for analysis in this paper. The commonly used CMOS

Differential Amplifier (Fig. 2) at 32nm was optimized for area, power and performance and then extended it to the CNFET design with similar geometry as CMOS. The initial design parameters of CNFET topology was set to their most practical values and then optimized. It was found that the gain of the topology using CNFET was higher than that of CMOS which can be expected due to higher transconductance and output impedance, but the bandwidth of CNFET was lower.

For increasing the bandwidth of CNFET and to have low voltage operation, we modified the design a shown in Fig 3 to have lower capacitances at all nodes. It was found through simulations that the optimum topology for high-bandwidth analog circuits is obtained by using architecture which avoids loading by CNFET gate capacitance in the main signal path. This is due to the high gate capacitance of CNFET due to high dielectric constant of commonly used insulating material ($\epsilon_{\text{ox}}=16$) [7]. The junction capacitances of CNFET are comparatively lower than silicon MOSFET [7]. Thus high bandwidth can be obtained by using this CNFET topology.

BW (MHz) vs Cloud (fF), Gain=40.5dB

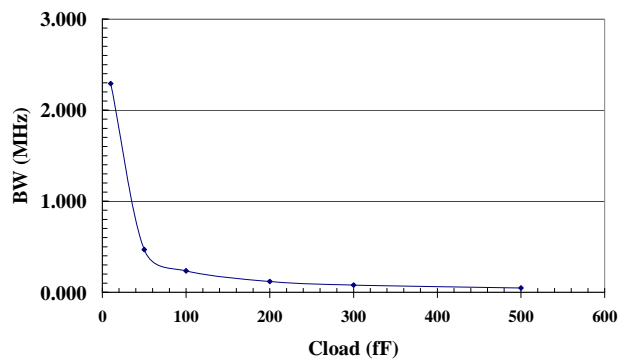


Fig 4: Variation of bandwidth with load capacitance at outputs for design with gain of 40dB and DC power dissipation of $3.75\mu\text{W}$

Gain (dB) and BW (MHz) vs Supply Voltage

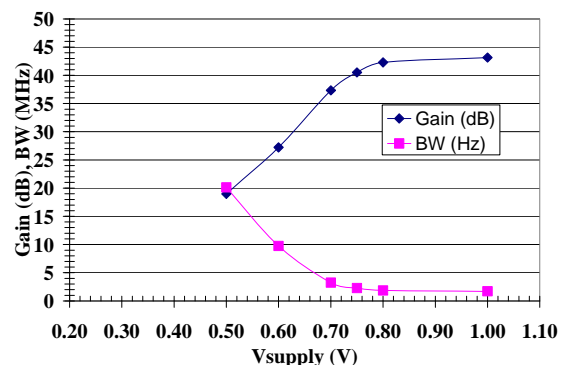


Fig.5: Variation of Gain and Bandwidth with Supply Voltage.

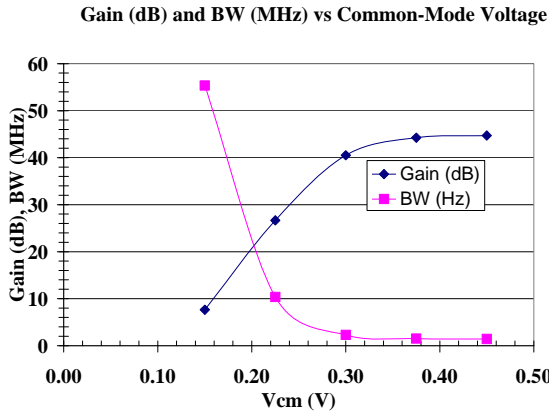


Fig. 6: Variation of Gain and Bandwidth with Common-Mode Voltage with a Supply Voltage of 0.75V.

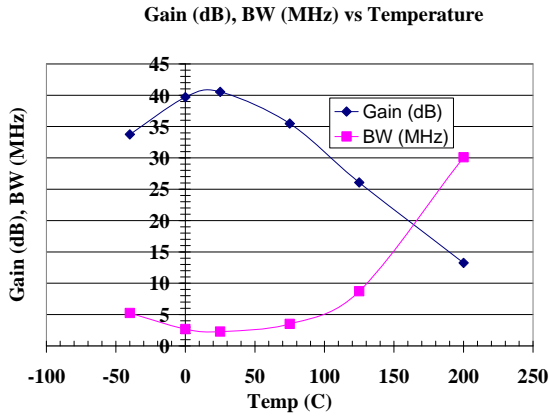


Fig. 7: Variation of Gain and Bandwidth with Temperature for a Supply Voltage of 0.75V.

There is close relationship between CNFET diameter, band-gap energy, E_g and threshold voltage, V_{th} of intrinsic CNT channel given by equations [7-8]

$$E_g = \frac{0.84 eV}{D_{CNT}} \quad (3)$$

$$V_{th} = \frac{E_g}{2e} = \frac{0.577 \alpha V_{\pi}}{D_{CNT}} \quad (4)$$

$$D_{CNT} = \alpha \frac{\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \quad (5)$$

The parameter 'a' ($\sim 2.49 \text{ \AA}$) is the carbon to carbon atomic distance, V_{π} ($\sim 3.033 \text{ eV}$) is the carbon p-p bond energy in the tight bonding model), 'e' is the unit electron charge and (n_1, n_2) are the chirality. Analytical results show that with diameter increase, all circuit performance parameters suffer with the exception of some improvement in bandwidth and transient performance. Diameter D_{CNT} is the main parameter that affects the on-current proportionally (and hence transconductance) in a CNFET apart from barrier height at

the S/D contact (E_{f0}), chirality (n_1, n_2) and oxide thickness, due to which Gain and CMRR changes. The change is appreciable when random values are used for different transistors in the topology simulated using Monte-Carlo simulations. The power consumption of the amplifier increases due to smaller band gap as CNTs become more conducting thereby, enhancing the current drive. Bandwidth improves with an increase in diameter due to smaller effective pitch which strongly affects the outer fringe and C_{gc} capacitances. It is primarily due to enhanced screening between adjacent channels. We conclude that Differential Amplifier could be designed for low power-low bandwidth and high power-high bandwidth applications on the basis of the selection of diameter.

3. CNFET Simulation Results

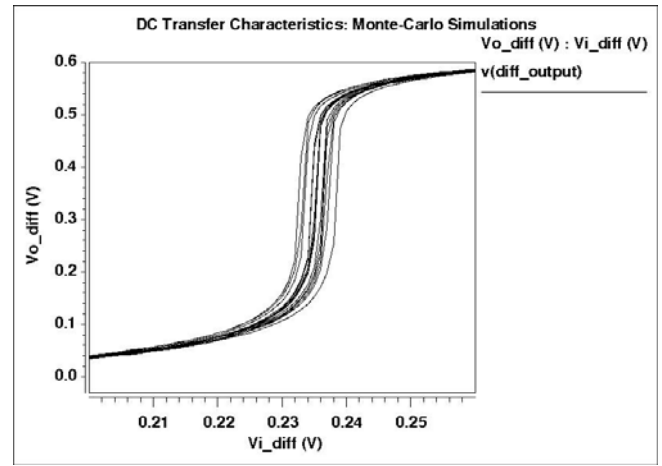


Fig. 8: Monte-Carlo Simulation with random variation of parameters to obtain DC Transfer characteristics (Output Differential Voltage vs Input Differential Voltage)

CNFET differential amplifier (Fig. 5) was found to operate at supply voltages as low as 0.5V with very low total DC current consumption (5uA) and low power (2.5uW) making it an attractive technology for Low Power/Micro-power Analog Circuits. Variation of characteristics with supply voltage variation is shown in Fig. 5. For each supply voltage, the design parameters can be adjusted to get the optimized gain, bandwidth, power trade-off. Keeping the supply voltage at 0.75V, the differential amplifier was functional with a common-mode voltage in the range of 0.15V to 0.45V. The common-mode range was extended using dual input pairs as in the case of CMOS while causing increase in power consumption. CNFET differential amplifier has been simulated to work well at high temperatures as high as 200C as shown in Fig 7. This is because of reduced scattering of carriers in CNFET compared to silicon where the scattering is increased with temperature.

Monte-Carlo simulations of CNFET topology was done to look at the effects of process variations. With random variation between transistors, the circuit parameters was found to be highly dependent on the nanotube diameter,

channel length and source/drain doping. The Monte-Carlo simulation results obtained by varying diameter, channel length and S/D doping of CNFET is shown in Fig. 8-12. The simulations indicate that matching techniques should be used in CNFETs similar to CMOS such as common centroid geometry, dummy devices at the ends etc. The median parameter values are gain of 40 dB, bandwidth of 1 MHz, unity gain frequency of 25 MHz, PSRR of -160 dB for differential output and -60 dB for common-mode output, output impedance of 47 Mega-ohm, output noise of 900nV/sqrt(Hz). These circuit parameters can be expected to get better as the technology parameters improve. Among the device parameters, the nanotube diameter had the biggest influence for random variations between transistors. However, when the parameters were varied identically for different transistors in our topology, there was minimal variation in circuit parameters indicating that CNFET technology is feasible for producing analog circuits when layout matching techniques are employed and the process variations are reduced. The change of gain and BW with nanotube diameter when it is varied identically for different transistors is shown in Fig. 13. It can be seen that if high bandwidth is desired, the carbon nanotube diameter should be small (~1 nm) while making necessary trade-offs in gain and power. For high gain in the range of 40 dB, the diameter should be in the range of 1.5 nm while achieving low power (2.5-5 μ W) at the expense of bandwidth (~2 MHz). Increase in diameter leads to decrease in band-gap energy and threshold voltage. By carefully choosing the diameter for a particular application optimum trade-off between gain, bandwidth and power can be achieved. in deciding the broad range of possible applications.

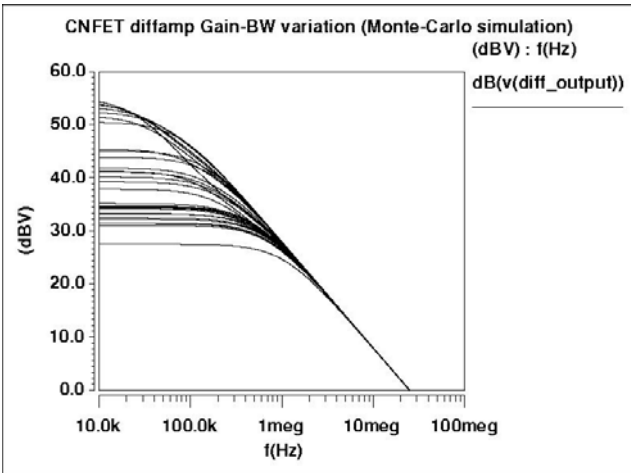


Fig. 9: Monte-Carlo Simulation with random variation of parameters to obtain Gain-BW variation.

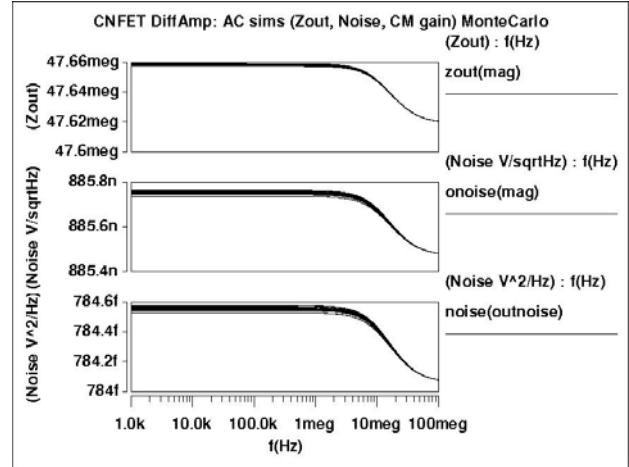


Fig. 10: Monte-Carlo Simulation with random variation of parameters to obtain Output Impedance and Noise variation.

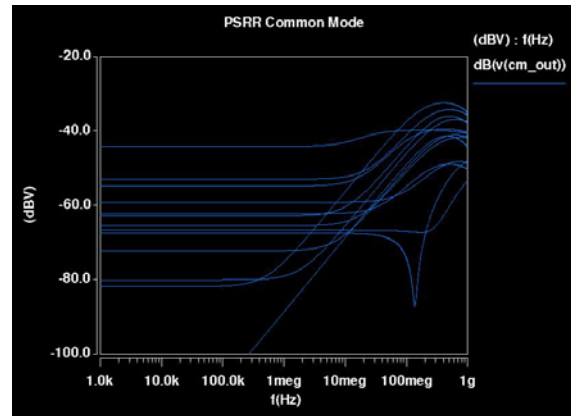


Fig. 11: Monte-Carlo Simulation with random variation of parameters to obtain PSRR (common mode output) variation.

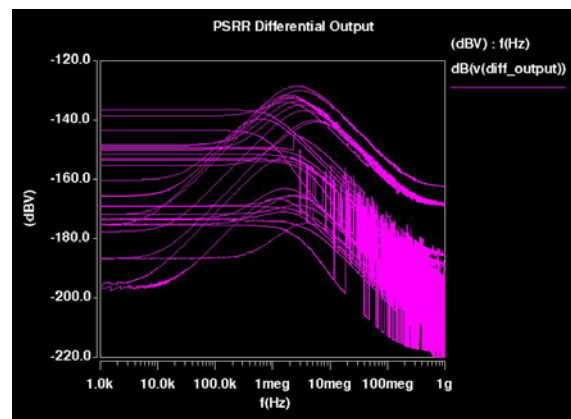


Fig. 12: Monte-Carlo Simulation with random variation of parameters to obtain PSRR at differential output.

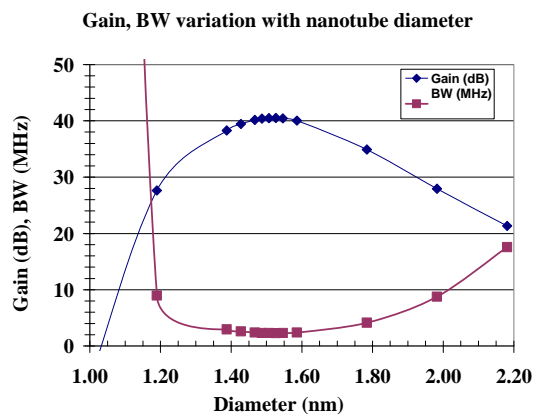


Fig. 13: Variation of Gain and BW with uniform variation of carbon nanotube diameter for all CNFET in the circuit.

4. Conclusions

This work explores basic building block of analog circuits, the differential amplifier using newly emerging CNFET technology. Bulk CMOS is expected to be at the scaling limit and this paper investigates a potential replacement. An advantage found for CNFETs is that it can be operated with supply voltages lower than 0.5V leading to lower power dissipation and compatibility to digital logic supply voltages. Another advantage found for CNFETs was good high temperature operation. Circuit characterization was also performed using variations of process conditions. Depending on performance requirements, the carbon nanotube diameter plays an important role.

In summary, CNFET technology is a promising technology for analog circuit applications provided suitable circuit topologies are used. The optimum circuit topologies are different from silicon MOS technology. Applications requiring low voltage operation, high temperature, high gain would especially benefit from CNFET technology. Some of the issues using CNFET technology for analog circuits were also discussed.

5. References

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