

A Novel All-Digital Fractional-N Frequency Synthesizer Architecture with Fast Acquisition and Low Spur

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Abstract

Digital implementation of analog function is becoming attractive in CMOS ICs, given the low supply voltage of ultra-scaled process. The conventional fractional-N frequency synthesizers suffer from the fractional spur due to the application of fractional divider. A new architecture of an all digital fractional-N phase-locked loop based frequency synthesizer is presented in this paper. The unique feature of the proposed frequency synthesizer is application of an extra time-to-digital converter (TDC) to measure the fractional value. The proposed Fraction-N frequency synthesizer is implemented using 32nm CMOS Predictive Technology Model (PTM) at 0.9V supply voltage. In the implementation example, input reference frequency is 300 MHz, frequency division factor is 2.125. The proposed circuit architecture accomplishes fast acquisition (6 cycles) time and low spurs levels.

1. Introduction

Phase-locked loops are widely used in many communication systems for clock and data recovery or frequency synthesis [1]-[3]. Cellular phones, computers, televisions, radios, and motor speed controllers are just a few examples that rely on PLLs for proper operation. With such a broad range of applications, PLLs have been extensively studied in literatures.

As technology progresses deep into submicron CMOS, traditional analog circuits face problems that cannot be solved by purely analog innovations. The analog PLLs have to overcome the digital switch noise coupled with power through power supply as well as substrate induced noise. In addition, the analog PLL is very sensitive to process parameters and must be redesigned if the process is changed or migrates to next generation process. Instead, new architectures are being proposed which take advantage of the relative cheapness of digital circuits to augment or improve the diminishing performance of the analog circuitry. Recently, all digital phase locked loops have become more attractive. Although ADPLL won't have the same performance as its analog counterpart, it provides a faster lock-in time and better testability, stability, and portability over difference process [4], [5].

Digital Phase locked loop based frequency synthesizers have been used in applications requiring either agile frequency switching or high-precision frequency control. An unavoidable occurrence is that frequency multiplication (by N), raises the signal's phase noise by $20\text{Log}(N)$ dB. By reducing the value of N , we could rationally reduce the phase noise of the system. However, the channel spacing of an

integer-N synthesizer is dependent on the value of N . A fractional-N frequency synthesizer has benefits compared with classical integer-N implementations. It is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state.

Although fractional-N frequency synthesizer could achieve better phase noise performance, faster lock and better spur levels, it also generates fractional spurs from the fractional divider. By introducing delta-sigma control in the feedback divider, fractional spurs can be eliminated. In this case, fractional spurs are spread over the spectrum and become quantization noise which is shaped by the delta-sigma modulator to high frequencies. A low pass filter with one order higher than that of the delta-sigma modulator is used to filter out the high frequency noise. This approach is efficient but might not lead to complete elimination of spurs, since a delta-sigma modulator can generate spurs by itself due to idle tones. Pseudorandom sequences can be mixed with the delta modulator input to reduce the idle noise, but this will incorporate additional hardware. Another way to suppress fractional spurs is to reduce the bandwidth, but this result in degradation of the noise and an increase of the lock time.

In this paper an all digital phase locked loop based fractional-N frequency synthesizer is presented. During the lock-in process, the update of the control words of the DCO in every reference cycle is based on the exact measurement of the time difference between DCO output and Ref clock. This lock-in process is much faster than the blind "fast" or "slow" comparison. In addition, different from the conventional fractional-N frequency synthesizer, an extra TDC is applied to obtain the fractional value avoiding the use of fractional divider, which is the main source of fractional spur in a fractional-N frequency synthesizer. The proposed Fraction-N frequency synthesizer is implemented using 32nm CMOS Predictive Technology Model (PTM) at 0.9V supply voltage.

2. Fractional Spur Analysis in Conventional Fractional-N frequency Synthesizer

The fractional- frequency synthesizer can both generate a high frequency signal with a well defined frequency and modulate that signal. An introduction to the use of modulator in frequency synthesis can be found in [6], and a block diagram of a conventional fractional- synthesizer is shown in Fig. 1. This structure is very similar to integer-N frequency synthesizer with the additional of an accumulator. The accumulator is a simple state machine that changes the main divider value (between N and $N+1$) during a locked condition.

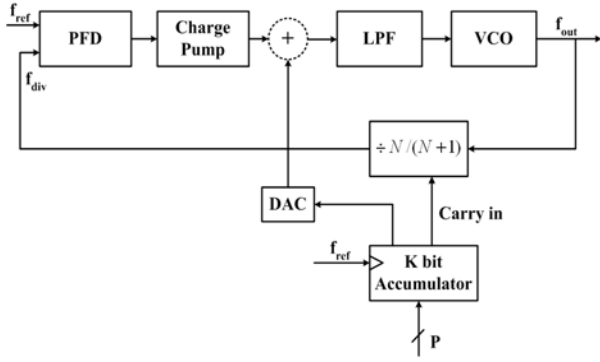


Figure 1: Conventional fractional-N synthesizer.

By varying the divider number between N and $N+1$ dynamically, a fractional divide ratio can be obtained. However, even though a VCO is locked into a desired frequency, there always exists a phase error or noise at most of comparing instants due to the uneven division. If out of 2^k cycles, we divide by $N+1$ p times and by N , 2^k-p , then average output frequency will be:

$$f_{out} = (N + p / 2^k) f_{ref} \quad (1)$$

,where p and k are the fractional parts and the number of the bits of the accumulator.

Similar to the analysis in [7], within one reference cycle, the phase difference ΔT between the reference signal and divided output should be:

$$\Delta T = 1 / f_{ref} - 1 / f_{div} = \frac{p}{2^k} T_{out} \quad (2)$$

At the- n th reference cycle, the corresponding phase difference ΔT_n should be:

$$\Delta T_n = \left[\frac{pn}{2^k} \right] T_{out} \quad (3)$$

$[\cdot]$ represents the fractional part of the quantity inside $[\cdot]$ (less than 1). Assume the average phase shift of the divided output to be Δ . In fractional-N frequency synthesizer, the average control voltage V_{ctrl} should be a constant value. As a result, the average current of the charge pump should equal to 0 and we get:

$$I_{cp} \sum_{n=0}^{Q-1} (\Delta T - \Delta) = I_{cp} \sum_{n=0}^{Q-1} \left(\left[\frac{pn}{2^k} \right] T_{out} - \Delta \right) = 0 \quad (4)$$

Therefore,

$$\Delta = \frac{1}{Q} \sum_{n=0}^{Q-1} \left[\frac{pn}{2^k} \right] T_{out} \quad (5)$$

$Q \cdot T_{out}$ is the time period of the charge pump output current. The pulse position and pulse width of this periodic current signal can be calculated as following:

$$p_p(n) = \left(n \cdot T_{ref} + \frac{\Delta T_n - \Delta}{2} \right) \quad (6)$$

$$p_w(n) = (\Delta - \Delta T_n) \quad (7)$$

The Fourier series coefficient of each current pulse is:

$$C_{n,k} = \frac{1}{k} \sin[kw_Q \frac{1}{2} (\Delta - \Delta T_n)] \cdot \exp[-ikw_Q (nT_{ref} + \frac{\Delta T_n - \Delta}{2})] \quad (8)$$

$$w_Q = 2\pi / QT_{out} \quad (9)$$

$$k = 0, 1, \dots, Q-1 \quad (10)$$

By adding the corresponding Fourier series coefficients of each current pulse together, we get the Fourier series of the charge pump's output current pulse noise. This phase noise generated by the fractional divider can be modeled as if it were an autonomous phase noise source with a special spectral property and the output frequency spectrum can be calculated through the closed loop transfer function. The normalized power of the charge pump output current pulse noise's Fourier series components k is shown in Fig. 2.

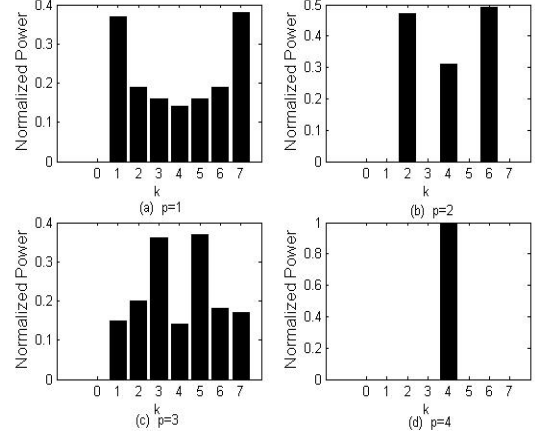


Figure 2: Normalized Fourier series of the current pulse.

3. Principle of the Proposed ADPLL Based Fractional-N Frequency Synthesizer

The concept of the digital phase locked loop has existed almost as long as the PLL itself and has been widely used in clock synthesis and data recovery application. However, the conventional DPLL based fractional-N frequency synthesizer suffers from the spur as discussed above. In ultra-scaled technologies, the ADPLL, which has replaced all the analog components with purely digital equivalents, is becoming more attractive. The output frequency in fractional-N designs is given by

$$F_{DCO} = F_{REF}(N + K/F) \quad (11)$$

The F is the fractional resolution of the device with respect to the reference frequency. In the time domain, we can rewrite the equation as follows:

$$T_{REF} = (N + K/F)T_{DCO} \quad (12)$$

Without taking into consideration the fractional part, $(K/F)T_{DCO}$, the proposed architecture is an integer-N frequency synthesizer. The fast lock-in process of a similar structure has been published in [8]. A time-to-digital converter measures the time difference between the reference clock and the divided DCO output. As shown in Fig. 3, it converts time difference into the digital word T_1 and T_2 , which are the time difference between the divided DCO output's rising edge and the reference clock's rising and falling edges, respectively. As a result, the frequency (period) difference can be defined as follows:

$$\Delta T = (T_1 - T_1') + (M - 2)T / 2 \quad (13)$$

$$T = 2(T_2 - T_1) \quad (14)$$

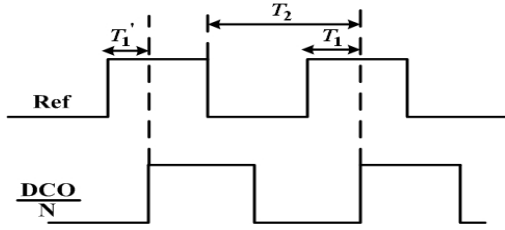


Figure 3: Principle of an integer-N frequency synthesizer lock-in process.

M represents the reference clock's low-to-high or high-to-low transition number during one DCO_clock period from the 4-bit counter. T_1' is the stored value of T_1 in the previous DCO period.

In conventional fractional frequency synthesizer design, the integer divider is usually replaced by a fractional one. The proposed ADPLL based fractional-N frequency synthesizer uses an extra TDC to calculate the fractional part as shown in Fig. 4. The fractional division can be replaced by a multiplication function and equation 3 can be rewritten as

$$\Delta T = (T_1 - T_1') + (M - 2)T / 2 + \frac{K}{F} T_{DCO} \quad (15)$$

As a result, when the DCO is locked into the desired frequency, there is no spur noise resulted from the uneven divider anymore. The proposed design in this paper provides a low spur and fast lock-in solution to the fractional-N frequency synthesizer design.

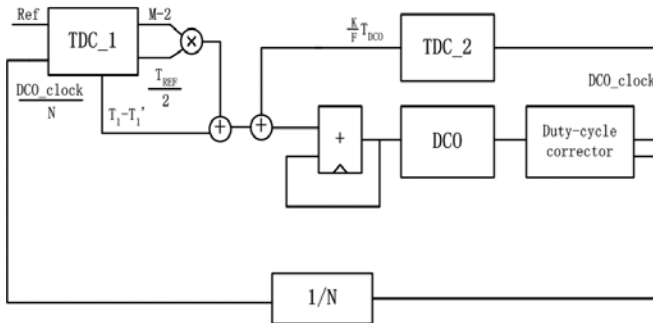


Figure 4: Proposed ADPLL based fractional-N frequency synthesizer

4. Circuit Design

1. Time-to-digital Converter

The TDC used in this paper is composed of two parts: an integer counter that counts the reference clock edges within one DCO clock period and a fractional counter that quantizes the residual phase difference, which helps to improve the resolution of the proposed TDC.

The block diagram of the fractional TDC structure is shown in Fig. 5. It consists of 16 delay blocks and two types of independent decoders. The resolution of the TDC is the delay of a single buffer, which minimizes the delay mismatch compared to the delay of a single inverter. The reference clock waveform propagates through a chain of 8 times 16 delay elements whose outputs are sampled by 8 times 16 flip-flops at the rising edge of each DCO_clock.

The decoding process is shown in Fig. 6. The 16 bits output of the delay block are decoded into the higher 4 bits of T_1 & T_2 . At the same time, the 8 bit output of each delay block is also decoded into a series of lower 3 bits of T_1 & T_2 . Based on the output of decoder1, the proper set of T_1 (0:2) and T_2 (0:2) is selected. As shown in Fig. 6, the transition takes place in the 2nd and 6th blocks. As a result, the decoded output of those two blocks is selected as the lower 3 bits of T_1 and T_2 . The separation of the decoder into two parts greatly reduces the design complexity.

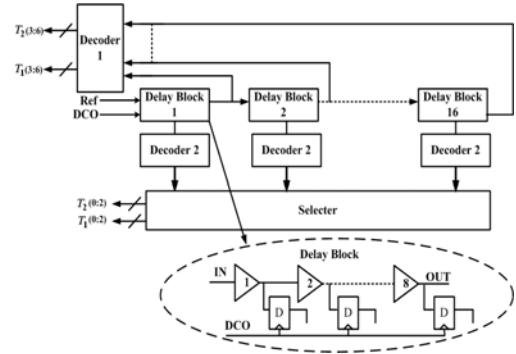


Figure 5: Block diagram of fractional TDC structure

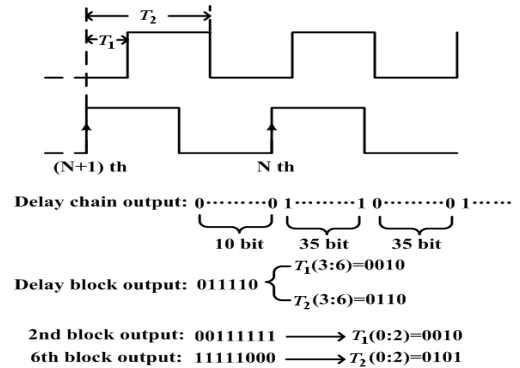


Fig 6: Decoding process of the TDC

2. Digitally Control Oscillator

The digitally controlled oscillator in this paper employs a new approach to increase the delay tuning range using digitally controlled pass transistor arrays and Schmitt trigger based inverters as shown in Fig. 7. The coarse cells have tuning codes of 2 bits with PMOS array or NMOS array in a form of thermometer code, which could provide a better duty cycle performance and linearity. Three stage constant delay chains and 4:1 MUX are used to increase the operating range. The fine cell has tuning codes of 6 bits by only NMOS array in the form of thermometer code as shown in Fig. 7c. The thermometer code could minimize the jitters. Since they are grouped per 2 bits, the conversion circuit size is also minimized. Moreover, the Schmitt trigger based DCO circuit provides the same tuning range with smaller capacitance loading, which is beneficial for power consumption reduction. It has a good robustness to process, voltage, and temperature variations and better linearity comparing to the conventional design.

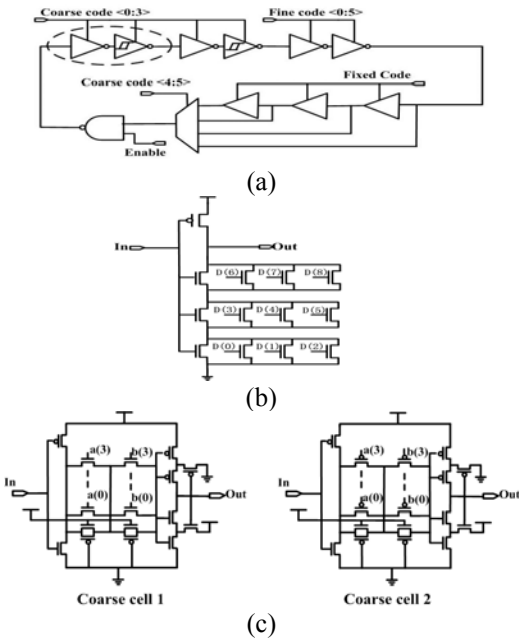


Figure 7: Digitally controlled ring oscillator. (a) DCO block diagram, (b) Fine delay cell, (c) Coarse delay cell.

5. Simulation Results

The proposed APDLL structure is designed and simulated using 32nm CMOS Predictive Transistor Model (PTM). The target spec used for the example design is the following: Integer part of division, N is 2, and reference frequency is 300MHz. The effective division ratio is 2.125. The reference and VCO waveforms in locked state are plotted in Fig.8. The frequency acquisition time is 6 cycles while the conventional approaches take at least 10 cycles. In this figure, 17 cycles of the DCO output signal has same duration of the 8 cycles of the reference signal. This indicates that the theoretical frequency division ratio of 2.125 is achieved. The frequency spectrums of DCO output and reference signal are shown in Fig. 9.

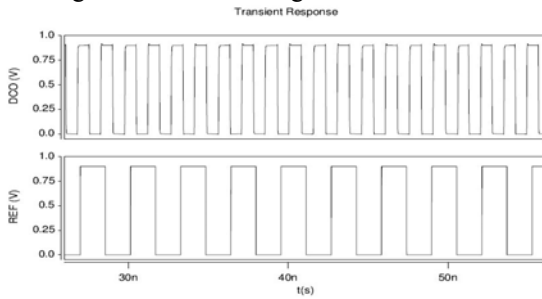


Figure 8: Reference and VCO waveforms in locked state

6. Conclusion

In this paper a new APDLL based fractional-N frequency synthesizer is presented. This design is aimed to reduce the spur by replacing the fractional divider with another TDC. The proposed architecture is designed and simulated using 32nm PTM. The transient simulation result shows that proposed design has a fast lock-in time and reduced spur noise which has potential use in highly noise environments.

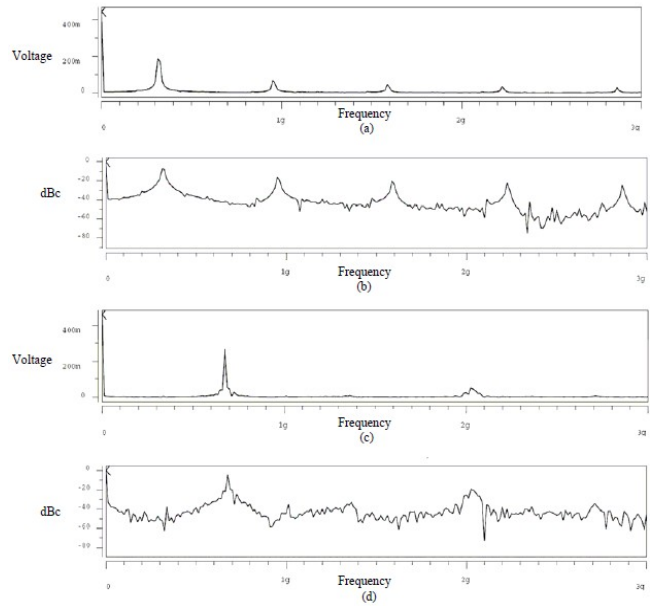


Figure 9: Frequency spectrum of DCO output and reference signal. (a) FFT analysis of reference signal, (b) Frequency spectrum of reference signal (c) FFT analysis of DCO output (d) Frequency spectrum of DCO output

7. Reference

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