Self Adaptive Body Biasing Scheme for Leakage Power Reduction in Nanoscale CMOS Circuit

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ABSTRACT

This paper presents techniques to determine the optimal reverse body bias (RBB) voltage to minimize leakage currents in modern nanoscale CMOS technology. The proposed self-adaptive RBB system finds the optimum reverse body bias voltage for minimal leakage power adaptively by comparing subthreshold leakage current (I_{SUBTH}), gate tunneling leakage (I_{GATE}), and band-to-band tunneling leakage currents (I_{BTBT}) in standby mode. The proposed circuit has been designed and tested using 65nm bulk CMOS technology at 25ºC under a supply voltage of less than 1V. The optimal RBB was achieved at -0.372V with 1.2% error in the test case of the paper, and the simulation result shows that it is possible to reduce the total leakage current significantly as much as 86% of the total leakage using the proposed circuit techniques.

Categories and Subject Descriptors

B.7.1 [types and design styles] advanced technologies

General Terms

Design, Performance

Keywords

Self-adaptive body bias voltage, Subthreshold leakage, Gate tunneling leakage, Band-to-band tunneling, Power consumption

1. INTRODUCTION

To achieve higher density, higher performance, and lower power consumption, CMOS transistors have been scaled aggressively for decades and the supply voltage has been reduced along with the shrinking of device dimensions. Therefore, the threshold voltage (V_{TH}) of a transistor has to be commensurately scaled to achieve high performance. Unfortunately, due to the exponential relationship between leakage current and threshold voltage, decreasing of V_{TH} leads to a dramatic increasing of subthreshold leakage. Reverse body biasing (RBB) is one of the most widely used methods to reduce subthreshold leakage, which has already been introduced by [1]. However, the increasing RBB increases drain-induced barrier lowering (DIBL) and substrate doping density, which leads to an increasing of band-to-band tunneling leakage. At the same time, increasing of RBB will increase V_{TH}, causing short channel effect in ultra-small technology, which results in an increase of gate tunneling leakage.

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Previous research [2] [3]shows, in the standby mode, a certain fixed RBB can reduce I_{SUBTH} while maintains a relatively small I_{GATE} and I_{BTBT}. And it has been shown in [4] that correctly applying body bias reduces the impact of die-to-die and within die parameter variations. Therefore, the implement of optimal RBB can lead to both reduction of leakage power and yield improvement.

In this paper, a novel leakage monitoring schematic is proposed, and the principle of the scheme is illustrated in Figure 1. To monitor the leakage current components, I_{SUBTH}, I_{BTBT}, and gate induced drain leakage (I_{GIDL}) currents, are generated from a test device and convert the difference of I_{SUBTH} and I_{BTBT} current into voltage signals assuming the gate tunneling leakage is not as large as the other two leakage components. The converted voltage called "Vc" goes to the charge pump shown in the Figure 1 to charge and discharge the capacitor in the charge pump. The voltage in the capacitor is fed back to the leakage monitoring circuit through the output stage in the Figure 1 to control the body bias voltage of the test device to reduce the total leakage and to form a closed loop. The closed loop is necessary to make the scheme adaptive and to maintain the optimal body bias status continuously. An optimal RBB is achieved and maintained in the steady state if the two leakage currents become equal.

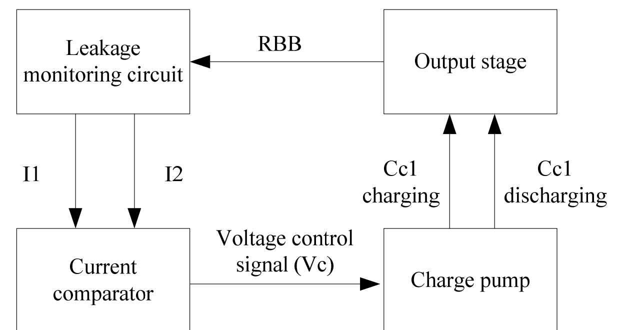

Figure 1 block diagram of optimal RBB generating system

This paper is organized as follows: Section 2 presents the three major leakage current components in ultra-small CMOS technology, and Section 3 explains the novel schematic of our optimal RBB system. Section 4 presents the results of the achieved optimal RBB and its VT variations, followed by the conclusion of the paper in Section 5.

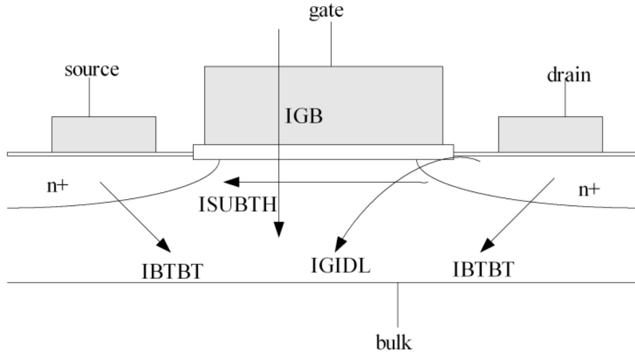

Figure 2 Leakage components in 65nm bulk CMOS transistor in the standby mode

2. Leakage current components

There are several leakage components in scaled CMOS transistors as illustrated in Figure 2. The major leakage components in nanoscale CMOS technology are I_{SUBTH}, I_{GATE} and I_{BTBT}. Thus, the total leakage current can be expressed as

$$I_{LEAKAGE} = I_{SUBTH} + I_{GATE} + I_{BTBT} \tag{1}$$

Those three major leakage currents components need to be understood for leakage reduction efforts and they are explained in this section.

2.1 Subthreshold leakage

When the gate-to-source voltage in a MOS transistor is below V_{TH}, the transistor is not completely turned off, instead, there is weak inversion region having some minority carriers along the length of the channel. This makes a small current flow from drain to source in NMOS case, which is called the subthreshold leakage and is expressed as:

$$I_{SUBTH} = I_0 e^{\frac{V_{GS}-V_{TH}}{nkT/q}} \cdot \left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \tag{2}$$

Where

$$\mathbf{I_0 = \mu_0 \cdot C_{ox} \cdot (W/L) \cdot (\frac{KT}{q})^2 \cdot \left(1 - e^{1.8}\right)} \tag{3}$$

V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, kT/q is the thermal voltage, n is the body effect coefficient [5], and V_{DS} is the drain to source voltage.

2.2 Gate tunneling leakage

In order to keep short-channel effect under control and to maintain a good subthreshold turn-off slope, gate oxide thickness is reduced in proportion to channel length. This results in an exponential increase in the gate leakage due to the direct tunneling of electrons through gate oxide into the substrate. This current is referred to as gate leakage and is expressed as below:

$$I_{GATE} = B \cdot (\frac{V_{GB}}{T_{ox}})^2 \cdot (W \cdot L) \cdot e^{-\frac{T_{ox}}{V_{GB}} \cdot \alpha} \tag{4}$$

Where B and α are the fitting parameters, V_{GB} is the gate to substrate voltage and T_{OX} is the gate oxide thickness.

Considering I_{GATE} has an inverse exponential relationship with V_{GB}, it is less sensitive to RBB. What is more, gate leakage current issue can be overcome while maintaining excellent gate control by using high-k dielectric material. Therefore, when considering RBB adjustment to reduce leakage power, I_{GATE} can be ignored as in [2].

2.3 Band-to-band tunneling (BTBT)

In a high electric field (>10^6V/cm), there are electrons tunneling across the reverse biased PN junction of drain-substrate and source-substrate. If both n and p regions are heavily doped, the BTBT significantly increases and becomes a major contributor to the total leakage current, and the current is expressed as below:

$$I_{BTBT} = A \cdot J_s \cdot (1 - e^{-\frac{V_{RB}}{nkT/q}}) \tag{5}$$

Where A is the junction area, J_S is the maximum reverse saturation current density, n is the emission coefficient (usually set to 1), and V_{RB} is the reverse bias voltage across the junction. Compare with the high drain-substrate leakage, source-substrate leakage can be ignored.

The gate induced drain leakage (I_{GIDL}) is the current from drain to substrate caused by high electric field between gate and drain. This leakage mechanism becomes worse by high drain-to-body voltage and high drain-to-gate voltage. In this paper, I_{GIDL} is taken into account with I_{BTBT}. Since both currents are from drain to substrate, they are not easy to measure from the simulation results and they are all related to drain-to-body voltage. In a CMOS transistor, there also exists gate induced source leakage, but it is relatively small compare with I_{GIDL}, thus can be ignored in leakage analysis.

3. Optimal body biasing technique

From equations (2) (3) and (5), it can be seen that there exists an optimum RBB voltage to minimize the total standby leakage. I_{SUBTH} and I_{BTBT} have opposite dependence on body bias. As I_{GATE} is insensitive to body bias, the standby leakage is minimized at the RBB at which I_{SUBTH} and I_{BTBT} are approximately equal.

3.1 Prior Arts of leakage monitor

The ratio of I_{SUBTH} and I_{BTBT} is not easy to determine due to process variations and the complexity of calculating the electric field across the junction. In addition, the ratio varies with technology and doping profile [2]. Therefore, a leakage monitoring circuit to compare I_{SUBTH} and I_{BTBT} is the prerequisite to find the optimal RBB voltage. I_{SUBTH} and I_{BTBT} comparison circuits have been designed in [2][3] [9] and [10].

C.Neau [2] introduced a model to calculate$I_{SUBTH}/2 - I'_{SUBTH} - I_{DG}/2 - I_{GIDL}/2$. While ignorance of I_{GB} causes a minor error in leakage calculation, the drain-to-source voltage drop in PMOS current mirror also causes errors in mirroring leakage components in the approach. M.Nomura [3] developed a more precise model with consideration of I_{GB} and I_{DG} and maintaining the drain voltages of current mirrors with op-amps. However, the use of op-amp causes a voltage drop issue between the connected PMOS and NMOS on the current subtraction, which affects the mirror of the leakage currents as well. K.K.Kim [9] and H.Jeon [10] provided improved model, which separate I_{SUBTH} and I_{BTBT} by using current mirrors. However, the circuits are complicated and delicate to design, and the mismatch among current mirrors leads to erroneous results in leakage current calculation.

3.2 Proposed leakage comparator circuit

In this paper, a novel leakage current monitoring scheme is proposed. The proposed scheme compares the subthreshold and

the junction leakage by calculating the subtraction of I_{SUBTH} and I_{BTBT} to generate an optimum RBB at which the two leakage current components become equal. Figure 3 shows the circuit that generates leakage currents, compares them, and converts the subtraction of the currents into voltage signal.

The source and gate tied NMOS transistor N1 is in the "off" state and the leakage current through N_1 is leakage I1 and is given by $I_1 = (I_{SUBTH} + I_{DG} - I_{GB})$. Current through the drain of a gate-grounded "off" NMOS transistor N4 stacked on top of another NMOS transistor N5 is given by $I_2 = (I'_{SUBTH} + I_{DG} + I_{GIDL}) \approx (I_{DG} + I_{GIDL})$. Considering stack effect of N4 and N5, the subthreshold leakage I'_{SUBTH} through N4 is tremendously reduced by a factor of 10 compared with I_{SUBTH} of a single transistor and it can be even smaller in 65nm NMOS technology[6][7] with lower supply voltage. Therefore, ignoring the subthreshold current of N4 and N5, $I_1 = I_{SUBTH} + I_{DG} - I_{GB}$ is mirrored by N2, N3 and N6. An accurate current mirror is required as mentioned in [8] since the current level is quite low. In a similar way, $I_2 = I_{DG} + I_{GIDL}$ is mirrored by transistors P1, P2 and P3. And the difference between the current I1 and I2 provide a means to compare I_{SUBTH} vs. $I_{BTBT} = I_{GIDL} + I_{GB}$. The op-amp E2 with a feedback resistor R_f works converts $I_A = I_{BTBT} - I_{SUBTH}$ current to voltage signal V_A.

Level shifter using op-amp is used to adjust the voltage level of V_A and it generates V_A'. The use of level shifter makes the output voltage swing from zero to supply voltage.

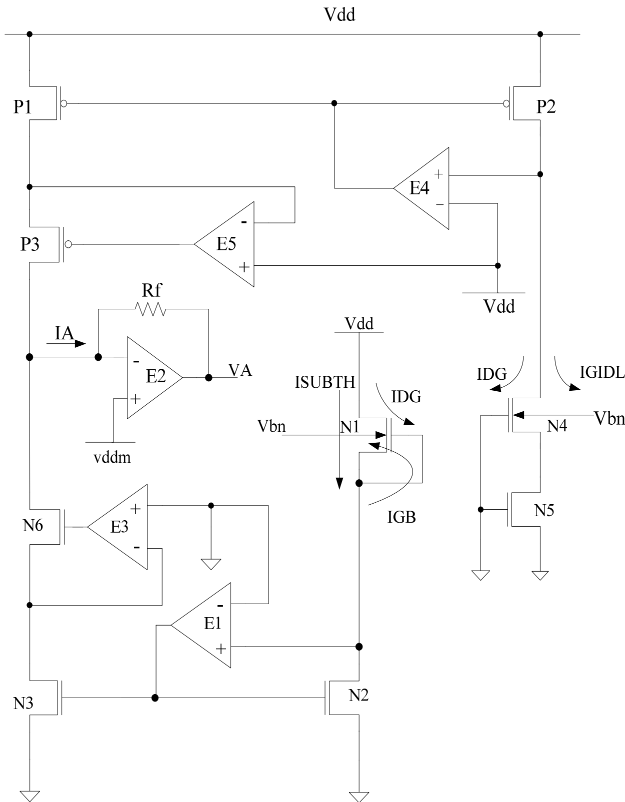

Figure 3 proposed leakage monitoring circuit

3.3 RBB regulator analysis

V_A drives gates of the two CMOS transistors P20 and N25. Figure 4 shows the circuit schematic of the charge pump and output stage of RBB. There are three operation modes for the gate inputs of P20 and N25:

(1) If $I_{SUBTH} > I_{BTBT}$, $I_A < 0$, $V_A > 0$, and N25 is turned on and capacitor Cc1 is discharging. Gate voltage of P22 decreases, drain current of P22 increases, and the absolute value of V_{bn} (|RBB|) increases. Increasing of |RBB| leads to decreasing of I_{SUBTH} and increasing of I_{BTBT}, which moves whole circuit toward mode (2).

(2) If $I_{SUBTH} = I_{BTBT}$, $I_A = 0$, $V_A = 0$, and P20 is slightly on, Cc1 will be charging slowly towards Vdd. Gate voltage of P_{22} increases slowly along with decreasing of drain current through P_{22}, and when voltage on Cc1 is greater than the threshold voltage of P22, P22will turn off and the absolute value of RBB voltage will decrease until a certain value. Then the voltage change through Cc1 is fixed and |RBB| is hold.

(3) If $I_{BTBT} > I_{SUBTH}$, $I_A > 0$, $V_A < 0$, and P_{20} is in the "on" state, Cc1 is charging towards Vdd. The gate voltage of P_{22} increases with its drain current decreasing, which drives |RBB| to decrease. And the decreasing of |RBB| leads to an increasing of I_{SUBTH} and decreasing of I_{BTBT}. The whole circuit will go back to mode (2)

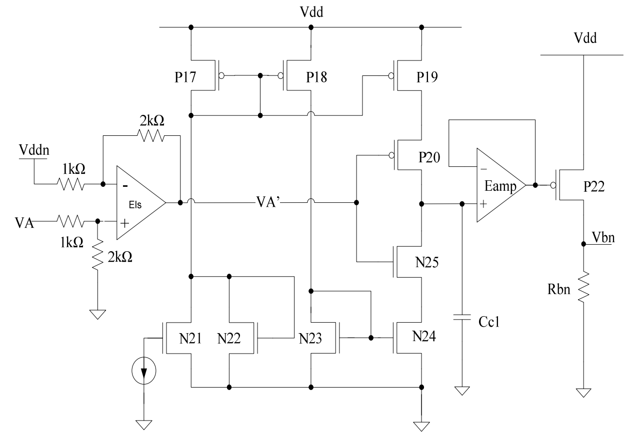

Figure 4 charge pump and output stage to generate RBB

From the above three modes, we can see that under the control of V_A, the output of V_{bn}(RBB) is continuously regulated through charging and discharging capacitor Cc1 in the charge pump until the optimal RBB is reached.

The implemented optimal RBB circuit accomplishes optimal RBB of NMOS transistors. In the exactly same way, an optimal RBB of PMOS transistor can be achieved as well.

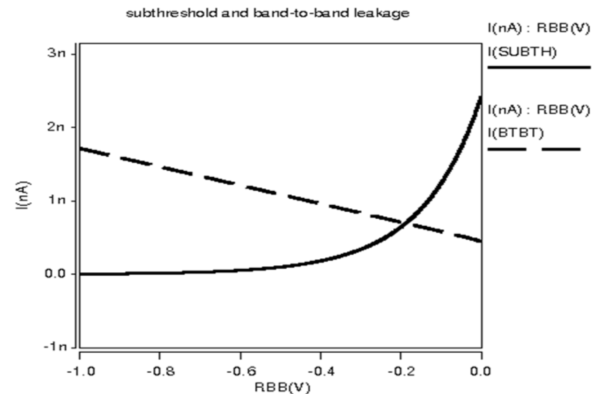

Figure 5 I_{SUBTH} and I_{BTBT} for single NMOS transistor in the standby mode with W/L=200nm/70nm at supply voltage of 1V and temperature of 25 ºC

4. Experiments and results

4.1 Experimental results

Figure 5 shows an optimal RBB when leakage of $I_{SUBTH}$and I_{BTBT} equals for single NMOS transistors in the standby mode. For NMOS transistor that has W/L=200nm/70nm, optimal RBB voltage is achieved at around -0.2V minimizing the total leakage currents.

Figure 6 shows simulation results of the proposed current monitoring circuit using 65nm bulk CMOS technology at the supply voltage of 0.8V and temperature of 25ºC. The W/L ratio of the NMOS transistors is 1μm/70nm. The standby mode NMOS transistors N1 and N4 have different leakage components as shown in Figure 3, and they are denoted as I1 and I2 as explained in Section 3.2. The subtraction of I1 from I2 is given by $I_{SUBTH} - I_{BTBT}$, and the zero value of $I_{SUBTH} - I_{BTBT}$ indicates the optimum RBB voltage point to minimize the total leakage current. As shown in Figure 6, the optimum RBB voltage turns out to be 0.37182V in the case.

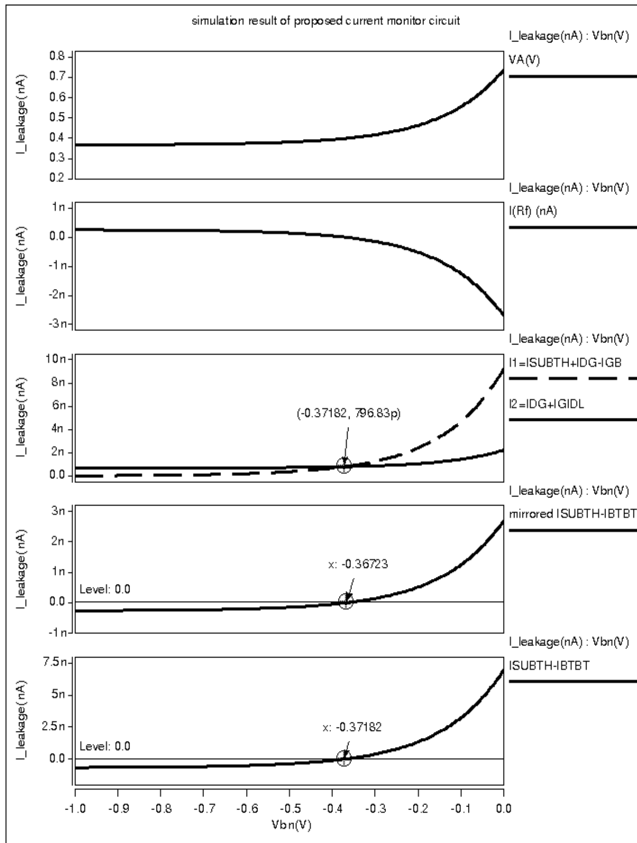

Figure 6 Simulation results of the proposed current monitoring circuit

The mirrored current through N_6 and P_3 form the current monitor and the subtraction of the two current (almost same as $I_{SUBTH} - I_{BTBT}$) reaches its zero value at the optimum RBB of 0.36723V, which is 1.2% error compared to $I_{SUBTH} - I_{BTBT}$ from N1 and N4. This result proved that the proposed current monitor circuit is precise enough to mirror the leakage components and perform the subtraction accurately. The total leakage current is 1.5937nA at the achieved optimal RBB at -0.372V compared with 11.46nA at zero body bias voltage, which demonstrates a significant reduction as much as 86% of the total leakage.

$I_{SUBTH} - I_{BTBT}$ flows through Rf and is converted to voltage signal. The top two curves in Figure 6 show the trend of the relationship between $I_{SUBTH} - I_{BTBT}$ and the corresponding voltage output signal VA.

4.2 VT variations of leakage current

Systematic and random variations in supply voltage and temperature caused leakage of low power circuits to vary significantly under design values and these variations are posing increasing challenge to nano-scale circuit design. The demand for low power causes supply voltage scaling, making voltage variations a significant design challenge. What is more, the quest for growth in operational frequency occurs at high junction temperatures and with die temperature variations. Sections below show how temperature and supply voltage changes affect optimal RBB in the proposed circuit.

4.2.1 Temperature variations with RBB

Temperature variations change the mobility of electrons and holes. An increase in operating temperature causes the mobility to decrease. From equation (2) and (3), with the increasing of T and decreasing of μ_0, I_{SUBTH} will decrease and the curve will be more flat. One the other hand, under high temperatures, electrons have more energy and the tunneling across the reverse biased pn junction of drain-substrate and source-substrate tunnels will be more easily, which results in an increasing of band tunneling current. Equation (5) well explained that, increasing of T leads to an increasing of I_{BTBT}, which makes the curve sharper. Therefore, the optimal RBB will decrease.

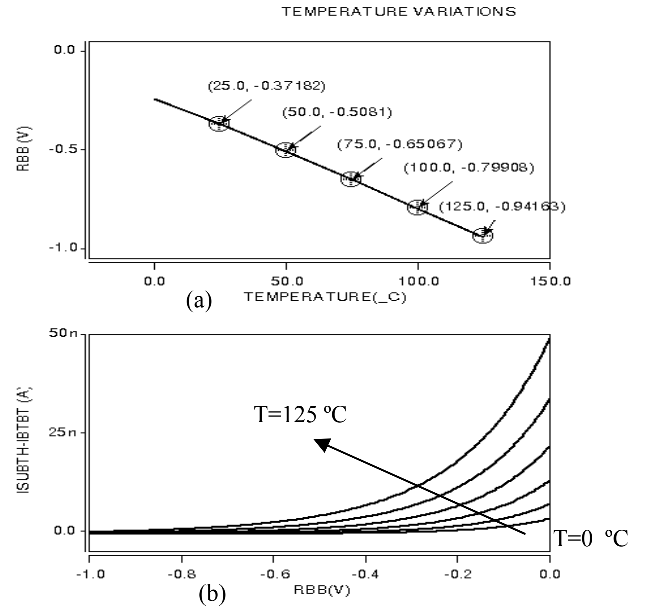

Figure 7 effects on temperature variations on leakage currents of proposed circuit

The above Figure 7 (b) shows the $I_{SUBTH} - I_{BTBT}$ curve at T ranging from 0 ºC to 125 ºC. Figure 7 (a) shows the corresponding RBB under temperature variations. We can tell that with T increasing, we need the substrate to be more biased in order to achieve less leakage.

4.2.2 Voltage variations with RBB

Large current consumption across long power lines with parasitic impedance causes varied, low and unstable voltage levels on the

power line. This variation results in uneven supply voltage distribution and temperature hot spots, across a die, causing transistor subthreshold leakage variation across the die. From Equation (2), increasing of VDD will result in increasing of I_{SUBTH}, making the curve more "curvy", and Equation (5) shows that I_{BTBT} will increase with increasing of VDD also, since the maximum reverse saturation current Js is a function of both the Electric field at the junction and the applied reverse bias. Therefore, the optimal RBB will decrease.

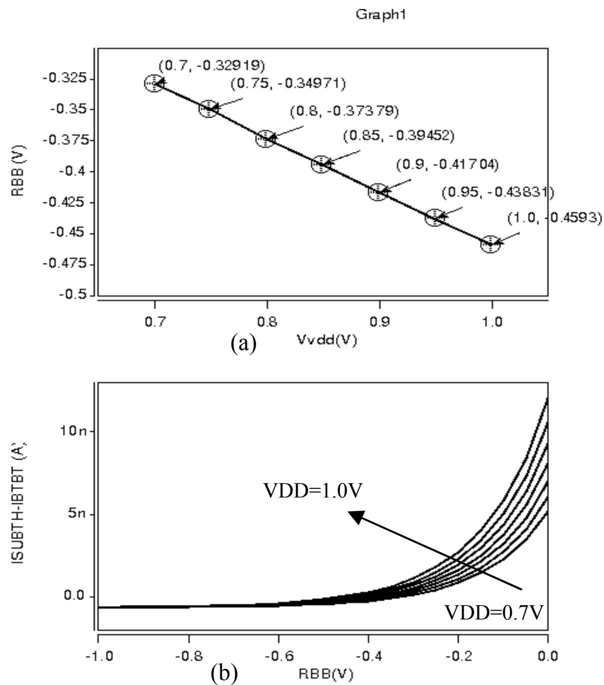

Figure 8 effects on supply voltage variations on leakage currents of proposed circuit

Figure 8 (b) above shows the $I_{SUBTH} - I_{BTBT}$ curve at VDD ranging from 0.7V to 1.0V. Figure 8 (a) shows the corresponding RBB under supply voltage variations. We can tell that with VDD increasing, we need the substrate to be more biased in order to achieve less leakage also.

5. Conclusion

As technology scaling goes down below 90nm, the standby leakage increase significantly. This makes the circuit design technique for minimizing leakage power more important. In this paper, a leakage monitoring circuit is proposed and designed to determine the optimal RBB by comparing leakage components of I_{SUBTH}, I_{BTBT} and I_{GATE}. It is possible to accomplish the minimum total leakage power during standby mode by monitoring the leakage current components. Using the information found in the monitoring circuits, an optimal body bias (RBB) voltage is found and applied to the substrate to accomplish the minimal leakage during standby state. The RBB is generated by the converted voltage from leakage current subtraction using charge pump. The voltage of the capacitor in the charge pump is held once the optimal RBB is reached. Otherwise, it keeps charging and discharging the capacitor to adaptively adjust RBB. The optimal RBB was achieved at -0.372V with a small in the test case in this paper. RBB also varies with supply voltage and temperature, with the increasing of supply voltage and/or temperature; we need more negative biased RBB to achieve leakage reduction. The result shows that it is possible to reduce total leakage significantly as much as 86% of the total leakage using the proposed algorithm. This research can be a good reference for the future research in leakage minimization.

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