

## Research Article

# A Low-Power Digitally Controlled Oscillator for All Digital Phase-Locked Loops

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Received 31 May 2009; Accepted 20 October 2009

Academic Editor: Gregory D. Peterson

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A low-power and low-jitter 12-bit CMOS digitally controlled oscillator (DCO) design is presented. The Low-Power CMOS DCO is designed based on the ring oscillator implemented with Schmitt trigger inverters. The proposed DCO circuit uses control codes of thermometer type to reduce jitters. Performance of the DCO is verified through a novel All Digital Phase-Locked Loop (ADPLL) designed with a unique lock-in process by employing a time-to-digital converter, where both the frequency of the reference clock and the delay between DCO\_output and DCO\_clock is measured. A carefully designed reset process reduces the phase acquisition process to two cycles. The ADPLL was implemented using the 32 nm Predictive Technology Model (PTM) at 0.9 V supply voltage, and the simulation results show that the proposed ADPLL achieves 10 and 2 reference cycles of frequency and phase acquisitions, respectively, at 700 MHz with less than 67 ps peak-to-peak jitter. The DCO consumes 2.2 mW at 650 MHz with 0.9 V power supply.

## 1. Introduction

Phase-locked loops are widely used in many communication systems for clock and data recovery or frequency synthesis [1–5]. Cellular phones, computers, televisions, radios, and motor speed controllers are just a few examples that rely on PLLs for proper operation. With such a broad range of applications, PLLs have been extensively studied in literature.

The conventional PLLs are often designed using analog approaches. However, analog PLLs have to overcome the digital switch noise coupled with power through power supply as well as substrate-induced noise. In addition, the analog PLL is very sensitive to process parameters and must be redesigned if the process is changed or migrates to next generation process. Although many approaches have been developed to improve the jitter performance, it often results in long lock-in time and increasing design complexity. With the increasing performance and decreasing cost of digital VLSI design technology, all digital phase-locked loops have become more attractive. Although ADPLL will not have the same performance as its analog counterpart, it provides a faster lock-in time and better

testability, stability, and portability over difference process [6, 7].

The controlled oscillator is a key component in PLL, which is a replacement of the conventional voltage or current controlled oscillator in the fully digital PLLs. They are more flexible and usually more robust than the conventional VCO. Furthermore, the design compromise for the frequency gain in voltage or current controlled oscillator is not necessary in DCOs because the immunity of their control input is very high. There are two main techniques for the DCO design as shown in Figure 1. One technique changes the driving strength dynamically using the fixed capacitance loading [8, 9] while the other uses shunt capacitor technique to tune the capacitance loading [10]. Although both of the approaches have a good linear frequency response and a reasonable frequency operating range, the power dissipation has not been taken into consideration. Moreover, for the DCO design, there is a tradeoff between the operating range and the maximum frequency that DCO can achieve. As a result, the increase of the operating range by adding more capacitance loading will result in a lower maximum frequency and higher power consumption. Since power

consumption is of extreme concern for portable battery-charged computing systems, the reduction of the power consumption has become a major concern in modern electronic systems.

This paper proposes a novel DCO circuit with significantly reduced power consumption using binary controlled pass transistors and Schmitt trigger inverters. The functionality and performance are verified through a novel ADPLL that uses the proposed DCO. Usually the ADPLL structure based on the second order negative feedback system has a faster lock-in time with a limited lock-in range [11, 12]. One the other hand, by separating the locking process into frequency and phase acquisition, a wide lock-in range is available [13, 14]. However, it takes more time due to the blind “ahead” or “behind” comparison as well as the extra phase acquisition process. In this paper, the new ADPLL also uses a separated frequency and phase lock-in process. Instead of “ahead” or “behind” comparison, a time-to-digital converter is used to measure the frequency difference accurately, which greatly reduces the lock-in time. The phase acquisition only takes two reference clocks. In the first cycle, the DCO is reset by the reference clock considering the delay between DCO\_output and DCO\_clock. In the second cycle, the DCO frequency changes back to the reference clock by updating the control bits. The ADPLL with the proposed DCO was implemented using a 0.9 V 32 nm practical transistor model.

## 2. DCO Principle and Design

*2.1. DCO Principle.* DCO should generate an oscillation period of  $T_{DCO}$ , which is a function of digital input word  $D$  and given by

$$T_{DCO} = f(d_{n-1}2^{n-1} + d_{n-2}2^{n-2} + \dots + d_12^1 + d_02^0). \quad (1)$$

Typically, the DCO transfer function is defined such that the period of oscillation  $T_{DCO}$  is linearly proportional to  $D$  with an offset. Therefore, the oscillation period is rewritten as

$$T_{DCO} = T_{offset} - D \cdot T_{step}, \quad D : \text{Digital Control Bits}, \quad (2)$$

where  $T_{offset}$  is a constant offset period and  $T_{step}$  is the period of the quantization step. For the conventional driving strength-controlled DCO shown in Figure 2, the constant delay of each cell is calculated as follows:

$$T_{constant} = R_1(C_1 + C_2) + R_2C_2, \quad (3)$$

$$R_{1,2} \propto 1/W_{1,2}, \quad (4)$$

where  $R_1$  and  $R_2$  are the equivalent resistances of  $M1$  and  $M1'$  and  $C_1$  and  $C_2$  are the total capacitances at the drain of  $M1$  and  $M1'$ , respectively, which mainly consist of drain to body and source to body capacitances. Assuming that they have the

same driving strength, the delay tuning range of this standard cell is obtained as follows:

$$\frac{T_{tune}}{2} = (C_1 + C_2) \left( R_1 // \frac{\Delta R}{d_0} // \frac{\Delta R}{d_1 2} // \dots // \frac{\Delta R}{d_{n-1} 2^{n-1}} \right) - (C_1 + C_2) R_1 \quad (5)$$

$$= \frac{R_1(C_1 + C_2)}{1 + (D \cdot \Delta W)/W_1} - (C_1 + C_2) R_1 \quad (6)$$

$$\approx R_1(C_1 + C_2) \frac{D \cdot \Delta W}{W_1}, \quad \left( \text{Only if } \frac{D \cdot \Delta W}{W_1} \ll 1 \right). \quad (7)$$

In order to have a good linear tuning range, the width of the transistor  $M1$  has to be increased as illustrated in (7). Consequently the equivalent resistance  $R1$  will decrease, resulting in a smaller delay tuning range. One way to increase the tuning range while keeping the linear response is to increase the capacitance loading. However, this will minimize the maximum frequency that the DCO can accomplish and the power consumption will also be increased.

*2.2. Proposed DCO Design.* The proposed DCO employs a new approach to increase the delay tuning range using digitally controlled pass transistor arrays and Schmitt trigger-based inverters [15]. The Schmitt trigger-based inverter has a higher  $VM+$  (low-to-high switching threshold) and lower  $VM-$  (high-to-low switching threshold) compared to the conventional inverters as shown in Figure 3. As a result, the proposed DCO circuit provides the same tuning range with a smaller capacitance loading, which is beneficial for power consumption reduction. Moreover, in the conventional DCO circuit, the slope of the input signal to each stage decreases gradually due to the large delay between each stage. This results in not only a nonideal rail-to-rail switch but also a poor power performance. The steep slope of the output signal from the Schmitt trigger-based inverter minimizes this problem to a certain extent.

The circuit diagrams of the conventional DCO and proposed DCO are shown in Figure 4. The conventional DCO consists of two identical binary controlled coarse cells as well as a similar fine cell with smaller tuning range. The proposed DCO also consists of two coarse cells and a fine cell. The coarse cells have tuning codes of 2 bits with PMOS array or NMOS array in form of thermometer code, which could provide a better duty cycle performance and linearity. The fine cell has tuning codes of 6 bits by only NMOS array in the form of thermometer code as shown in Figure 4(c). The thermometer code minimizes the jitters. Since they are grouped per 2 bits, the circuit to convert binary code to thermometer code is also minimized.

*2.3. Improved Structure with Larger Operating Range.* The binary controlled DCO structure has a limited linear operating range as discussed above. In this paper, three-stage constant delay chains and a 4 : 1 Mux are used to increase the operating range, and the three-stage constant delay is tuned by the fixed code such that each stage provides an accurate

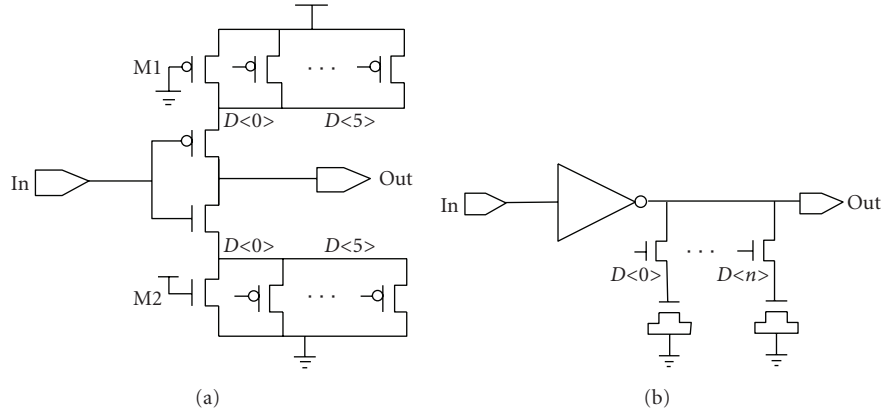


FIGURE 1: Standard cell of digitally controlled oscillator. (a) Driving strength controlled. (b) Shunt capacitance controlled.

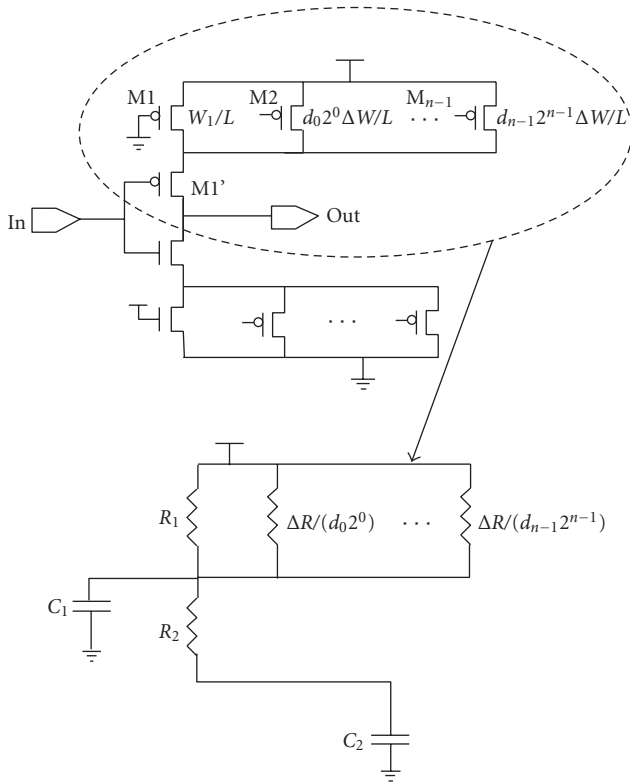


FIGURE 2: Equivalent circuit for the calculation of constant delay and delay tuning range.

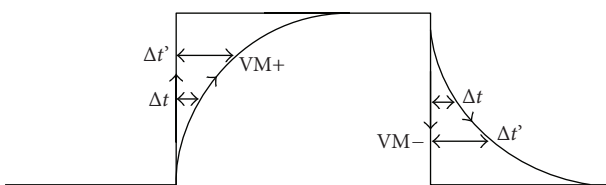


FIGURE 3: Delay comparison of Schmitt inverter and conventional inverter.

TABLE 1: Impact of each control bit on the DCO period

Control Bits	THE CONVENTIONAL DCO		THE PROPOSED DCO	
	Period (ns)	Delta (ps)	Period (ns)	Delta (ps)
111111	1.8022	257.7	1.7918	270.6
100000	1.5445	134.6	1.5212	139
010000	1.4099	69.8	1.3822	70.8
001000	1.3401	34.4	1.3114	36.8
000100	1.3057	19.8	1.2746	19.1
000010	1.2859	9.1	1.2555	9.4
000001	1.2768	9.2	1.2461	8.5
000000	1.2676	—	1.2376	—

delay as shown in Figure 5. As a result, the operating range can be four times larger compared to the original design.

2.4. Comparison between the Two DCO Structures. The proposed DCO and the conventional DCO are simulated and compared using 32 nm CMOS PTM (Predictive Technology Model) with a supply voltage of 0.9 Volts. The choice of 12 bits is a compromise between the DCO resolution, operating range and circuit complexity.

Table 1 shows the impact of each control bit on the period of the two DCO structures. Both structures have the same linear tuning range. Since the two DCO structure-have the same operating ranges, it is more reasonable for us to compare their power consumption.

Compared to the conventional DCO, the proposed DCO saves approximately 40% power consumption as shown in Figure 6. As discussed above, this reduction is due to the comparatively smaller capacitance loading for the Schmitt trigger-based inverter than the conventional inverter at the same operating frequency. The proposed DCO is significantly more power efficient than the conventional DCO. However, this DCO design has a limited operating frequency range, which is improved in this paper by employing the fixed delay blocks shown in Figure 5.

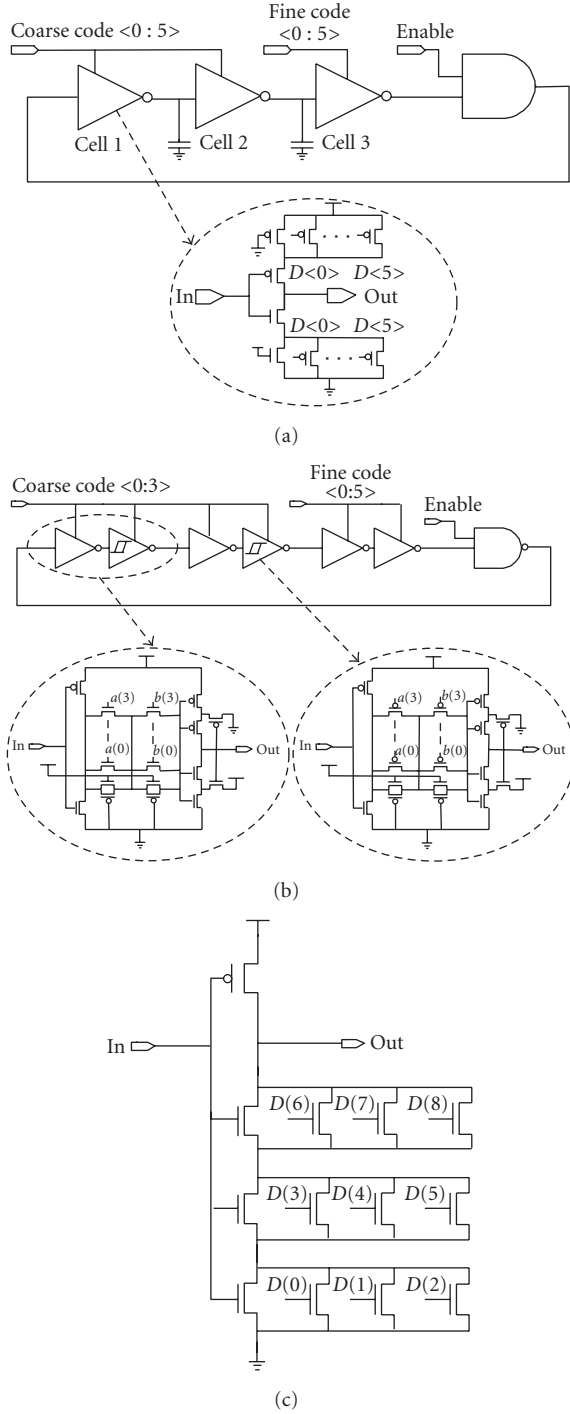


FIGURE 4: Digitally controlled oscillator. (a) conventional DCO structure. (b) Proposed DCO structure. (c) Fine delay cell.

**2.5. Simulation Result of the Proposed DCO.** The proposed DCO structure with increased operating range is designed and simulated using 32 nm PTM model. Figure 7 shows operating frequency ranges of the coarse and fine tuning frequency of the novel DCO. The curves have good monotonousness, which is a key factor in PLL performance. The frequency ranges are about 570 MHz ~ 800 MHz at

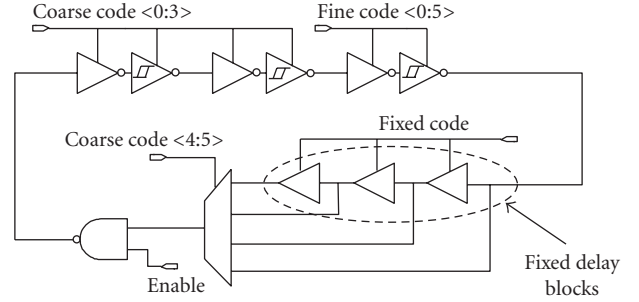


FIGURE 5: The proposed DCO structure with increased operating range.

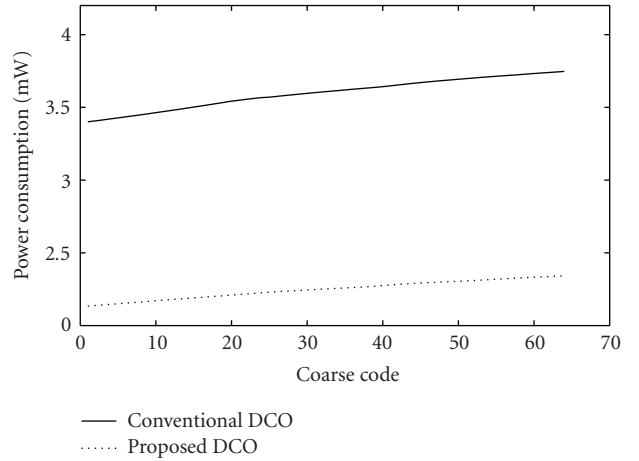


FIGURE 6: Power consumption of the conventional and the proposed DCO structures.

TABLE 2: Impact of each control bit on the DCO Period.

Items	Coarse Delay	Fine Delay
Resolution	6 bit	6 bit
Max. DCO Gain	10 ps	1 ps
Avg. DCO Gain	7 ps	0.7 ps
Operation Range	570 MHz~800 MHz	
Power Consumption	2.2 mW @ 650 MHz	

the condition of 0.9V supply voltage at 25°C and the delay range of the fine delay chain is about 45 ps. The characteristics of the proposed DCO are summarized at Table 2.

The operational frequency response to the process, temperature, and voltage variation is shown in Figure 8. The curves show the normalized data with respect to the center frequency. Figure 8 shows that the relative delay per code is almost same regardless of the process, temperature, and voltage variations. In other words, the proposed DCO design is very robust to PVT variations.

Table 3 shows the measurement results to compare with a few recent state-of-the-art DCO designs [6, 10, 16, 17]. The proposed DCO achieves the finest LSB resolution and

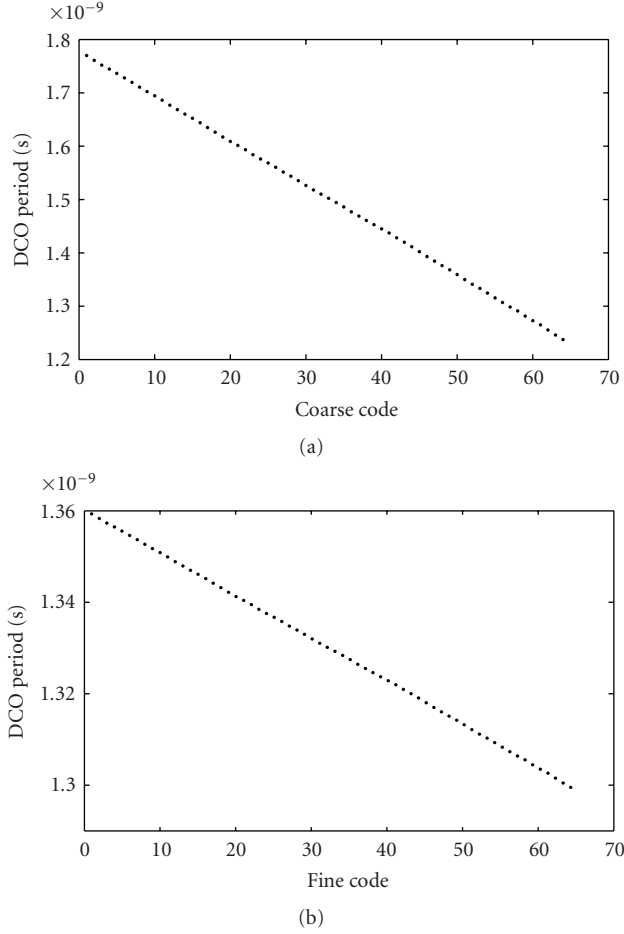


FIGURE 7: Operating range of the proposed DCO: (a) coarse loop and (b) fine loop.

the highest operating frequency. In addition, the proposed DCO consumes less power than others.

### 3. Performance Verification of the Proposed DCO

In this section, performance of the proposed DCO is verified through a novel ADPLL with the proposed DCO circuit. The proposed ADPLL is designed with a unique lock-in process based on the good monotonousness of the DCO.

**3.1. ADPLL Architecture Overview.** The block structure of the new ADPLL is shown in Figure 9. The control word corresponding to the period of the reference clock  $T_{ref}$  is stored in register1. In register 2, the control word corresponds to a new period of  $T_{ref} - T_{delay}$ , which is the period of reference clock subtracted by the delay between DCO\_output and DCO\_clock. Unlike the conventional ADPLL designs, the clock signals to all the logical blocks are generated from the DCO\_output.

Phase lock begins with frequency acquisition. In this mode, a time-to-digital converter measures the time difference between the reference clock and the DCO\_clock.

As shown in Figure 10(a), it converts time difference into the digital word  $T_1$  and  $T_2$ , which are the time difference between DCO\_clock's rising edge and the reference clock's rising and falling edges, respectively. As a result, the frequency (period) difference can be defined as follows:

$$\Delta T = (T_1 - T_1') + \frac{(N - 2)T}{2}, \quad (8)$$

$$T = 2(T_2 - T_1). \quad (9)$$

$N$  represents the reference clock's low-to-high or high-to-low transition number during one DCO\_clock period from the 4-bit counter.  $T_1'$  is the stored value of  $T_1$  in the previous DCO period.

Compared to other frequency acquisition approaches, the DCO does not have to be reset at the beginning of every reference cycle for the initial phase alignment, which reduces the design complexity. Moreover, the frequency acquisition process can be reduced to less than ten cycles if the DCO has a good linearity performance. However, as shown in Figure 10(b), due to the nonzero setup time, the last transition of the reference clock may be ignored if the time difference  $T_1'$  is smaller than the register's setup time, which will result in an incorrect transition number  $N$ . The improved integer counter, which is designed to address this problem, will be discussed in the circuit design part.

The ADPLL in this paper starts with frequency and phase acquisition followed by maintenance mode. Once the frequency and phase are acquired using the coarse code, the acquired frequency and phase are maintained by updating the fine codes to correct the phase and frequency drift due to noises.

During the frequency acquisition mode, the coarse control bits are generated by the algorithm (arithmetic) blocks in Figure 9 and applied to the DCO. Since the DCO has a good linearity, this acquisition process takes fewer reference cycles compared to the previous blind fast or slow comparison. When the frequency is locked, the control bits are stored in the coarse bit register and the lock-in process is switched from the frequency acquisition to the phase acquisition process by the state machine.

In the phase acquisition, the DCO\_clock edge will be aligned to the reference clock edge. In reality, there are several stages of logic separating DCO\_output and DCO\_clock such as the duty-cycle corrector shown in Figure 9. As a result, the DCO\_clock edge cannot be aligned to the reference clock by a simple reset process as shown in Figure 11. The delay time  $T_{Delay}$  results from the logic blocks between the DCO\_output and the DCO\_clock.

A phase acquisition process is required to get the phase aligned, which is usually done by comparing the phase position of the two signals. The adjustment on the control word is made based on the "behind" or "ahead" signal until there is a polarity change. However, such kind of acquisition process takes many cycles, which results in a slow lock-in process.

A novel reset process is presented in this paper, which is able to reduce the phase lock process to two cycles as shown in Figure 12. In the first cycle, the DCO is still

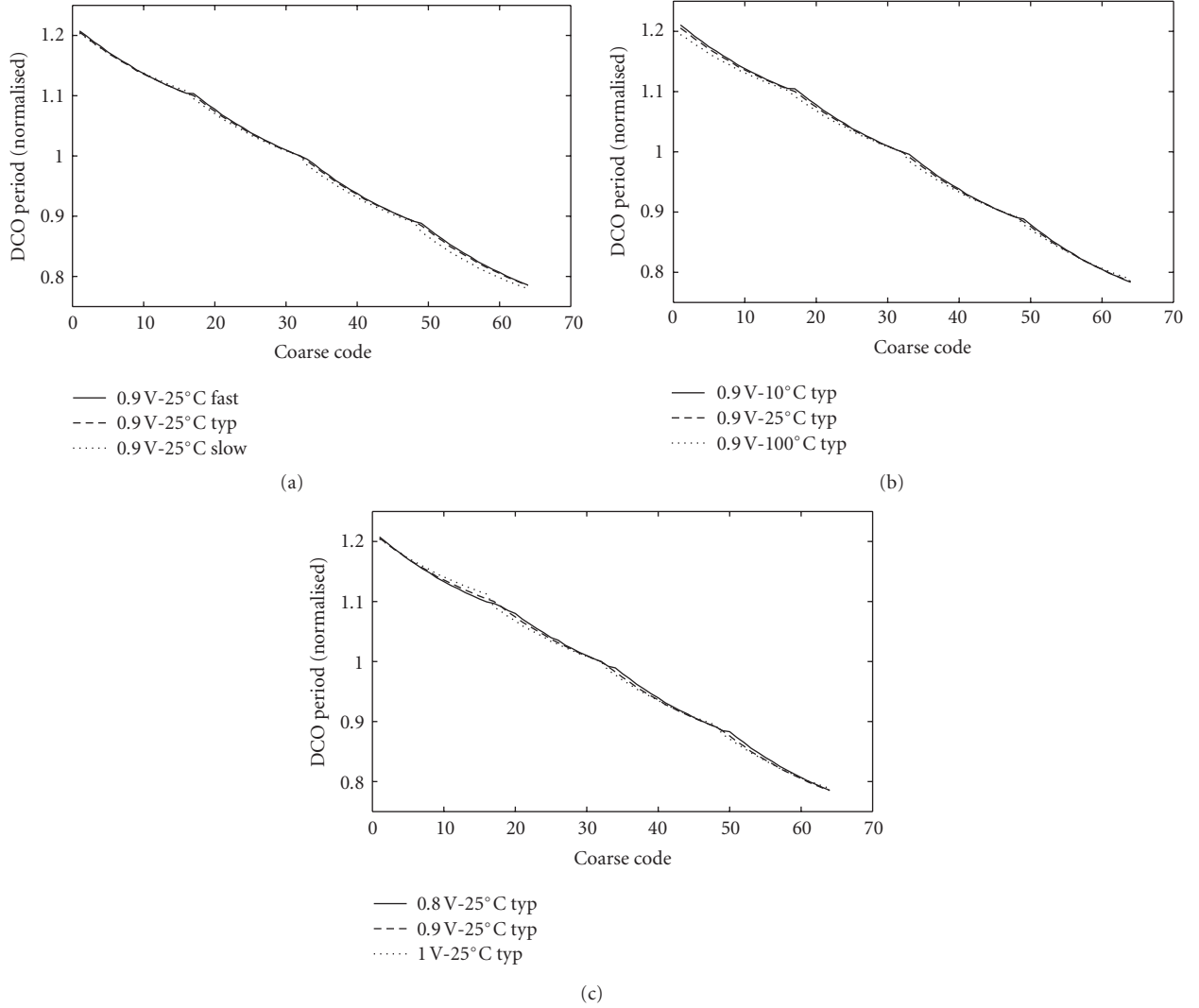


FIGURE 8: Delay characteristics of the coarse loop for the Process, Voltage, and Temperature variations. (a) Process variation. (b) Temperature Variation. (c) Voltage Variation.

TABLE 3: Comparison with existing DCOs.

Function	Proposed	Items			
		TCAS-II' 05 [16]	ISQED' 02 [10]	ISSCC' 03 [17]	JSSC' 03 [6]
Process	32 nm @ 0.9 V	0.35 $\mu$ m @ 3.3 V	0.13 $\mu$ m @ 1.65 V	0.6 $\mu$ m @ 5 V	0.35 $\mu$ m @ 3.3 V
DCO control word length	12 bits	15 bits	8 bits	10 bits	12 bits
LSB Resolution	1 ps	1.55 ps	40 ps	10 ps	5 ps
DCO output frequency	570 ~ 800 (MHz)	18 ~ 214 (MHz)	150 (MHz)	10 ~ 12.5 (MHz)	45 ~ 450 (MHz)
Power Consumption	2.2 mW @ 650 MHz	18 mW @ 200 MHz	1 mW @ 150 MHz	164 mW @ 100 MHz	100 mW @ 450 MHz

reset by reference clock with control word corresponding to  $T_{\text{ref}} - T_{\text{Delay}}$ . The control word is found in a similar way as mentioned in the frequency acquisition:

$$\Delta T = (T_1 - T'_1) + \frac{(N-2)T}{2} + T_{\text{Delay}}. \quad (10)$$

Without the delay, the second rising edge will lead the reference clock by  $T_{\text{Delay}}$  such as the DCO\_output. However, as for the DCO\_clock signal, this can be compensated by the existing delay  $T_{\text{Delay}}$  and the second rising edge will be aligned to the reference clock. In the second cycle, the control word in the register1 will be reloaded and DCO frequency will be the same as reference clock again.

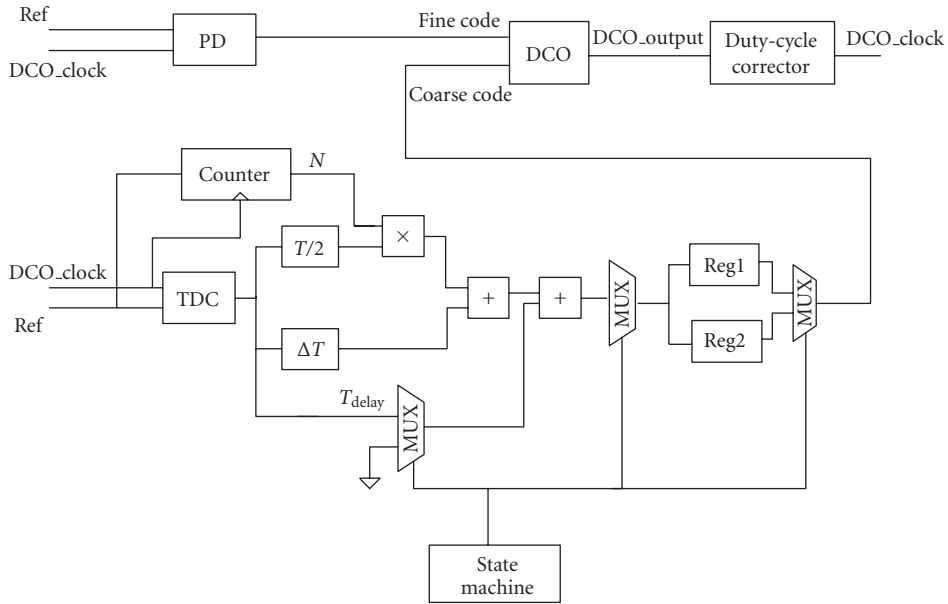


FIGURE 9: Block diagram of an ADPLL using the proposed DCO.

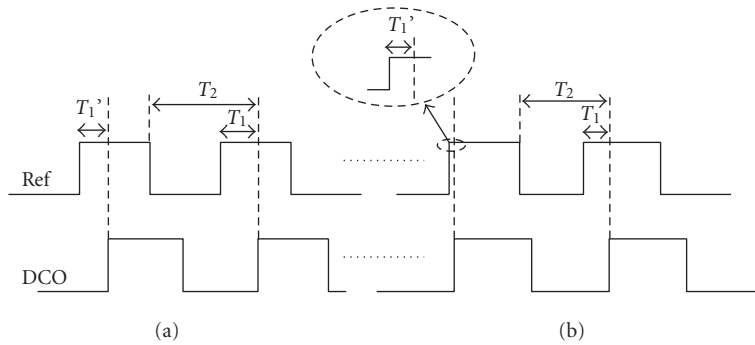


FIGURE 10: Principle of frequency acquisition.

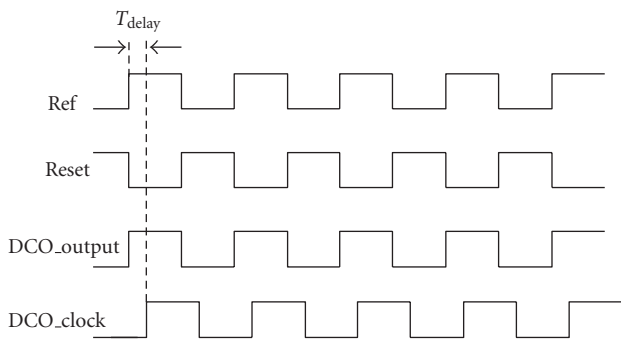


FIGURE 11: Failure in phase alignment due to logic blocks between DCO\_clock and DCO\_output.

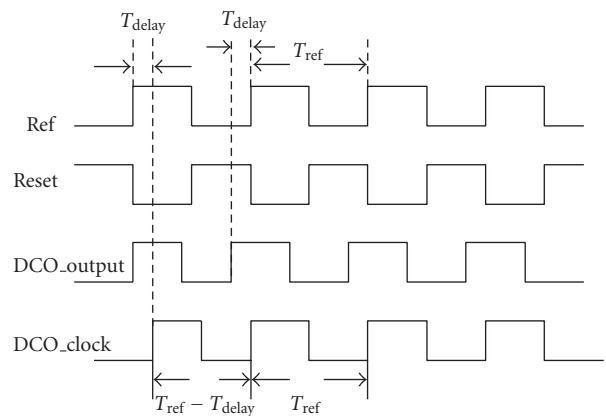


FIGURE 12: A new phase acquisition process with two lock-in cycles.

After the phase acquisition, a maintenance mode is applied to preserve the phase alignment of the DCO\_clock relative to reference clock. The phase detector generates “ahead” or “behind” signal based on the rising edges of

the reference clock and DCO\_clock. The ADPLL increments or decrements the control word every cycle. The magnitude of the change, which is the value held in the phase-gain

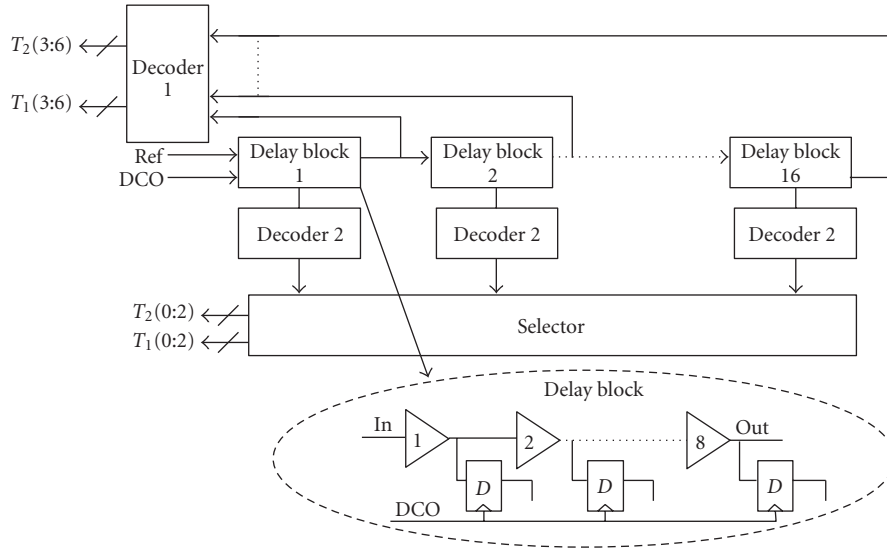


FIGURE 13: Block diagram of fractional TDC structure.

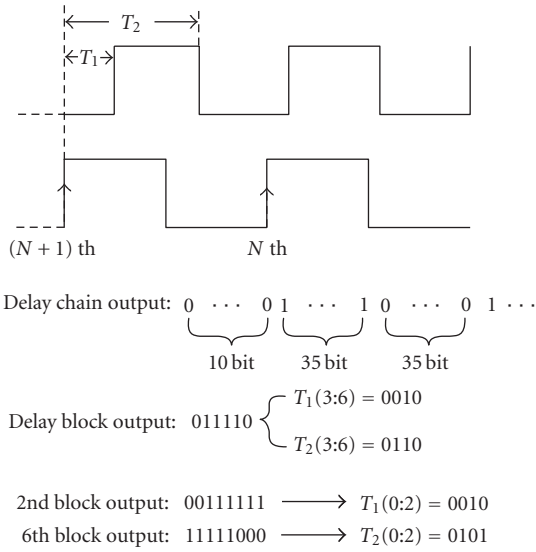


FIGURE 14: Decoding process of the TDC.

TABLE 4: Impact of each control bit on the DCO period.

Status	Function
“000”	Fine the control word for $T = T_{ref}$
“001”	Reset DCO in order to find the delay value $T_{Delay}$
“010”	Find a new control word for $T = T_{ref} - T_{Delay}$
“011”	Reset DCO in order for the phase alignment
“100”	Maintenance Mode

register, is shifted to the left by one bit every cycle. When the polarity changes, the control word and the phase gain will be reset to the initial value stored during the frequency acquisition. The edge detector keeps comparing the phase difference and updating the fine control bits in order to maintain the phase lock. The fine resolution of the DCO as well as the bit shift strategy provides a fast phase lock-in time and better jitter performance.

### 3.2. Circuit Designs.

#### (1) Time-To-Digital Converter.

The TDC used in this paper is composed of two parts: an integer counter that counts the reference clock edges within one DCO clock period and a fractional counter that quantizes the residual phase difference, which helps to improve the resolution of the proposed TDC.

The block diagram of the fractional TDC structure is shown in Figure 13. It consists of 16 delay blocks and two types of independent decoders. The resolution of the TDC is the delay of a single buffer, which minimizes the delay mismatch compared to the delay of a single inverter. The reference clock waveform propagates through a chain of  $8 \times 16$  delay elements whose outputs are sampled by  $8 \times 16$  flip-flops at the rising edge of each DCO\_clock.

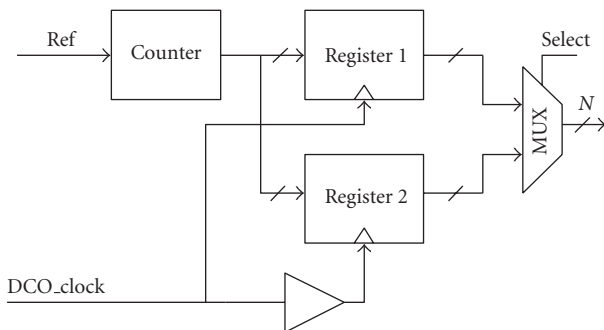


FIGURE 15: Block diagram of the integer counter.

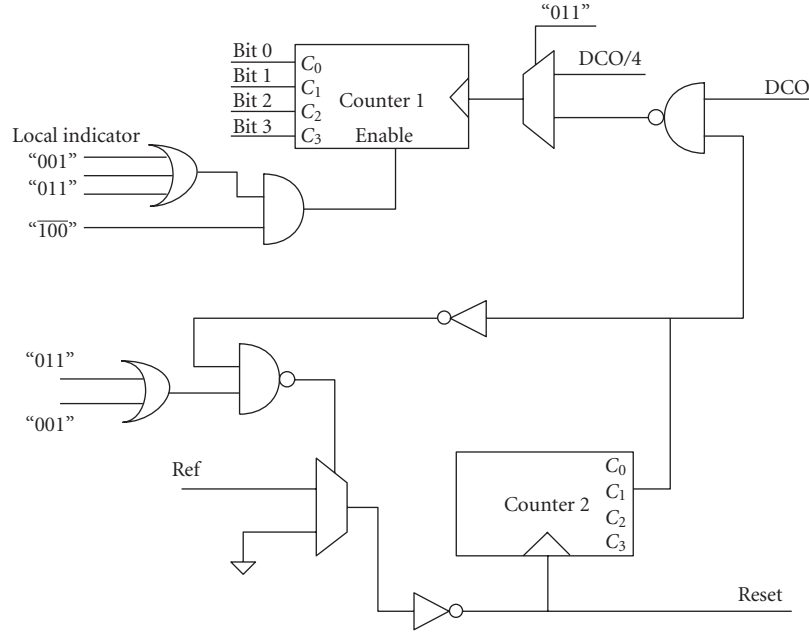


FIGURE 16: Block diagram of the state machine.

TABLE 5: Comparison on between conventional ADPLL and proposed ADPLL

Items	Proposed ADPLL	Approaches	
		Conventional ADPLL [11]	Conventional ADPLL [13]
Acquisition Time	10 cycles	18 cycles	50 cycles
Operation frequency range	570 MHz ~ 800 MHz	152 MHz ~ 366 MHz	50 MHz ~ 500 MHz
Lock-in range	Unlimited	Limited	Unlimited
Jitter	67 ps	150 ps	125 ps
Power consumption	19 mW @ 700 MHz	8.1–24 mW	40 mW @ 100 MHz

The decoding process is shown in Figure 14. The 16 bit output of the delay block is decoded into the higher 4 bits of  $T_1$  and  $T_2$ . At the same time, the 8 bit output of each delay block is also decoded into a series of lower 3 bits of  $T_1$  and  $T_2$ . Based on the output of decoder1, the proper set of  $T_1$  (0 : 2) and  $T_2$  (0 : 2) is selected. As is shown in Figure 14, the transition takes place in the 2nd and 6th blocks. As a result, the decoded output of those two blocks is selected as the lower 3 bits of  $T_1$  and  $T_2$ . The separation of the decoder into two parts has greatly reduced the design complexity.

### (2) Integer Counter.

As mentioned above, the nonideal setup time may result in an incorrect transition number  $N$  if  $T_1$  is less than the setup time. The proposed integer counter that is designed to solve this problem is shown in Figure 15.

Using a delay buffer in the clock path, register2 is able to detect the closest rising edge of the reference clock while register1 cannot. The selected signal is the XOR output of the first delay block. When the rising edge of DCO\_clock is slightly behind the edge of the reference clock, the transition will take place in the first delay block. As a result, the XOR output of this delay block will generate a logic high signal and the output of register2 will be selected. Apparently, when

DCO\_clock edge is slight ahead or  $T_1$  is large enough, the XOR output of delay block 1 is logic low and the output of register1 is selected. This eliminates another possible error that register2 may store value of  $N + 1$  instead of  $N$  when DCO\_clock edge is slight ahead of reference clock edge.

### (3) State Machine.

The state machine is the control unit of the proposed ADPLL, and it has five different kinds of working status as shown in Table 4. It takes the reference clock and DCO output as the input signals, and it outputs four-bit state signals such as bit0, bit1, bit2, and bit3 as well as a DCO reset signal as shown in Figure 16.

In the initial "000" status, the control word corresponding to  $T_{ref}$  is stored in register1. After that the lock indicator generates a high-voltage signal and ADPLL switches to "001" status. The delay between DCO\_output and DCO\_clock  $T_{Delay}$  will be measured by resetting the DCO using reference clock. Counter2 is used to make sure that the reset process only takes two cycles and it will be cleared after that. In "010" status, a new control word corresponding to  $T_{ref} - T_{Delay}$  is stored in register2 and the corresponding lock indicates that signal will switch the status to "011". Then, the reset process will restart again with the control word corresponding to

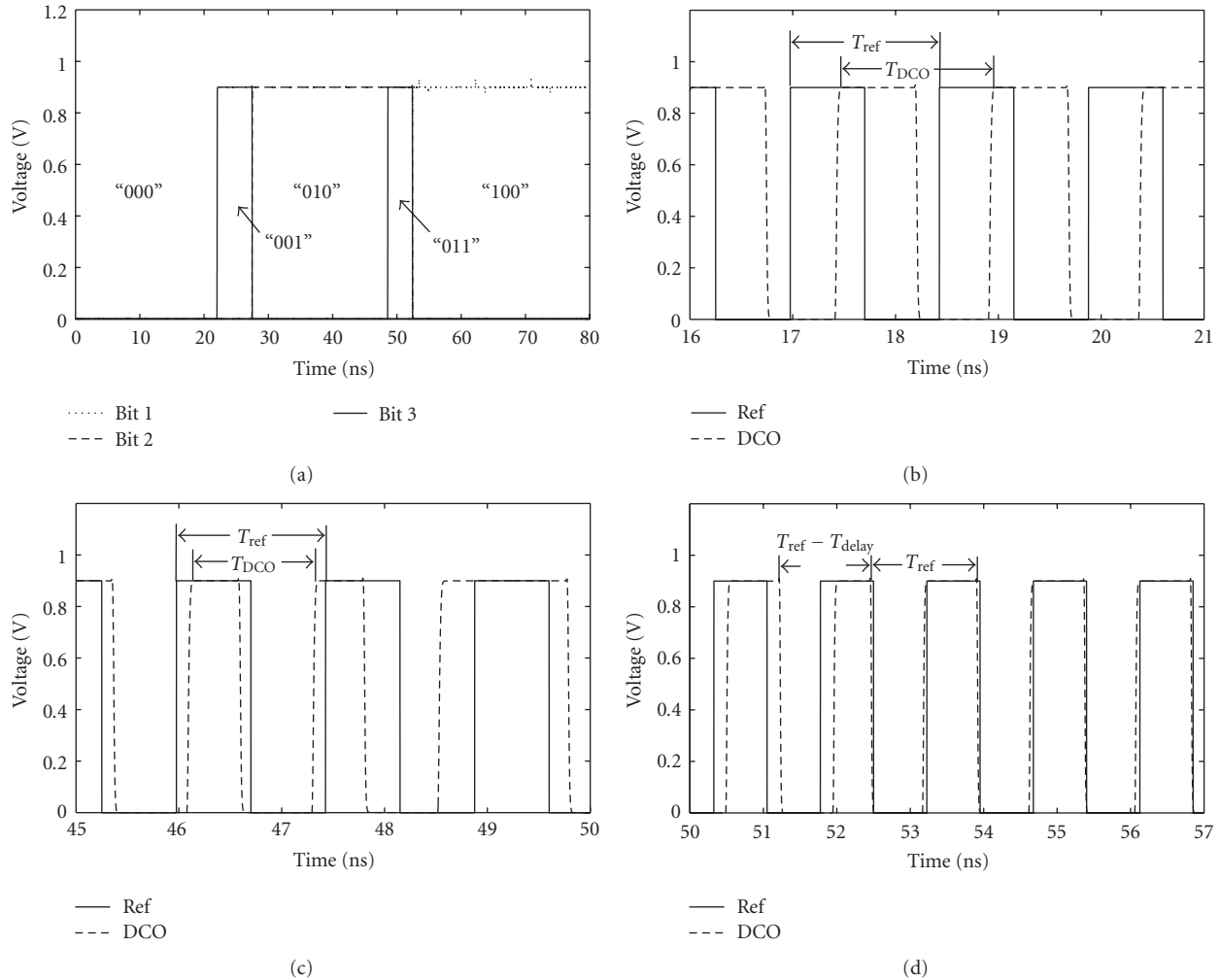


FIGURE 17: Lock-in process of the proposed ADPLL. (a) Lock process of the ADPLL with five different kinds of status from “000” status to “100” status. (b) Frequency acquisition at  $T_{DCO} = T_{Ref}$  during “000” status, (c) Frequency acquisition at  $T_{DCO} = T_{Ref} - T_{Delay}$  during “010” status, (d) Phase acquisition process during “011” status.

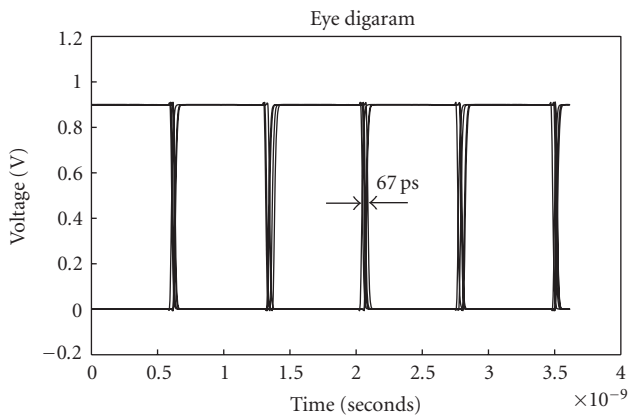


FIGURE 18: Output clock jitter (DCO @ 700 MHz)

$T_{ref} - T_{Delay}$  and  $T_{ref}$  in the first two cycles, respectively. After that, the ADPLL goes into the maintenance mode and

the state machine will be locked. The five consecutive kinds of status ensure a fast lock-in and low-jitter ADPLL design.

#### 4. Simulation Results of the ADPLL with the Proposed DCO

The proposed APDLL structure is designed and simulated using a 32 nm CMOS Predictive Transistor Model. The resolution of the TDC, which is the delay of a single buffer used in the delay chain, is 20 ps. The 12-bit digitally controlled oscillator has a coarse resolution close to 10 ps and fine resolution close to 1 ps with a tuning range from 570 MHz to 800 MHz.

The lock-in process of the proposed ADPLL is illustrated in Figure 17 when locking to 700 MHz. The output of the state machine ensures five consecutive kinds of status during the lock-in process as shown in Figure 17(a). Two-frequency lock-in processes are completed during “000” status and “010” status, respectively, and the corresponding control

words are stored in registers 1 and 2 as shown in Figures 17(b) and 17(c). The phase lock-in process takes 2 clock cycles, as in Figure 17(d). As a result, the whole lock-in process takes about ten reference cycles and phase acquisition process takes two cycles.

Figure 18 shows an eye diagram to show the DCO jitter performance during the maintenance mode after acquisition. As shown in the figure, this ADPLL achieves a peak-to-peak jitter of 67 ps at 700 MHz with the power supply of 0.9 V. Table 5 shows a comparison of the proposed ADPLL with the conventional ADPLL in items of acquisition time, jitter, operation frequency, power consumption, and locking range.

## 5. Conclusion

A 32 nm CMOS 12-bit digitally controlled CMOS oscillator design for low power consumption and low jitter is presented. The presented DCO demonstrates a good robustness to process, voltage, and temperature variations and better linearity comparing to the conventional design. The performance and the functionality of the DCO are verified through a novel ADPLL that uses the proposed DCO. This ADPLL is designed and implemented using 32 nm CMOS Predictive Technology Model for a frequency ranges of 570 MHz to 800 MHz at 0.9 V supply voltage. The overall lock-in process of the ADPLL takes about 12 reference cycles at 700 MHz with a peak-to-peak jitter less than 67 ps. The power consumption of the DCO is 2.2 mW at 650 MHz with supply voltage of 0.9 V. The presented results demonstrate that the proposed design is viable for various clock control systems for full digital implementations. The proposed work will be a good reference for future advanced ADPLL such as ADPLL that multiplies the reference clock frequency by a fractional number without using a fractional number divider.

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