

Novel 8-Phase VCO Design using Carbon Nanotube Transistor (CNT)

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Abstract—This paper proposes a novel 8-phase VCO design implemented using Carbon Nanotube Field-Effect Transistors (CNTFETs). Carbon Nanotube is a fast growing and promising technology to replace Traditional MOSFETs. Its operation principles and device structure are similar to the conventional bulk CMOS, however it shows a great power delay improvement over bulk MOSFET due to its near-ballistic CNT transport. In this paper, an eight phase VCO architecture is implemented using both 32nm CMOS and CNTFET technologies to compare the performances of the CNT implementation and CMOS implementation. The simulation results demonstrate that CNT VCO consumes less power than CMOS counterpart while reaching the same range of the working frequency and performance.

I. INTRODUCTION

Traditional CMOS technology has dominated for several decades. However, as silicon devices went into sub-100 nm regime, defined by the National Science Foundation as nanotechnology regime, problems such as short channel effects, ultrathin gate leakage, doping fluctuations, and increasingly difficult and expensive lithography arose. To maintain the trend of Moore's Law and technology's advances in nano-scale regime, novel nanoelectronic solutions are needed to surmount the physical and economic barriers of current technologies. Among them, carbon nanotube transistor (CNTFET) has been attracting more and more attention because of its excellent intrinsic delay, near-ballistic CNT transport, and similar device structure to a MOSFET.

As the demands for high speed data communication are increased, modulation techniques are proposed to increase the data transferring speed. Pulse width modulation (PWM) is one form of modulation schemes, which is mostly used in high-speed memory systems[10]. The major advantage of PWM scheme is that the clock signal is embedded in the PWM-encoded signal, therefore one rising edge is guaranteed during each clock cycle. Based on the jitter analysis addressed in [8], 8-phase clock is required for PWM-4 modulation scheme. In most applications, an eight-phase oscillator is derived from a quadrature VCO by using two identical divide-by-two circuits (DTC) [7]. Therefore, VCO has to be oscillated four times the frequency of the required eight-phase clock. This implementation is not preferred for I/O design since it challenges the speed limitation of the ring oscillator and consumes more power. [9] proposed a novel 8-phase

VCO architecture to generate 8-phase clock signal. In this paper, the VCO design from [9] is ported to CNTFET process and also scaled to 32nm CMOS process to compare the performance between CNTFET and CMOS process.

II. CMOS VCO IMPLEMENTATION

A. VCO Structure

[6] first proposed a ring oscillator architecture that has both internal and external feedback and feed-forward loop. In [9], this VCO architecture was expanded to 8-phase as shown in Fig 1. This oscillator has eight internal loops, each of which is a 5-stage ring oscillator. There are eight internal edges, each one consists of two inverters that form a latch to lock the phase. This VCO architecture can be further scaled up

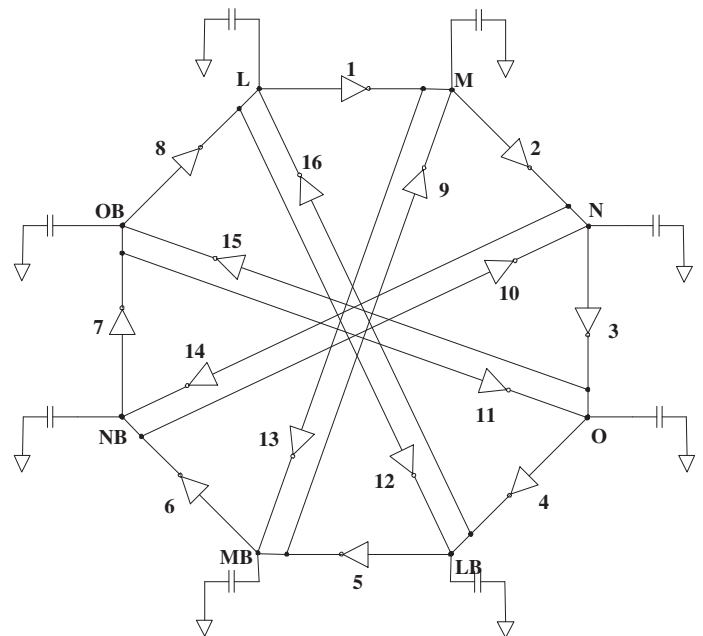


Fig. 1. Octa-VCO Architecture

to 12-phase, 16-phase and all $4n$ -phase VCO (n is a positive integer) as long as the internal loop can form a odd number stage ring oscillator. With the same load, VCO frequency f

is reverse proportional to the number of stages.

B. CMOS Implementation

The frequency of this VCO is determined by the delay of each inverter on the external loop. In CMOS process, the delay T for each inverter can be estimated by

$$T \propto \frac{(C_{ext} + C_{int})V_{supply}}{I_d}, \quad (1)$$

where C_{ext} includes the gate capacitances of the next stage inverter in the external loop, the gate capacitance of the internal latch inverter and the external load capacitance as shown in Fig 1. We use 32nm predictive CMOS model [1] to implement this VCO structure. The supply voltage is scaled to 0.9V. The ratio between the sizes of inverters within the latches and the inverters on the external loop is defined as k_r . From the simulations, we found that the VCO cycle time is proportional to the number of stages which is similar to the conventional odd-number stage ring oscillator. The simulations also show that the average current going through the external inverter chain such as inverter 1 and 2 is around 3 times the average current going through the internal latch inverter such as inverter 9 and 10 with $k_r = 1$. We found there is a good linearity between the C_{ext} and total VCO delay as shown in Fig 2 over the different temperatures. The simulation was setup with FO-N additional external load (N is the number of additional fan-out here excluding the next stage inverter and internal latch inverter). Therefore the total external load is $N + 1 + k_r$ in this simulation.

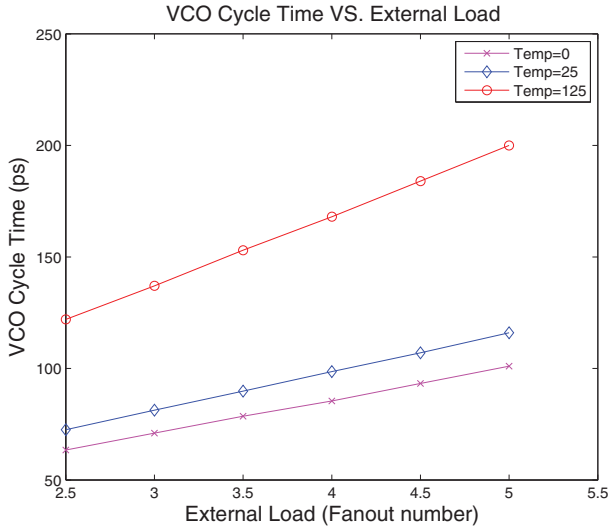


Fig. 2. VCO Cycle Time VS. The Fan-out Number of the External Load (CMOS)

Fig 3 shows a good linearity between VCO frequency and the control voltage over different k_r . Except for the external load and the control voltage, the ratio k_r also affects the frequency of this ring oscillator. The total capacitor load of the external loop increases with the increment of k_r ,

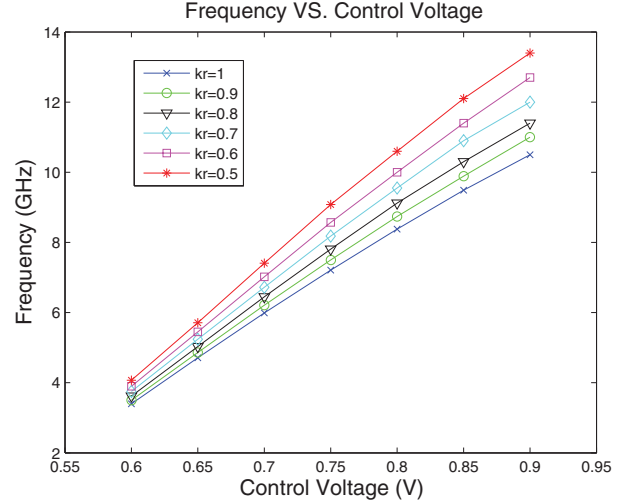


Fig. 3. VCO gain (K_{vco}) over different k_r (CMOS)

therefore, the oscillation frequency of the VCO decreases. As we can see from Fig 3, k_r between 0.5 and 0.7, VCO has a better linearity over a wide frequency range.

III. CNTFET DELAY AND VCO FREQUENCY

CNTFET has similar behaviors as traditional CMOS transistors. CNT gate delay can be estimated as[3]

$$T_{CNTFET} \propto \frac{(C_{ext} + C_{int})V_{supply}}{I_{CNTFET}}. \quad (2)$$

Similar to CMOS, C_{ext} is contributed by the next stage gate capacitance. The gate capacitance can be approximated by

$$C_{g-total}(CNT),n = n \cdot (C_{g-CNT,1}L_{g,CNT} + C_{g-parasitic}W_{g,CNT}), \quad (3)$$

where $W_{g,CNT}$ is the width of a single CNT and $L_{g,CNT}$ is the length of the lithographically defined gate, n is the number of tubes. For a CNTFET with n tubes, the driver current ($I_{CNTFET,n}$) can be expressed as

$$I_{CNTFET,n} = n g_{CNT} (V_{supply} - V_{SS'} - V_{th,CNT}), \quad (4)$$

where V_{th} can be expressed as [5],

$$V_{th} = \frac{\sqrt{3}}{3} \cdot \frac{aV_{\pi}}{eD_{CNT}}. \quad (5)$$

In equation (5), $a = 2.49\text{\AA}$ is the carbon to carbon atom distance, $V_{\pi} = 3.033\text{eV}$ is the carbon $\pi - \pi$ bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. With D_{CNT} of a (19,0), the threshold voltage is 0.29V as calculated from equation (5).

All of our simulations are based on Stanford University CNTFET Model [2], [13], [14]. We adopted the similar simulation setup as CMOS VCO. There is a good linearity between total VCO delay versus the external capacitance as shown in Fig 4 over the different temperatures. As we can see, the slop of the curve is steeper in CNT case since the external

capacitance is more dominated in CNT case. In the meanwhile, temperature variation is much smaller in CNT case.

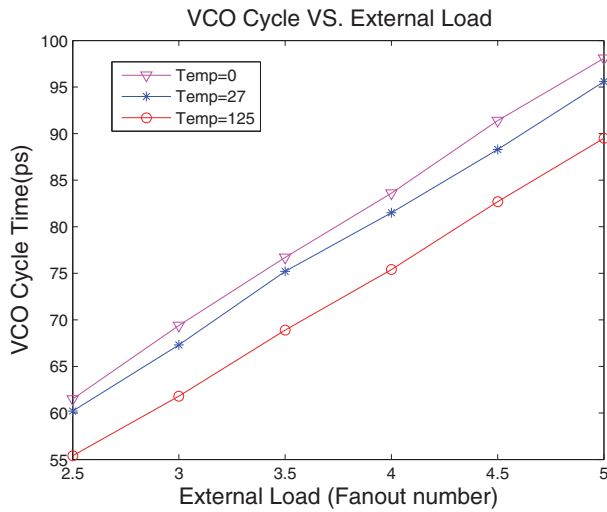


Fig. 4. VCO Cycle time VS. The Fan-out Number of the External Load (CNT)

The gain of the VCO (K_{vco}) is simulated over different k_r and plotted in Fig 5. There is a good linearity between VCO gain(K_{vco}) and the control voltage over different k_r for CNT VCO.

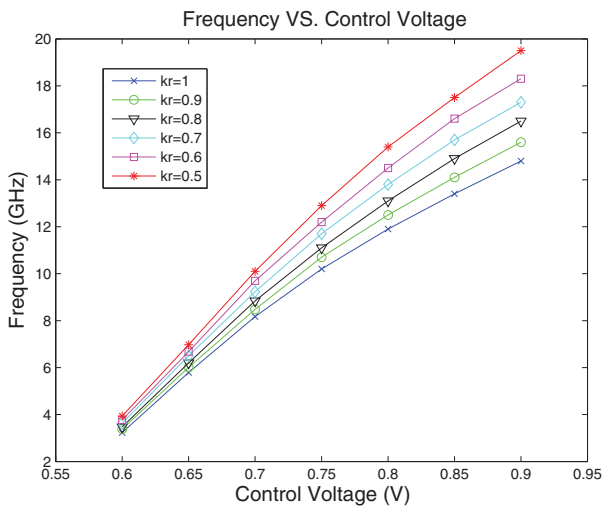


Fig. 5. VCO gain (K_{vco}) over different k_r (CNT)

IV. LEVEL SHIFTER

The output voltage swing of the proposed VCO may transit from $0 - 0.6V$ to $0 - 0.9V$ depending on the control voltage. To assure the full supply voltage swing of the different phase clock signal, level shifter is used to shift the output signal of the VCO to the full supply voltage swing. The level shifter structure is shown in Fig 6. With a carefully sizing, the DC input range of this shifter is adjusted to $0.3V - 0.45V$ and the unit gain bandwidth is extremely large. Therefore, this

level shifter can output full-voltage swing 50% duty cycle signal over a wide frequency range using CNT process. The simulation results shown in Fig 7 illustrate how the duty cycle is changed according to the different input common-mode voltages and the different signal frequencies. As we can see from this figure, the output signal of this level shifter can guarantee 50% duty cycle over a wide range of the input frequency and the working DC input voltage.

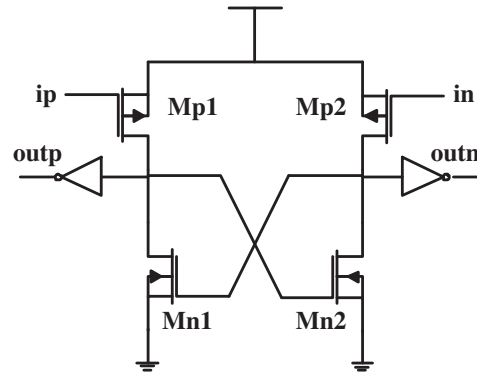


Fig. 6. Level Shifter Architecture

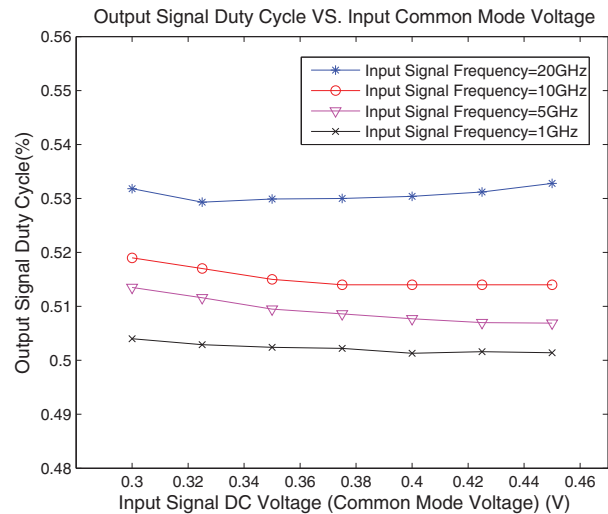


Fig. 7. Duty Cycle VS. The Common Mode Voltage of Input Signal over Different Frequencies

V. PERFORMANCE COMPARISON

Table I shows the VCO gain comparison between CMOS VCO and CNT VCO. As we can see, CNT VCO has a higher K_{vco} in the same voltage range, which means CNT VCO has a wider frequency tuning range than its CMOS counterpart.

As discussed in [11], [12], CNTFET based logic gate has a much lower power-delay product (PDP) and the leakage power than CMOS gates. From our simulations, we prove that CNT VCO consumes much less power given the same control voltage. Table II shows that on average, CMOS VCO

Control Voltage Range(V)	0.85-0.9	0.8-0.85	0.75-0.8	0.7-0.75	0.65-0.7	0.6-0.65	0.6-0.9(Average)
K_{vco} (CMOS)	($k_r = 1$)	20	24	25.8	28.4	31	26.8
	($k_r = 0.9$)	22	26	27.6	30.4	32.6	28.6
	($k_r = 0.8$)	26	26	30.4	32.8	34	30.7
	($k_r = 0.7$)	28	28	32	35.6	36.4	32.7
	($k_r = 0.6$)	30	32	34	37.4	38.4	35.1
	($k_r = 0.5$)	32	36	36	40.4	41.2	37.3
K_{vco} (CNT)	($k_r = 1$)	28	30	34	40.6	47.6	38.6
	($k_r = 0.9$)	30	32	36	44.4	49.4	40.7
	($k_r = 0.8$)	32	36	40	45.2	52.8	43.4
	($k_r = 0.7$)	32	38	42	49.4	54.6	45.6
	($k_r = 0.6$)	34	42	46	50.2	60.2	48.4
	($k_r = 0.5$)	40	42	50	56	62.6	51.8

TABLE I
VCO GAIN COMPARISON BETWEEN CMOS IMPLEMENTATION AND CNT IMPLEMENTATION

Control Voltage(V)	0.9	0.85	0.8	0.75	0.7	0.65	0.6
Power(uW)of CMOS VCO	610	482	371	276	195	129	77.4
Power(uW)of CNT VCO	52.6	39.6	28.6	19.3	11.8	6.1	2.4

TABLE II
POWER COMPARISON BETWEEN CMOS IMPLEMENTATION AND CNT IMPLEMENTATION

consumes 10 times more power than its CNT counterpart. Therefore, CNT VCO is a much better choice for the low power design while maintain the high speed performance.

VI. CONCLUSIONS

The Carbon Nanotube Field Effect Transistor (CNTFET) is one of the most promising devices among emerging technologies to extend and/or complement the traditional silicon MOSFET. In this paper, the design of a novel 8-phase VCO based on CNT process is proposed. And the performances of the CNT VCO have been evaluated and compared against the counterpart in CMOS with the same gate channel length. Simulation results have shown that CNT VCO has slightly larger VCO gain and frequency tuning range while consumes much less power. The VCO designed using CNTFET gates also has a high robustness to temperature variations. Therefore, the quantitative results of this paper have confirmed that CNTFET technology is a viable solution to replace conventional MOSFET technology.

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