

High Speed and Low Power Transceiver Design with CNFET and CNT Bundle Interconnect

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ABSTRACT

In this paper, a low power capacitive 4-PWAM transmitter architectures and circuits design using Carbon Nanotube Field Effect Transistor (CNFET) and Carbon Nanotube bundle interconnects is presented along with its performances analysis considering random jitter and PVT variations. A novel technique is proposed to reduce power and to increase speed by using capacitive driven low swing transceiver. The proposed transceiver design saves power by factor of 5.7~6.4 and accomplishes 4 times higher data rate than the conventional CMOS technology designs. To implement 4-PWAM transmitter, new phase controller and adaptive capacitance network are designed while new architectures are proposed for PWM and PAM demodulation at the receiver side.

I. INTRODUCTION

The environment of the communication channel and the semiconductor technology limit the maximum symbol rate of the serial data transmission. Therefore, many researches have been published to increase the data rate while keeping the same symbol rate and sustaining the signal integrity. Among them, pulse-amplitude modulation (PAM) and pulse-width modulation (PWM) are two advanced modulation schemes. [1] introduced a transceiver that uses both PWM and PAM modulation to boost the data transmission rate for the first time. However, its application has been limited to a relatively low-speed data transmission (250M symbol/s) and it utilizes the conventional PWM and PAM symbol representations. This paper presents a novel and universal PAM and PWM combination scheme that provides a high data transmission rate, where the unit pulse width (one full clock period) and the basic pulse width (minimum modulated pulse width) are determined by the channel environment and

the jitter specification due to its high data transmission rate. Therefore, it is essential to perform jitter analysis and Bit Error Rate (BER) analysis considering process, voltage, and temperature variations.

In order to design low power and high speed circuit, power consumption cannot be overlooked since the power consumption increases with the circuit operation speed. In modern integrated circuit design, due to the switched capacitances of the interconnect lines, on-chip wires also present an increasing energy issue. A CMOS wire driver running at an effective frequency must switch a total wire capacitance C_w through the voltage, leading to a power cost proportional to CV^2f . Under technology scaling, C_w remains largely constant (for global wires spanning constant-sized die), voltage scales down only slowly, and frequency (f) scales up, leading to nearly constant power per wire. However, as chip's device integration level is increasing continuously, this constant power per wire gets multiplied by an ever-increasing number of wires. Therefore, it is necessary to reduce C_w and signal voltage swing to save power. In CNFET technology C_w can be reduced by replacing Cu interconnect with CNT bundle interconnect, and it is possible to obtain low voltage swing driving a wire with a capacitor. A coupling capacitor in line with the long wire pre-emphasizes transitions is proposed in [6] to reduce wire delay and to reduce the load seen by the driver. It also lowers the wire's voltage swing without additional power supply. However, a new wire model of the CNT bundle interconnect needs to be developed for signal integrity analysis and bit error rate estimations. This paper investigates the CNT bundle interconnect model and signal integrity issues along with the circuit design of the low power and high speed transceiver based on CNT

FET technology. Moreover, the power can be saved applying CNFET technology[2].

In this paper, to maximize the speed and minimize the power, new PWAM scheme with capacitive transceiver with CNFET and CNT bundle interconnect is proposed

II. CNFET AND CNT BUNDLE Technologies

CNTs are sheets of graphene rolled into tubes; depending on the chirality (i.e., the direction in which the grapheme sheet is rolled), a single-walled CNT can be either metallic or semiconducting. Semiconducting nanotubes have attracted widespread attention of device/circuit designers as an alternative possible channel implementation for high-performance transistors [2]. A typical structure of a MOSFET-like CNFET device is illustrated in Figure 1. The CNT channel region is undoped, while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices. Carbon nanotubes are high-aspect-ratio cylinders of carbon atoms. The electrical properties of a single wall carbon nanotube (SWNT) offer the potential for molecular-scale electronics since a typical semiconducting single-wall carbon nanotube is 1.4nm in diameter with a 0.6eV bandgap (the bandgap is inversely proportional to the diameter). Recent carbon nanotube field effect transistors (CNFETs) have a metal carbide source/drain contact and a top gated structure (figure 1) with thin gate dielectrics [2]

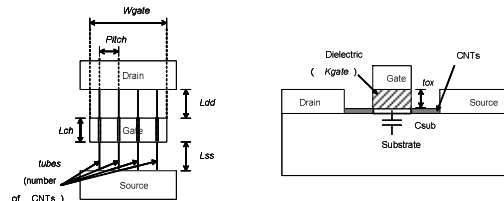


Figure 1. CNFET structure

The contact resistance and the subthreshold slope of a CNFET are comparable to those of silicon MOSFET. While a silicon FET's current drive is typically measured in current per unitary device width (e.g. $\mu A/\mu m$), the current of a CNFET is measured in current per tube (as reflecting the structure of the CNFET as an array of equal carbon nanotubes with constant spacing and fixed diameter). Carbon nanotubes have recently been proposed as a possible replacement for metal interconnects in future technologies [2]. Its structure and interconnect model[3] are shown in Figure 2.

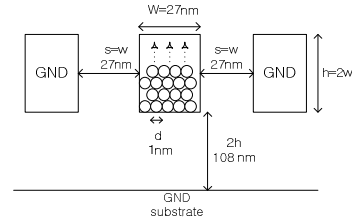


Figure 2. CNT bundle interconnect structure

Because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [6], CNTs have aroused a lot of research interest in their applicability as VLSI interconnects of the future. However, the high resistance associated with an isolated CNT (greater than 6.45 K Ω) [9] necessitates the use of a bundle (rope) of CNTs conducting current in parallel to form an interconnection [3]. Moreover, due to the lack of control on chirality, any bundle of CNTs consists of metallic as well as semi-conducting nanotubes. CNTs are also classified into single-walled and multi-walled nanotubes. Single-walled CNTs (SWCNTs) have electron mean free paths of the order of a micron [3]. Therefore, in the domain of interconnects, metallic SWCNTs are the preferred candidates, and the single-walled metallic CNT bundle structure is used for the channel media between the transmitter and receiver in this paper. Noise and bit error rate of the transceiver is estimated and analyzed based on the interconnect structure.

III. POWER CONSIDERATIONS FOR 4-PWAM DESIGN

PWAM-(M \times N) scheme combines PAM-M (M is the number of different voltage levels) and PWM-N (N is the number of different pulse widths) together.

With M different pulse amplitudes and N different pulse widths, there exist M \times N different symbol representations [1]. M \times N symbols represent $\log_2 M + \log_2 N$ bit binary information. Therefore, the bit rate of PWAM-(M \times N) is $\log_2 M + \log_2 N$ times the symbol rate. The M different level voltages should be driven over a long channel. However, it is essential to use lower levels of the signals to save power since the power is quadratically proportional to the voltage. In this paper, a capacitive voltage divider scheme is used to reduce and control the voltage swing of the transmitted signal. Driving a long wire of capacitance C_w through a capacitor C_c reduces the signal swing on the wire through capacitive voltage divider [6]. As shown in Fig. 2,

including parasitic capacitance on the right side of the coupling capacitor and including the final load capacitance gives a final wire voltage swing of $V_{swing} = V_{DD}C_d/(C_c+C_w+C_{p2}+C_l)$. Typically, C_{p2} and C_l are both small compared to C_w .

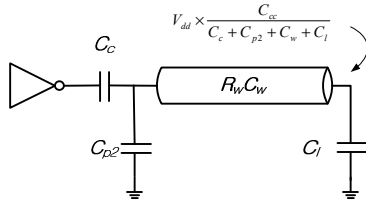


Figure 3. The capacitively driven wire

The node immediately after the coupling capacitance will initially overshoot and then settle to V_{swing} , while the end of the wire will show a rapid rise to the final V_{swing} voltage.

The energy-cost for a rising edge with swing V equals the well-known $E=CV^2$. Half of this energy is dissipated during charging. The other half is stored in the interconnect and dissipated at a later time when the interconnect is discharged (the resistance of the interconnect prevents efficient charge-recycling techniques). To reduce the link power, it hence makes sense to reduce the swing and interconnect capacitance. In this paper, the energy reduction can be achieved by using CNT bundle interconnect and capacitive transmitter which produces low swing signal.

IV. 4-PWAM CIRCUIT DESIGN

A. CNFET circuit design

The parameters of the CNFET used for the circuit design are 20nm pitch (distance between adjacent CNTs), 0.3V V_{th} (threshold voltage), and 1.8V VDD (power supply voltage). The methodology for CNFET design in [2] was used in order to optimize the circuits. From [2], the optimal fan-out factor ($f=4$) are obtained, which decides the optimal number of carbon nantubes of each P-CNFET and N-CNFET. Most important factor for process variation of CNFET is the number of carbon nanotubes for each CNFET because of the lack of control on chirality. Any CNTs can be semi-conducting as well as metallic nanotubes. The metallic carbon nanotubes are removed by electrical burning [2] or chemical/plasma etching [2]. After removal of the metallic CNTs, the circuit operation can be affected by improper number of carbon nanotubes. Therefore, the enough number of carbon nanobues has to be chosen. In this work,

the number of carbon nanotubes is decided considering the portion of the metallic carbon nanotubes (15%).

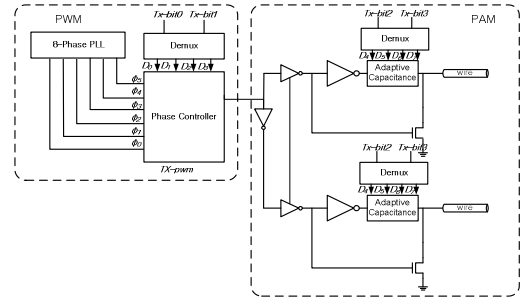


Figure 4: The block diagram of the transmitter

B. Transmitter circuit

The architecture of the PWAM transmitter is shown in Fig. 4. It contains three main building blocks: a PWM modulator, a PAM modulator, and 8 phase PLL. An 8 Phase PLL provides evenly spaced clock phases that are used to produce PWM-encoded signals. After processing Tx-bit0 and Tx-bit1 using the PWM technique, PAM signaling is used to modulate the information from Tx-bit2 and Tx-bit3. In addition to the PWAM modulator, the capacitively driven wire acts as a pre-emphasis block. This compensates for the limited bandwidth of the package leads and channel medium [6]

a) 2-PWM modulator

The pulse width modulation can be implemented using the 8 phase PLL and phase controller. 6 phase signals and control data D0~D3 are used as inputs. Based on their combinations, the pulse width is determined, and the phase controller is shown in Fig 5.

b) 2-PAM modulator

In order to realize low power PAM modulator, the low swing capacitive pulse amplitude modulation scheme is proposed in this paper. The capacitive PAM driver can be implemented using adaptive capacitance which is shown in Fig. 6. The bit3, bit4 determine the output of the Demux $D1, D2, D3, D4$ which consequently decide the capacitance. By changing the capacitance, multiple V_{swing} can be obtained, and the level of the voltage swing V_{swing} is expressed as Equation (1).

$$V_{swing} = V_{DD} (\sum D_k C_{ck} + C_w + C_{p2} + C_l) \quad (1)$$

Where D_k is $\{0,1\}$ and C_{ck} is a capacitance element of the adaptive capacitance network. C_{ck} can be expressed as (2);

$$C_{ck} = N_k \cdot C_{c1} + C_{gate,k} \quad (2)$$

Where C_{c1} is the capacitance of one carbon nanobue in $P_{1\sim4}$, N_k is the number of carbon nanotubes and $C_{gate,k}$ is the capacitance due to the gate size in CNFET in adaptive capacitance network. The C_{ck} is nearly propotional to N_k . the $N_{1\sim4}$ are $N_1 = 120$, $N_2 = 220$, $N_3 = 410$, $N_4 = 790$ in this paper.

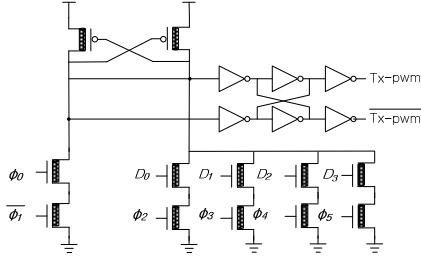


Figure 5: Phase controller

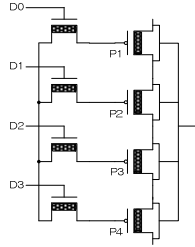


Figure 6: Adaptive Capacitance

B. Receiver circuit

Fig.7 shows the block diagram of the receiver. The receiver consists of 4 differential amplifier, 4 comparators, one PLL, the pulse width demodulation circuits, and supplementary circuits. Bit2 and bit3 are recovered by PAM demodulator and bit1 and bit0 are generated from pulse width demodulation circuits. As shown in Fig 7. The architecture of the PWM demodulator is quite simple. It is composed of three D-latch and a 3bit to 2bit decoder. The PLL in the receiver end provides 8-phase clock required by the pulse width demodulation circuit. Because the voltage swing of the signal received from wire is small, it is amplified by differential amplifier ($\Delta V_{swing} = 100\text{mv}$). The different amplitude level of the received signal after amplification is 200mV. Accordingly, the reference voltages for comparators are $V_{ref1} = 1.5\text{V}$, $V_{ref2} = 1.3\text{V}$, $V_{ref3} = 1.1\text{V}$, and $V_{ref4} = 0.9\text{V}$. This multiple voltage references can be obtained from [10]. After

amplification, the signal is fed into the comparator, where digital output 0(0V) or 1(V_{DD}) is determined. The final bit2 and bit 3 are recovered by the decoder based on the comparator output.

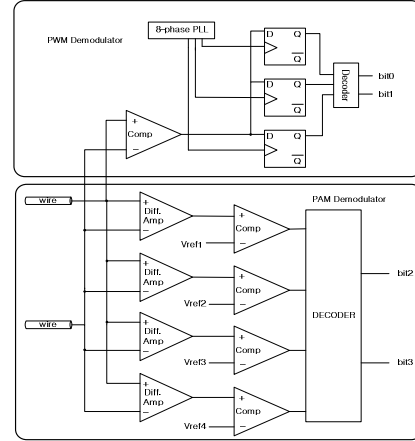


Figure 7: Receiver circuits

V. Noise Modeling and Bit 4-PWAM CIRCUIT DESIGN

A. Noise Models

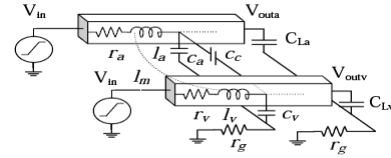


Figure 8. Wire model for crosstalk noise.

The major portion of the noise that causes a bit error is crosstalk noise. Crosstalk noise model is shown in Fig 8, and the low swing signal can be victimized by large aggressor signal severely. If the large aggressor signal affects the small victim signal, shielding technique [6] needs to be used between small and large swing signals. Fig. 9 shows the difference between the shielded and unshielded victim signals. Even though the shield technique is used, it is evident that there is crosstalk noise between two small signals.

B. Bit error rate (BER) estimation

The probabilities of bit error in this transceiver system can be expressed as the following;

$$P_{err-pwam} = P_{err-pwm} + P_{err-pam} \quad (3)$$

$$P_{err-pwm} = P_{err-Djitter} + P_{err-Dljitter} \quad (4)$$

$$P_{err-pam} = P_{err-process} + P_{err-voltage} + P_{error-crosstalk} \quad (5)$$

Where $P_{err-pwm}$, $P_{err-pam}$, $P_{err-Djitter}$, $P_{err-Dljitter}$, $P_{err-process}$, $P_{err-voltage}$ and $P_{error-crosstalk}$ are probabilities of error caused by PWM, PAM, DD(data dependent) jitter,

DI (data independent) jitter, and process/voltage variation including crosstalk, respectively.

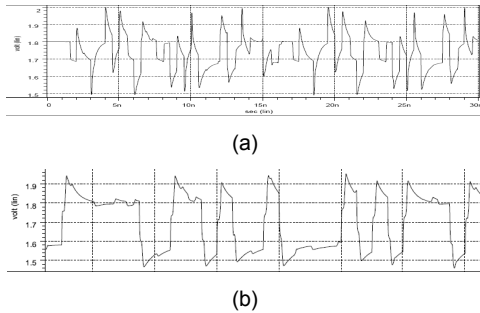


Figure 9. Crosstalk noise caused by large aggressor signal (a) victim signal without shield technique (b) victim signal with shield technique.

It can be assumed that all probabilities are independent so there is no correlation between them. In this paper, all error events are assumed to have Gaussian distribution except $P_{error-crosstalk}$. Therefore, it is possible to find all probabilities by Monte Carlo simulation using PRBS-11 test bit patterns except crosstalk noise.

VI. SIMULATION RESULTS

The circuit simulation has been done with 32nm CNFET technology model. The wire model and its parameters were obtained from [14] (wire length = 2 mm, C_{bundle} = 140fF, R_{wire} = 500 Ω), and the supply voltage 1.8V is used in this simulation.

Fig 9 shows eye diagrams of the 4 different pulse widths and 4 different levels of voltage amplitudes. The voltage difference of each level is around 100mv in the design. In order to test the proposed 4-PWAM transceiver, the PRBS-11 signal is used, and the test was done with various environments with Monte Carlo method with 1000 times iteration.

A. Without PVT Variation

The first simulation was done without any random jitter and PVT variations. The eye diagram for this is shown in Fig 9. The proposed transceiver works without any error (BER=0) and there is only data dependent jitter, which is ΔT_{rms} = 5.7ps and ΔT_{pk-pk} = 20.1 ps.

B. Process variation

The process variation was simulated by setting number of carbon nanotubes of each CNFET with variation 0.1, and 3σ Gaussian distribution. Its eye diagram is shown in Fig 10. The bit error can be caused by inaccurate pulse width and amplitude. The eye is almost closed between 1.29 ~ 1.49. As

the data rate increases, it is more sensitive to jitter. Due to variation of number of carbon nanotubes, the jitter is increased. As a result bit error is caused if the jitter exceeds the half of the minimum pulse width. The measured bit error rate is $2.8E-10$, which is less than expected value 10^{-10} .

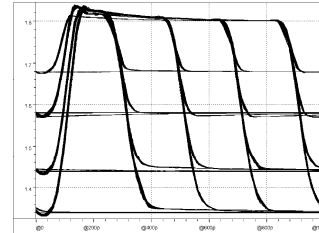


Figure 9. Eye-diagram of received PWAM signals without PVT Variation

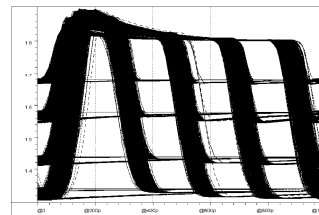


Figure 10. Eye-diagram of received PWAM signals with process Variation

C. Voltage variation

The simulation of supply voltage variation was performed using Gaussian distribution which has 0.01 ~ 0.1 variations and 3σ for voltage. By changing the voltage variation, it is observed that the eye opening changes drastically. Fig 11 shows eye-diagram for 0.5 variations. At 0.01 variation the eye is almost 60~70% open and as the variation goes over 0.5, the eye is completely closed. The measured BER is $1.3E-7$ and it is higher than the expected value 10^{-8} .

D. Temperature variation

The simulation was run from 0 $^{\circ}$ C to 100 $^{\circ}$ C. However, the jitter and voltage level variation are very little due to CNT characteristics.

E. Crosstalk noise

Crosstalk noise was simulated using the crosstalk noise model shown in Fig 8, where PRBS pattern is applied to the aggressor and victim line is observed. The eye-diagram of the simulation is obtained by generating almost ten thousand bit patterns and the result is shown in Fig 12. From the measurement, the $2.63E-12$ BER was obtained, which is less than the BER caused by process and voltage variations.

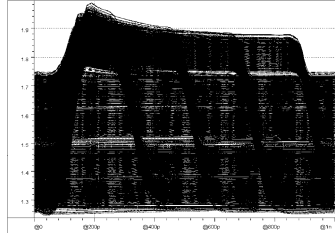


Figure 11. Eye-diagram of received PWAM signals with voltage variation

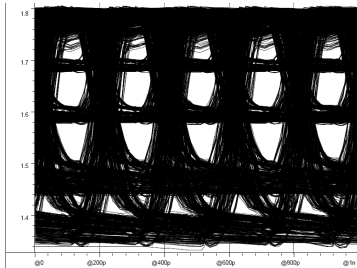


Figure 12. Eye-diagram of received PWAM signals with crosstalk noise.

F. Comparison with CMOS 4-PWAM

Because of the PWAM scheme and capacitively driven method, the data rate in this work is higher than any other scheme. Since it is impossible to make the pulse width 20% of clock cycle over 8GHz, the maximum frequency of this work is limited to 8GHz. Table 1 summarized the comparisons. In case of capacitively driven wire, the data dependant jitter is less than other methods. The data dependant jitter of this work is smallest among others because the intrinsic delay of CNFET is smaller than any other cases, and the CNFET transceiver consumes less power than others due to smaller CNT bundle capacitance and low swing. The results prove that the voltage swing and interconnect capacitance are dominant factors for power consumption.

VII. CONCLUSION

In this paper, CNFET capacitive 4-PWAM transmitter architecture is proposed and its performances are analyzed considering PVT variations. To implement 4-PWAM transmitter, new phase controller and adaptive capacitance network are designed with CNFET. At the receiver side, new architecture for PWM and PAM demodulation is proposed. The 4-PWAM CNFET transceiver in this work has low data dependant jitter, and it does not affect the bit error rate. However, it is very sensitive to supply voltage variation due to low voltage difference (100mv) between the amplitude

modulation levels, which causes low noise margin. But if the supply voltage variation is lower than 5%, the bit error rate is less than 10^{-10} .

Table 1. Summary of the performances and comparison

Reference	[4]	[6]	CMOS	CNFET
Technology	0.18 μ	90nm	0.18 μ	32nm
Supply	1.8V	1.2V	1.8V	1.8V
Max. Voltage Swing	900mV	120mv	400mv	400mv
Power dissipation	Tx : 86mW Rx : 79mW	Tx : 14.4mW Rx : 18.4 mW	Tx : 36.5 mW Rx : 45.2 mW	Tx :9.5 mW Rx : 10.2 mW
Data rate	2Gb/s	5Gb/s	8Gb/s	32Gb/s
Jitter	$T_{rms} = 49.9ps$ $T_{pk-pk}=180ps$	$T_{rms} = 9.8ps$ $T_{pk-pk} = 58.2ps$	$T_{rms} = 11.2ps$ $T_{pk-pk}= 70.1ps$	$T_{rms} = 5.72ps$ $T_{pk-pk} = 20. ps$

The proposed CNFET capacitive 4-PWAM transmitter with low swing voltage saves power consumption significantly comparing with the full swing one and other PAM scheme due to low voltage swing and low CNT bundle capacitance. Furthermore, it increases data rate using PWAM modulation and pre-emphasis [5]. In this paper, the proposed transceiver demonstrates that almost 5.74~6.4x times power is saved compared to the conventional CMOS design and it shows 4 times higher data rate than CMOS 4-PWAM.

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