



A Charge Pump that Generates Negative High Voltage with Variable Voltage Gain

Journal:	<i>IEEE Transactions on Very Large Scale Integration Systems</i>
Manuscript ID:	TVLSI-00348-2011
Manuscript Type:	Regular Paper
Date Submitted by the Author:	02-Aug-2011
Complete List of Authors:	ZHAO, JUN; Northeastern University, ECE Kim, Yong-Bin; Northeastern University, Electrical and Computer Engineering Ivanov, Evgeny; Analog Devices, Linear and Radio Frequency Group
Key Words:	dc-dc converter, Charge pump, voltage multiplier

SCHOLARONE™
Manuscripts

A Charge Pump that Generates Negative High Voltage with Variable Voltage Gain

Jun Zhao, Evgeny Ivanov, *Member, IEEE*, and Yong-Bin Kim, *Senior Member, IEEE*

Abstract— A high efficiency and variable voltage gain charge pump to generate negative high voltages is presented based on a cross-coupled structure. The problem of shoot-through current is solved using a four-clock phase scheme, and a variable voltage gain is obtained by switching the power supply to each stage based on the input voltage range. A complete analysis and optimization method of the interaction among the power efficiency, area, and frequency are presented. The proposed negative charge pump is designed using on-chip capacitors to deliver 40 uA with a wide supply range from 2.5V to 5.5V using 0.18um high voltage LDMOS technology.

Index Terms—Charge pump, dc-dc converter, switched-capacitor power converter, voltage multiplier.

I. INTRODUCTION

CHARGE pump circuits [1-2] (also called switched capacitor dc-dc converters) provide a voltage that is higher than the voltage of the power supply or a voltage of reverse polarity. Charge pumps have been widely used in the nonvolatile memories, such as EEPROM and Flash memories, Power IC, and switch capacitor systems.

Among many approaches to the charge pump design, the switched capacitor circuits such as Dickson charge pump [3] are very popular, because they can be implemented on the same chip together with other components of an integrated system. However the voltage drop across the diodes or diode-connected transistors is too lossy for high efficiency applications. Wu et al. [4] presented a static charge transfer switches technology to compensate the inherent transistor threshold voltage drops. Theoretically, the modified charge pump is more efficient than the conventional one, but a major drawback is an undesirable reverse charge leakage, which reduces the voltage pumping gain. An improved design proposed two years later claimed to be capable of solving the leaking problem by adding a pair of auxiliary transistors in each power stage [5]. However the

impact of the body effect limited this topology to five power stages.

As the supply voltage decreases to the threshold voltage, the conventional Dickson charge pump can't function properly since its conversion efficiency becomes near zero. As the alternative to Dickson charge pump circuits, cross-coupled switched capacitor DC-DC converters are more appropriate for battery-driven portable applications [6-8]. Since the voltage gain for the cross coupled architecture is higher than that of the Dickson charge pump, the number of stages required to reach a specific output voltage is reduced. This reduces the parasitic capacitances introduced in the circuit.

This paper describes a new charge pump that is able to generate a high negative voltage using on-chip capacitors with a wide supply voltage range. The charge pump is used as the input stage of an instrumentation amplifier. By using this charge pump in combination with a similar positive charge pump, the instrumentation amplifier can be powered from 2.5-5 V external power supply but will be able to process input voltages in $\pm 15V$ common-mode range required for industrial signal processing. The variable voltage gain is realized by switching the power supply to each power stage based on the supply voltage V_{DD} . The proposed negative charge pump is able to deliver 40uA current with a supply range from 2.5V to 5.5V using 0.18um high voltage LDMOS technology.

II. ARCHITECTURE OF THE PROPOSED HIGH VOLTAGE NEGATIVE CHARGE PUMP

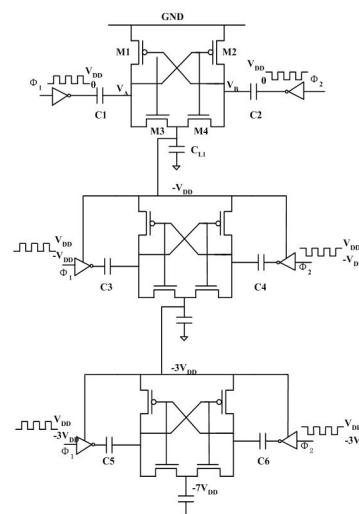


Fig. 1. Conventional cross-coupled structures of negative charge pump circuits.

Manuscript received Nov, 2010. This work was supported by Analog Devices Inc.

Jun Zhao is with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115 USA (e-mail: jzhao@ece.neu.edu).

Yong-bin Kim is with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115 USA (phone:617-373-2919; fax:617-373-8970; e-mail: ybk@ece.neu.edu).

Evgeny Ivanov is with the Analog Devices Inc., Wilmington, MA 01887 USA, (e-mail: Eugene.Ivanov@analog.com).

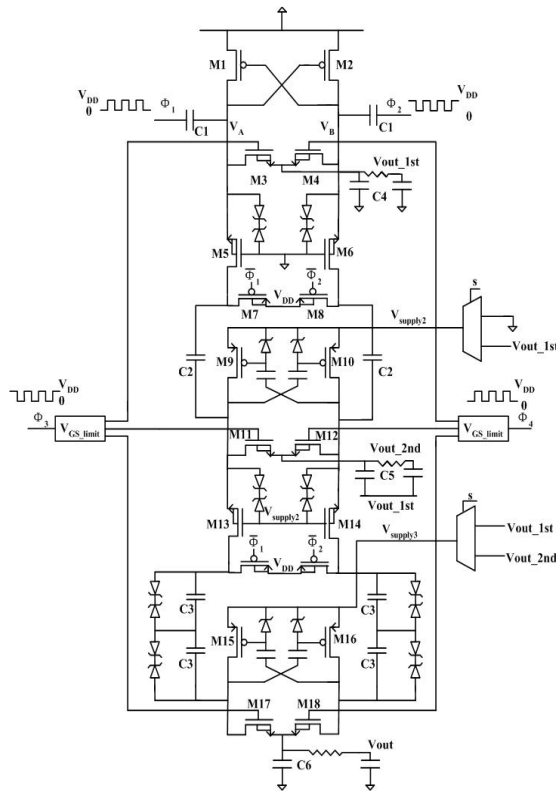


Fig. 2. Circuit topology of the proposed negative charge pump.

The basic operation of the conventional cross-coupled charge pump circuits [9-10] is shown in Fig. 1. The non-overlapping complementary clock phases Φ_1 and Φ_2 are designed to avoid shoot-through current. V_A and V_B swing from V_{DD} to $-V_{DD}$ alternately to charge C_{L1} to $-V_{DD}$. By cascading three such structures, a voltage gain of $-7X$ can be obtained. Since C_{L1} is charged in both phases, the operating frequency is 2 times of the Dickson charge pump. However, in order to prevent shoot-through current of the inverters driving $C_3 - C_6$, a level shifter circuit is needed, which consumes static power. Moreover, the non-overlapping clock phase Φ_1 and Φ_2 prevent shoot-through current for M1 and M2, but they also generate shoot-through current for M3 and M4. This also happens in the 2nd and 3rd stages. Finally, the conversion ratio of the conventional charge pump circuit is fixed as soon as the circuit topology is decided, which results in a limited input voltage range.

The improved negative charge pump design based on cross-couple structure is shown in Fig. 2. Based on previous design [11], an improved four-clock phase scheme has been designed to avoid the shoot-through current. When $\Phi_1 = 1$ and $\Phi_2 = 0$, V_A is pushed up to $0V$ and V_B is pulled down to $-V_{DD}$. At the same time, M3 is turned off and M4 is turned on. As a result, the output voltage of the 1st stage will be pulled down to $-V_{DD}$. The gate voltage of M5 and M6 is grounded, which makes sure they are turned on separately only when V_A or V_B is pulled down to $-V_{DD}$. V_{gs_limit} in the Fig. 2 represents the LDMOS drive circuit designed to protect the V_{gs} breakdown.

In the 2nd stage, the top plate of C_2 is pushed up to V_{DD} when $\Phi_1 = 1$ and pulled down to $-V_{DD}$ when $\Phi_1 = 0$. The bottom plate of C_2 is pushed up to $-V_{DD}$ and pulled down to $-3V_{DD}$ separately when the supply voltage of the second stage is

V_{out_1st} . In this case, the voltage gain of the 2nd stage is $-3X$. Finally, if $V_{supply3} = V_{out_2nd}$, this negative charge pump can provide a maximum voltage gain of $-7X$. By switching the supply voltage of the 2nd and 3rd stage, a variable voltage gain ($-4X$, $-5X$, and $-7X$ separately) can be realized [12-14].

For process consideration, since the MIM cap has a maximum voltage across it around 8V, the bottom plate of C_5 has been connected to V_{out_1st} and capacitor C_3 has been replaced by two capacitors in series. Although fringing capacitance can be used here, it provides lower power efficiency due to high parasitic capacitance. The only fringing capacitance that can't be avoided is C_6 . By connecting the gate voltage of M13 and M14 to $V_{supply2}$ instead of Φ_3 and Φ_4 , we could have a larger V_{GS} , which reduces the RC delay. The charge pump circuit operates at a high-frequency level in order to increase their output power with in a reasonable size of total capacitance used for charge transfer. The operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

III. CIRCUIT DESIGN ISSUES

A. Clock Scheme

The non-overlapping clock phases Φ_1 and Φ_2 prevent shoot-through current from M1 and M2 as shown in Fig. 2. However, when these two clock phases are applied to the gates of M3 and M4, the shoot-through current occurs when both of them are at high voltage. This results in higher ripple voltage and power loss.

In order to avoid current flowing from C_1 to the output while Φ_1 is high, M3 should be turned off. The clock phase Φ_3 and Φ_4 have been generated as shown in Fig. 3 similar to [15]. The negative delay is realized by adding a buffer between the inverter and the clock generator. As a result, M3 or M4 will be turned on only during the time V_A or V_B is pulled down. Since C_2 is charged and discharged by clock phases Φ_1 or Φ_2 , the clock phases in the 2nd stage are the same as those in the 1st stage. This clocking scheme has two advantages. First, the clock phases of M9 and M10 are still non-overlapping. Second, the clock phases of Φ_3 and Φ_4 can still be used to avoid shoot through current from V_{DD} to V_{out_2nd} . This also applies to the

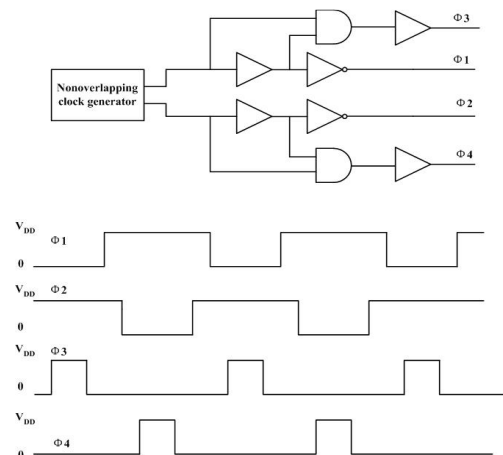
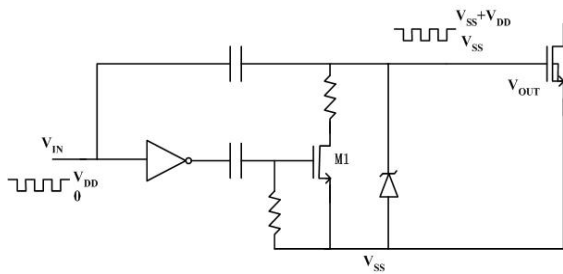


Fig. 3. Four clock phase generator used to prevent shoot-through current.

Fig. 4. LDMOS drive circuit for V_{GS} breakdown protection.

3rd stage. This four-clock scheme is applicable to all the three stages in this charge pump circuit to avoid the shoot-through current. Since only 6 minimized logic gates are added, the extra power consumption is negligible.

B. LDMOS Drive Circuit

The LDMOS switches [16] (M3-M18) are placed in separate isolated high-voltage deep N-wells. In order to prevent forward biasing of the PW-DNW junction, the actual N-LDMOS is realized as a pair of two identical N-LDMOS devices connected drain-to-drain in series with each other. The LDMOS devices in the HV process are designed to withstand up to 40V across drain-to-source and drain-to-gate terminals, but only up to 6V across gate-to-source terminals. Therefore, Zener diodes are used to protect the gates from voltage overstress. The Zener diode is implemented in a P-well isolated by deep N-well from the substrate. Inside the P-well special diffusions are used to form the Zener diode junction. Although Zener diode diffusions require additional masks and process steps, it is required in order to protect the gates of LDMOS devices in this HV process.

The V_{GS} breakdown protection circuit referred to V_{GS} limit in Fig. 2 is designed using capacitive coupling technology as shown in Fig. 4. The input signal swings between V_{DD} and ground while the output voltage V_{out} swings between $V_{SS}+V_{DD}$ and V_{SS} . The transistor M1 is added here to ensure that while $V_{SS} < V_{Breakdown}$ (Zener diode's reverse breakdown voltage), the lower DC level of V_{out} is still able to be pulled down to V_{SS} .

C. Non-Regular Multiplexer

The multiplexer used in this design is used to switch the power supply of the 2nd and 3rd stage in order to provide a variable voltage gain based on the level of the supply voltage V_{DD} . Since the input voltage level to the multiplexer is unknown and is based on V_{DD} as well as the voltage gain, the select signal of this multiplexer has to be designed carefully.

Fig. 5 shows the circuit diagram of the non-regular multiplexer, which consists of NMOS select signal generator, PMOS select signal generator, and two pass transistors. For the NMOS select signal generator, as shown in Fig. 5a, while the input voltage is high, transistor M3 is turned off. The current only flows through M4 and the Zener diode to the ground, which outputs a voltage level of $V_{SS}+5V$. On the other hand, while the input voltage is low, V_1 will be pulled down. Transistor M4 operates in the weak inversion region and M6 is in the triode region. The voltage between the drain and source of M6 almost

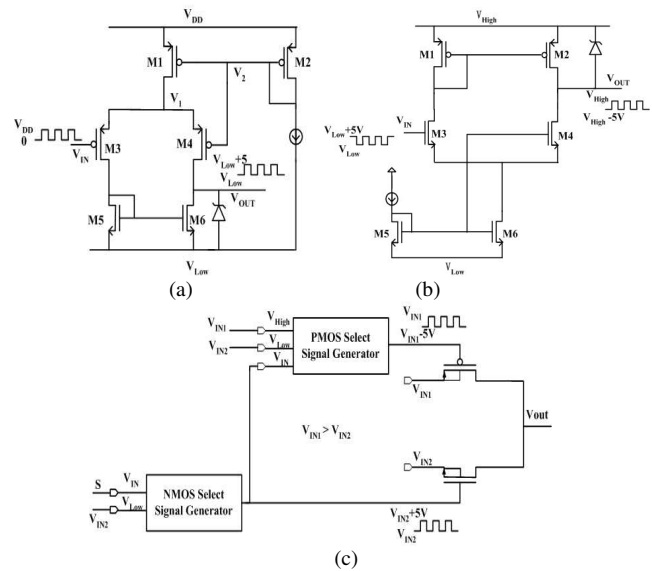


Fig. 5. Non-regular Multiplexer circuit design. (a) Select signal generator for NMOS. (b) Select signal generator for PMOS. (c) Detailed circuit diagram of the Non-regular multiplexer.

equals to zero in order to meet the zero current condition. The output voltage level is now pulled down to V_{SS} . Similarly, the output voltage of the PMOS select signal generator, as shown in Fig. 5b, is able to swing between V_{High} and $V_{High}-5V$. The reverse breakdown voltage of the Zener diode is 5V.

The design of the non-regular multiplexer uses GND and V_{DD} as the select signal and outputs a voltage level of V_{IN1} or V_{IN2} . As shown in Fig. 5c, V_{IN2} is the 2nd stage output voltage and V_{IN1} is the 1st stage output voltage, so we have $V_{IN2} < V_{IN1}$. When select signal S is high, the output voltage of the NMOS select signal generator is $V_{IN2}+5V$, which turns on the NMOS pass transistor and pulls V_{out} down to V_{IN2} . On the other hand, while select signal S is low, V_{out} is pushed up to V_{IN1} without a threshold voltage drop.

IV. POWER, AREA AND FREQUENCY CONSIDERATIONS

In order to design and implement a viable charge pump, it is required to have a minimum area and high power efficiency in modern IC technology to save the fabrication cost and power. In order to optimize the circuit performance, the tradeoff among the power, area, and frequency is analyzed.

Fig. 6 is the simplified diagram of the proposed negative charge pump circuit with the voltage gain of $-7X$. Each MOSFET has been replaced by two-phase switch. For the cross-coupled structure, the operating and charging phases are switched every half period. For example, suppose the loading current is I_0 , while the left half part of the circuit is being discharged by the load current, the right half part of the circuit is being charged from the power supply. In this case, the average current flowing from C_5 to $V_{out_2^{nd}}$ equals to I_0 during the operating phase. Simultaneously, C_6 is being charged by the same amount of average current I_0 in order to restore the charge that has been discharged during the operating period. At the 2nd output stage, the equivalent load current is now $2I_0$, consisting of the discharging currents flowing from C_5 and C_6 to $V_{out_2^{nd}}$. The average current flowing from the capacitors C_3 and C_4 to

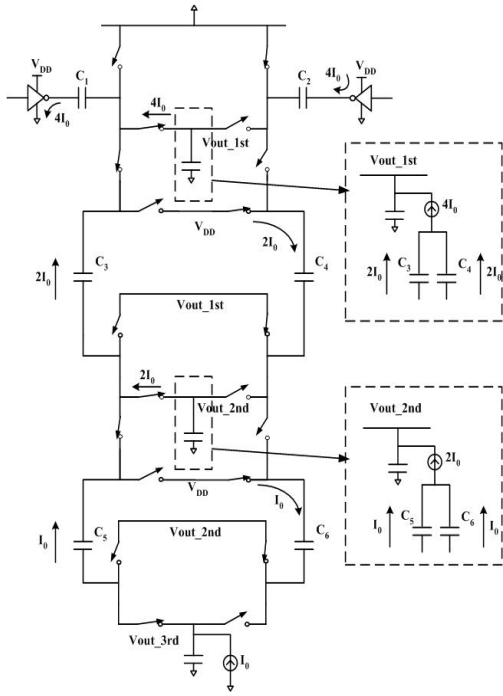


Fig. 6. Simplified circuit topology for the analysis of power, area, and frequency interaction

V_{out_1st} in the 2nd stage equals to $2I_0$ as well. Based on the same analysis, it is found that the equivalent loading current at the 1st output stage is $4I_0$ and the current flowing through C_1 and C_2 equals to $4I_0$ too. Given the analysis above, the output voltage of the proposed negative charge pump circuit with loading current I_0 can be calculated as follow:

$$\begin{aligned} V_{out_3rd} &= -7V_{DD} + 4I_0t / C_1 + 2I_0t / C_3 + I_0t / C_5 \\ &= -7V_{DD} + I_0t(4/C_1 + 2/C_3 + 1/C_5) \end{aligned} \quad (1)$$

For a given area, the lowest output voltage is obtained only when $C_1 = \sqrt{2}C_3 = 2C_5 = 2C$.

$$V_{out_3rd_{min}} = -7V_{DD} + \frac{(3 + \sqrt{2})I_0}{Cf} \quad (2)$$

For the input power, there are three sources:

$$P_{in} = 4V_{DD}I_0 + 2V_{DD}I_0 + V_{DD}I_0 = 7V_{DD}I_0 \quad (3)$$

Given the output voltage V_{out_3rd} and load current I_{load} , the output power is:

$$P_{out} = \langle V_{out_3rd} \rangle * I_{load} = P_{in} - P_{res} = 7V_{DD}I_{load} - \frac{(3 + \sqrt{2})I_0^2}{Cf} \quad (4)$$

Comparing (4) to (3), the second part is the resistive power loss P_{res} . The power efficiency can be calculated as follows:

$$PowerEfficiency = \frac{P_{out}}{P_{in}} = \frac{7V_{DD}I_0 - \frac{(3 + \sqrt{2})I_0^2}{Cf}}{7V_{DD}I_0} = 1 - \frac{(3 + \sqrt{2})I_0}{7V_{DD}Cf} \quad (5)$$

Equation (5) shows that higher power efficiency can be obtained by increasing the operating frequency of the charge pump

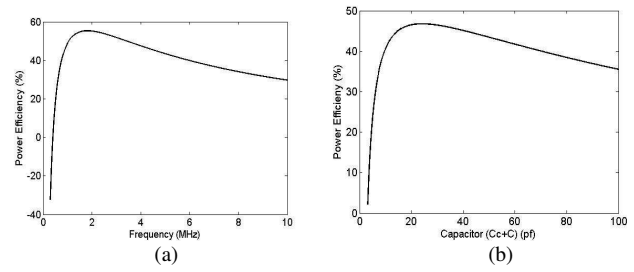


Fig. 7. Numerical simulation of power efficiency as a function of frequency and area. (a) Power efficiency vs. frequency @ $C=2C_C=2C_{MOS}=50\text{pf}$, $V_{DD}=2.5\text{V}$, $I_0=40\mu\text{A}$, and $\alpha=\beta=25\%$. (b) Power efficiency vs. area @ $V_{DD}=2.5\text{V}$, $I_0=40\mu\text{A}$, $C_{MOS}=25\text{pf}$, $\text{Freq}=5\text{MHz}$, and $\alpha=\beta=25\%$

circuit. However, this is not correct since the analysis so far has neglected the parasitic capacitance. A more accurate calculation of power efficiency can be approximately expressed as

$$\begin{aligned} PowerEfficiency &= \frac{P_{out}}{P_{out} + P_{res} + P_{dym} + P_{cont}} \\ &= \frac{7V_{DD}I_0 - \frac{(3 + \sqrt{2})I_0^2}{Cf} - \frac{(3 + \sqrt{2})\alpha I_0^2}{C_C f} - \frac{(3 + \sqrt{2})\beta I_0^2}{C_{MOS} f}}{7V_{DD}I_0 + (E_{C-C} + E_{C-MOS})f} \\ &= \frac{7V_{DD}I_0 f - (3 + \sqrt{2})\left(\frac{I_0^2}{C} + \frac{\alpha I_0^2}{C_C} + \frac{\beta I_0^2}{C_{MOS}}\right)}{(E_{C-C} + E_{C-MOS})f^2 + 7V_{DD}I_0 f} \end{aligned} \quad (6)$$

where C_C and C_{MOS} are the parasitic capacitance of MIM capacitors and transistors, respectively. E_{C-C} and E_{C-MOS} are the corresponding energy consumption due to the voltage switch, which is constant within one period and is the contribution of the dynamic power consumption P_{dym} . The resistive power loss need to be recalculated due to the parasitic capacitance too. As shown in (6), the value of αI_0 and βI_0 represents the equivalent current flowing through the parasitic capacitors and is determined by the technology used. The power consumption of function blocks such as the multiplexers and the clock phase generator is constant which is P_{cont} in (6). The value of C_4-6 has little effect on the power performance. It is chosen based on the maximum output voltage.

Fig. 7 shows the numerical simulation of power efficiency as a function of frequency and capacitors area. While the frequency increases, the power efficiency initially increases and then decreases as shown in Fig 7a. This means that for a given area there always exists an optimum switching frequency that could provide maximum power efficiency. As shown in Fig 7b, when the area of capacitors increased to a certain value, the power efficiency starts decreasing since the parasitic capacitors from the MOS transistors dominate the power performance. The parameters of the charge pump circuit can be optimized by sweeping the frequency and area repeatedly until the maximum power efficiency is obtained.

V. CIRCUIT SIMULATION AND OPTIMIZATION

Based on the analysis shown above, in order to have the maximum voltage gain, the capacitors from the 1st to the 3rd stage should be sized as $2:\sqrt{2}:1$. The capacitors in the third stage are connected in series in order to divide the voltage droop

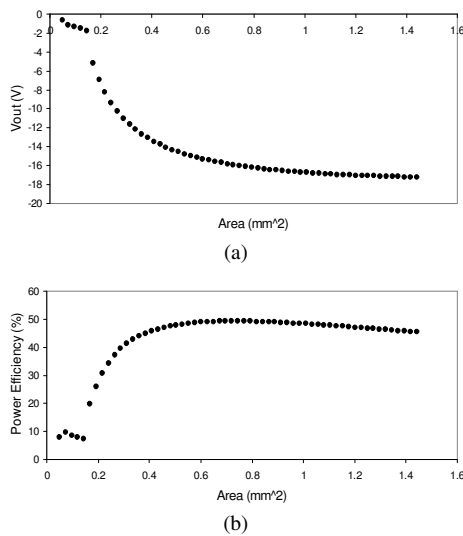


Fig. 8. Output voltage and Efficiency as a function of area @ 1MHz frequency with 40uA load current and 3V power supply. (a) Output voltage vs. Area. (b) Efficiency vs. Area.

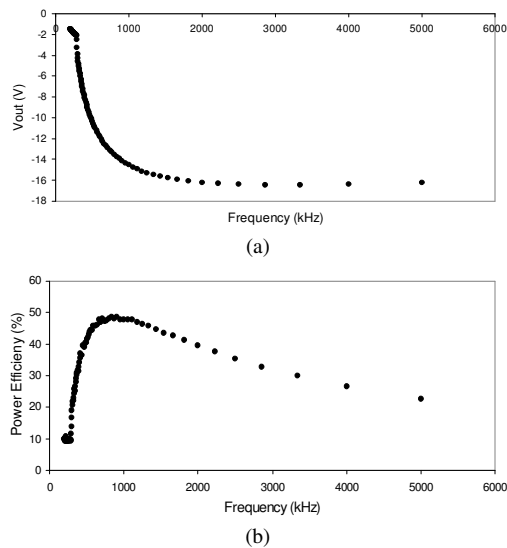


Fig. 9. Output voltage and Efficiency as a function of operating frequency @ 0.5 mm^2 area with 40uA load current and 3V power supply. (a) Output voltage vs. frequency. (b) Efficiency vs. frequency.

across the caps by 2. As a result, the area of the capacitors has increased by 4 times. In order to reduce the parasitic capacitance, we resized the cap ratio to 8:4:1.

In order to verify the effect of capacitance on the output voltage and power efficiency, the proposed charge pump is simulated at 1MHz with a current load of 40uA using 0.18um high voltage LDMOS technology. The parameters used in the numerical simulation depend on the process technology. Those values may not be exactly the same as in this specified design. As a result, we compare the relationship between the power efficiency and frequency & area only. The area discussed below is the overall area of the negative charge pump circuit which is proportion to the on-chip capacitance. As shown in Fig. 8a, the output voltage is inversely proportional to the area. The relation between the power efficiency and area, as shown in Fig. 8b,

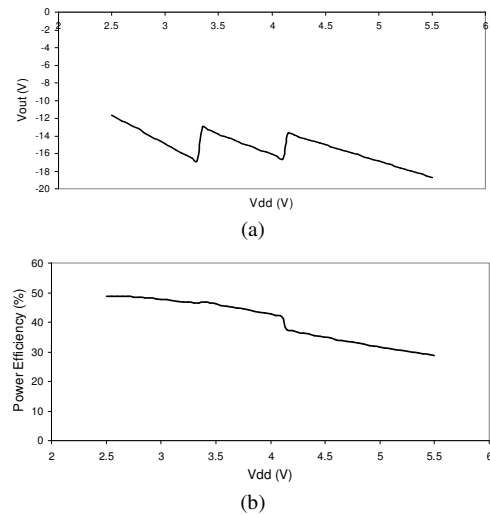


Fig. 10. Output voltage and efficiency of the negative charge pump circuit as a function of supply voltage with 40 uA load current. (a) Output voltage vs. V_{DD} @ 0.5 mm^2 area (b) Efficiency vs. V_{DD} @ 0.5 mm^2 area.

meets well with the numerical simulation results in Fig. 7b. Simulation of the charge pump shows an optimized overall chip area of 0.5 mm^2 as shown in Fig. 8 by taking into consideration of both output voltage and power efficiency.

Another important issue in charge pump operation is the operating frequency. Fig. 9 shows the output voltage and efficiency as a function of operating frequency. The output voltage is inversely proportion to the switching frequency as shown in Fig. 9a as expected from (2). The charge pump has a maximum efficiency of 50% at around 1MHz switching frequency as shown in Fig. 9b. A maximum efficiency is also expected from Fig. 7a, but the values are not the same as we discussed above. Taking both output voltage and efficiency as a function of operating frequency into consideration, the optimized frequency of 1MHz is selected.

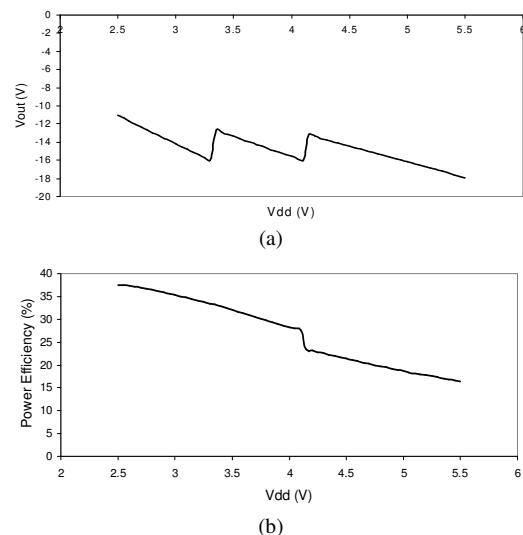


Fig. 11. Output voltage and efficiency of the negative charge pump circuit as a function of supply voltage with 40 uA load current. (a) Output voltage vs. V_{DD} @ 0.25 mm^2 area (b) Efficiency vs. V_{DD} @ 0.25 mm^2 area.

Given the optimized parameters, the proposed charge pump circuit is simulated with 40uA load current at 1MHz operating frequency. Fig. 10 shows the performance of the negative charge pump with the area of 0.5mm² and supply voltage range from 2.5V to 5.5V. The output voltage is within -15±3V with variable voltage gains of -4X, -5X, and -7X selected based on the supply voltage V_{DD}. The power efficiency of the proposed negative charge pump circuit varies from 30% to 50%, which is lower than the typical power efficiency of charge pumps using off-chip capacitors due to the high parasitic capacitances in the on-chip charge pump. In order to reduce the fabrication cost, the area is further reduced to 0.25mm². In this case, the output voltage is within -14.5±3.5V and the power efficiency is from 18% to 38% as shown in Fig. 11.

VI. CONCLUSION

In this work, a negative voltage charge pump circuit with variable voltage gain is designed and implemented using 0.18um high voltage LDMOS technology. The proposed charge pump circuit operates at 1MHz frequency with 40 uA load current with a wide power supply range from 2.5V to 5.5V. The losses caused by overlapping clock phases are eliminated by four clock phase scheme. In order to have a fixed output voltage within -15±3V, the voltage gain of the charge pump circuit is variable from -4X to -7X depending on the supply voltage. The proposed negative charge pump uses on-chip capacitors unlike the conventional charge pump. The measured results confirmed the functionality and performance of the proposed charge pumps. The proposed charge pump can be used as regulated power converter for applications that require high voltage supply.

REFERENCES

- [1] G. Palumbo, D. Pappalardo "Charge Pump Circuits: an Overview on Design Strategies and Topologies", IEEE Circuits and Systems Magazine, No. 1, pp. 31-45, January 2010.
- [2] G. Palumbo, D. Pappalardo, M. Gaibotti, "Charge Pump Circuits: Power Consumption Optimization," IEEE Trans. on Circuits and Systems part I, Vol. 49, No. 11, pp. 1535-1542, November 2002.
- [3] J. K. Dickson, "On-chip high voltage generation in NMOS integrated circuits using an improved voltage multiplier technique", *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 374 - 378, 1976.
- [4] J. Wu, Y. Chang, and K. Chang, "1.2V CMOS switched-capacitor circuits," *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, pp.388-389, February, 1996.
- [5] J. Wu and K. Chang, "MOS charge-pumps for low-voltage operation," *IEEE Journal of Solid-State Circuits*, Vol.33, No 4, pp. 592-597, April 1998.
- [6] C. C. Wang and J. C. Wu, "Efficiency improvement in charge pump circuits ", *IEEE J. Solid-State Circuits*, vol. 32, pp. 852 - 860, 1998.
- [7] Y. Moisiadis, I. Bouras, and A. Arapoyannoi, "A CMOS charge pump for low voltage operation ", *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 577 - 580, 2000.
- [8] TianRui Ying, Wing-Hung Ki, Mansun Chan, "Area-Efficient CMOS Charge Pump for LCD Drivers," *IEEE Jour. of Solid-State Circuits*, vol. 38, No. 10, pp. 1721-1725, Oct. 2003.
- [9] Nakagome, Y.; et al., "An experimental 1.5-V 64-Mb DRAM", *IEEE Journal of Solid-State Circuits (JSSC)*, Apr. 1991, pp. 465-4721.
- [10] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.
- [11] S. D'Arrigo, G. Imondi, G. Santin, M. Gill, R. Cleavelin, S. Spaglicca, E. Tomassetti, S. Lin, A. Nguyen, P. Shah, G. Savarese, D. McElroy, "A 5V-only 256k Bit CMOS Flash EEPROM", *ISSCC Digest of Technical Papers*, pp.132-3, Feb., 1989.
- [12] T. Tanzawa, T. Tanaka, K. Takeuchi, H. Nakamura, "Circuit Techniques for a 1.8-V-Only NAND Flash Memory," *IEEE Jour. of Solid-State Circuits*, vol. 37, No. 1, pp. 84-89, January 2002.
- [13] G. Palumbo, D. Pappalardo, M. Gaibotti, "Charge Pump with Adaptive Stages for Non-Volatile Memories," *IEE proc. Circuits, Devices and Systems*, Vol. 153, No. 2, pp. 136-142, April 2006.
- [14] Feng Su, Wing-Hung Ki, "Component-Efficient Multiphase Switched-Capacitor DC-DC Converter with Configurable Conversion Ratios for LCD Driver Applications," *IEEE Trans. on Circuits and Systems part II*, Vol. 55, No. 8, pp. 753-757, August 2008.
- [15] S. D'Arrigo, G. Imondi, G. Santin, M. Gill, R. Cleavelin, S. Spaglicca, E. Tomassetti, S. Lin, A. Nguyen, P. Shah, G. Savarese, D. McElroy, "A 5V-only 256k Bit CMOS Flash EEPROM", *ISSCC Digest of Technical Papers*, pp.132-3, Feb., 1989.
- [16] A. W. Ludikhuizen, "A Review of RESURF Technology", *Power Semiconductor Devices and ICs, 2000, The 12th International Symposium on May 22-25, 2000*, pp. 11-18.

Jun Zhao received the B.S. degree from Fudan University of Physical Electronics, Shanghai, China, in 2002 and the M.Engr. degree from Chinese Academy of Sciences, Beijing, China, in 2005. He is currently pursuing the Ph.D. degree in electrical and computer engineering from Northeastern University. His research interests include nanoscale CMOS design, high speed low power VLSI design, analog VLSI circuit design, electronic CAD, and ATE system design.

Evgeny V. Ivanov (M'02) received B.S.E.P. degree from Moscow Institute of Physics and Technology, Moscow, Russia, in 1982, B.S.E.E. degree from Moscow State Open University, Moscow, Russia, in 1986, and M.S.E.E. degree from University of Saskatchewan, SK, Canada, in 2000.

From 1986 to 1998, he worked as electro-optic instrumentation design engineer at Central Aerological Observatory, Moscow, Russia, and Kipp&Zonen, SK, Canada, and from 2000 to 2008, he worked as analog IC design engineer at Analog Design Automation and Kleer Semiconductor, Ottawa, Canada. In 2008 he joined Analog Devices as an analog IC design engineer in Wilmington, MA, USA. His interests are in precision analog circuit design. He is the author or coauthor of 16 scientific papers and 5 patents and recipient of 1997 ISA Analysis Division GTF best paper award.

Yong-Bin Kim (S'88-M'88-SM'00) received the B.S. degree in electrical engineering from Sogang University, Seoul, South Korea, in 1982, the M.S. degree from New Jersey Institute of Technology, Newark, and the Ph.D. degree from Colorado State University, in 1989 and 1996, respectively, both in electrical and computer engineering.

He is currently an associate Professor with the Department of Electrical and Computer Engineering, Northeastern University, Boston, MA.

From 1982 to 1987, he was with the Electronics and Telecommunications Research Institute, South Korea, as a Member of the technical staff. From 1990 to 1993, he was with Intel Corporation as a Senior Design Engineer, and involved in micro-controller chip design and Intel P6 microprocessor chip design. From 1993 to 1996, he was with Hewlett Packard Co., Fort Collins, CO, as a Member of technical staff, and involved in HP PA-8000 RISC microprocessor chip design. From 1996 to 1998, he was with Sun Microsystems, Palo Alto, CA, as an individual contributor, and involved in 1.5-GHz Ultra Sparc5 CPU chip design. From 1998 to 2000, he was an Assistant Professor with the Department of Electrical Engineering, University of Utah. His research focuses on low power analog circuit design, high-speed low power VLSI circuit design, and methodology.