Hybrid CMOS and CNFET Power Gating in Ultralow Voltage Design

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***Abstract*—This paper proposes a new hybrid MOSFET/carbon nanotube FET (CNFET) power-gating (PG) method using 32 nm technology in the ultralow-voltage region (∼0.4 V). Traditionally, PG is one of the most effective methods to reduce the power dissipation of systems in sleep mode, but it suffers from increased propagation delay and wake-up time due to the high-threshold voltage of power switches in the low-voltage region. In this paper, to reduce the propagation delay and wake-up time of the PG structure while keeping low leakage power in the sleep mode, the CNFET power switches are combined with silicon MOSFET logic cells. The proposed hybrid structure reduces the time gap in switching over from silicon MOSFET to CNFET technology. For the trade-off between wake-up overhead and leakage power saving, a new four-power-mode PG structure and a new two-pass PG structure using back-gate biasing of the CNFET switches are used. The simulation results of the proposed hybrid PG at 0.4 V are compared with those of the logic blocks without PG and the MOSFET PG structure using low-threshold voltage power switches. The simulation results show that the proposed hybrid structure reduces the total leakage power by 69.07%, the rush current by 5.13%, and the delay by 5.96%, on average, compared to the conventional PG structure for ISCAS85 benchmark circuits designed in 32 nm technology. More specifically, the proposed structure reduces the total leakage by 95.85% at the cost of 3% delay penalty compared to the logic blocks without PG for ISCAS85 benchmark circuits designed in 32 nm technology.**

***Index Terms*—Carbon nanotube FET (CNFET), multimode power gating, power gating (PG), two-pass power gating.**

I. Introduction

AS TECHNOLOGY scales down to 90 nm and below, the bulk CMOS technology has approached the scaling limit due to the increased short-channel effects, increased leakage power dissipation, severe process variations, high power density, and so on. To overcome this scaling limit, different types of materials have been experimented. Si-MOSFET-like carbon nanotube FET (hereafter called CNFET) devices have been evaluated as one of the promising replacements in the future nanoscale electronics. The reason that makes CNFETs a promising device is that they are compatible with high dielectric constant materials and a unique 1-D band-structure that restrains back-scattering and makes near-ballistic operation a realistic possibility. Using this CNFET, a high-k gate oxide can be deployed for lower leakage currents while keeping the on-current drive capability (compared to Si-MOSFET). CNFET has lower short-channel effect and a higher subthreshold slope than Si-MOSFET [1]–[7].

Despite this promising progress of CNFETs, CNFET has been applied only to a simple circuit design such as SRAM, ring oscillator, etc. because of the high fabrication cost of CNFETs and fabrication issues regarding imperfection and variability. Therefore, the fabrication of carbon nanotube (hereafter called CNT) at very large digital circuits on a single substrate has not been achieved. For cost-effective and reliable utilization of CNFETs and the time-gap reduction in migrating from silicon MOSFET to CNFET technology, the CNFET technology has been required to be combined with low-cost and reliable CMOS technology.

Although several papers have proposed the hybrid MOSFET/CNFET structure, the structure is only for simple circuits such as ring oscillator and inverting amplifier [8]–[10]. Hence, it is very important to find the best hybrid application in the large circuit design practicable in the state-of-the-art processing technology. In this paper, we propose a new MOSFET/CNFET power gating structure as a hybrid CMOS/CNFET circuit application which combines CNFETs with large silicon MOSFET logic circuits.

A conventional power gating (hereafter called PG) structure is one of the most well-known techniques to reduce the subthreshold leakage in sleep mode where a header and/or footer with high-threshold voltage (called sleep transistor) is added between actual power/ground rail and virtual power/ground node. By using this PG, the subthreshold leakage is significantly reduced by cutting off the high-$V_{\rm th}$ sleep transistor in the sleep mode [11]–[14]. However, the conventional PG structure is no longer effective in the low-voltage region because high $V_{\rm th}$ of the power switches degrades the operation frequency and increases wake-up time rapidly at the low voltage. To cope with this problem, a well-known scheme (named supercut-off CMOS) has been proposed, but it suffers from reduced performance and long wake-up time [15], [16].

As a solution to these issues at the low voltage, in this paper, the MOSFET sleep transistors are replaced by CNFET sleep transistors while MOSFETs are still used for all the cells of logic blocks connected to the sleep transistors.

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In the PG structure, digital blocks are placed on the virtual power/ground generated by the sleep transistor. If the hybrid MOSFET/CNFET structure is applied to the PG application, the digital block as a hardcore can be implemented using the silicon CMOS. On the other hand, a small number of sleep transistors are separated from the digital hardcore and can be implemented using the CNFET device. That is, in the PG structure using the hybrid MOSFET/CNFET, a large number of complex digital blocks are fabricated using low cost and reliable CMOS technology, and a small number of simple sleep transistors are fabricated using state-of-the-art CNFET technology.

This highly cost-effective hybrid technique is implemented and compared with the cell-modified hybrid techniques. There is no question about the fact that the PG structure is one of the best circuit topologies to which the hybrid MOSFET/CNFET technology can be applied.

Another disadvantage of the conventional PG structure is that the virtual ground rail takes a long time (known as wake-up time or latency) to discharge through the sleep transistor when the PG circuit switches from the sleep mode to the active mode. After the wake-up time, circuits are functional and start working at its full operating speed. At the same time, this discharging current brings about a significant wake-up power that can exceed overall leakage saving in sleep mode depending on the number of sleep-to-active mode transitions and the length of their sleep cycles. In order to minimize this wake-up penalty while keeping low leakage power, several multimode PG structures have been suggested. However, these techniques require complicated timing control circuitry or additional bias generation circuitry for a sleep transistor [17], [18]. Therefore, this paper proposes a different novel multimode hybrid PG structure for the tradeoff between wake-up overhead and leakage savings, which employs four different modes (Active, Standby1, Standby2, and Sleep) using a simple back-gate biasing in weak CNFET sleep transistors. In addition to the hybrid structure, a new two-pass PG structure is also proposed to reduce the excessive wake-up rush current by using the back-gate biasing and a sequence for turning ON the CNFET switches.

In this paper, silicon MOSFET circuits have designed using 32 nm predictive technology model [19]. In addition, for PG footers in the proposed hybrid PG, the 32 nm Stanford CNFET HSPICE model [18] has been employed.

II. Carbon Nanotube FET

Carbon nanotube FETs employ semiconducting single-wall carbon nanotubes to assemble electronic devices, and the single-walled CNFET is obtained by replacing the channel of a conventional MOSFET with carbon nanotubes (a 1-D conductor obtained by rolling a sheet of graphite) as shown in Fig. 1 [5], [6]. The nanotubes can be either a metallic (conductor) or a semiconducting (semiconductor) depending on the angle (represented as a chirality integer vector (n, m)) of the atom arrangement along the nanotube. The nanotube is metallic if $(n = m)$ or $(n - m =$ "a multiple of 3"); otherwise, the tube is semiconducting.

The CNFET device has four terminals (drain, gate, source, and back-gate); a dielectric film is wrapped around a portion of the undoped nanotube in the intrinsic region, and a metal gate surrounds the dielectric while the other nanotube regions are heavily doped for a low series resistance during the on-state. As shown in Fig. 1(a), the top-gated CNFETs are fabricated on an oxidized Si substrate that can be used as a back-gate in the CNFET. In the early 1990s, most CNFETS studied had adopted a back-gate top-contact structure [20], [21], in which the nanotubes are grown on a conducting substrate covered by an insulating layer. Two metal contacts are deposited on the nanotube to serve as source and drain electrodes while the conducting substrate is the gate electrode in the three-terminal device. However, these early CNFETs are found to have poor device characteristics such as an ambipolar transistor characteristic and gentle subthreshold swing. In order to improve the poor device characteristics, dual-gate CNFET structures have been proposed. The structures show a MOSFET-like unipolar transistor characteristic, excellent subthreshold slopes, and a drastically improved OFF state. Each device has one or more single-wall semiconducting carbon nanotubes. The currents of the CNFET device are controlled by adjusting device parameters such as gate length (Lch), the number of nanotubes, chirality vector, and pitch between nanotubes [2], [22]. As the gate voltage increases or decreases, the device is electrostatically turned ON or OFF through the gate node.

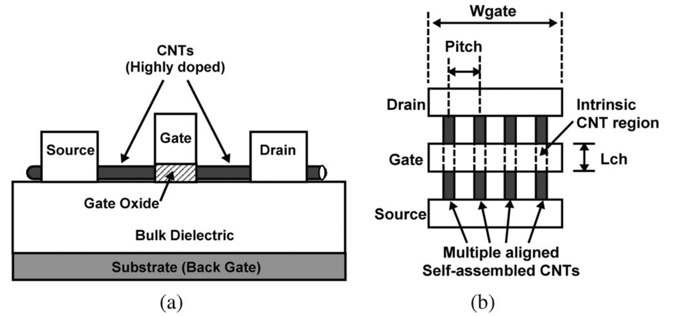


Fig. 1. CNFET structure. (a) Cross-sectional view. (b) Top view.

The drain current characteristics of a 32-nm N-type CNFET are presented in Fig. 2, where the characteristics are compared to those of the N-type MOSFET. $I_{\rm DS}$ (drain current) of the CNFET is saturated at higher $V_{\rm DS}$ (drain-to-source voltage) as $V_{\rm GS}$ (gate-to-source voltage) increases as shown in Fig. 2(a), where the amount of $I_{\rm DS}$ of the CNFET is greater than that of the MOSFET although the CNFET width is 6.35 nm (5 nm of the pitch length and 1.35 nm of the diameter) and the MOSFET width is 64 nm. According to the simulation results, it is possible to reduce the device size by approximately an order of magnitude if the CNFET is replaced with the MOSFET.

In the subthreshold (weak inversion) region, the characteristics of the CNFET show that $I_{\rm DS}$ of the CNFET is much greater than that of MOSFET and the CNFFET almost does not have drain-induced barrier lowering (DIBL) and gate-induced drain leakage (GIDL) effects. As shown in the figure, CNFET on-current is higher and leakage current is lower than the MOSFET transistor. Fig. 2(b) illustrates $I_{\rm DS}$ characteristics of the N-type CNFET in the weak inversion region, which implies that the

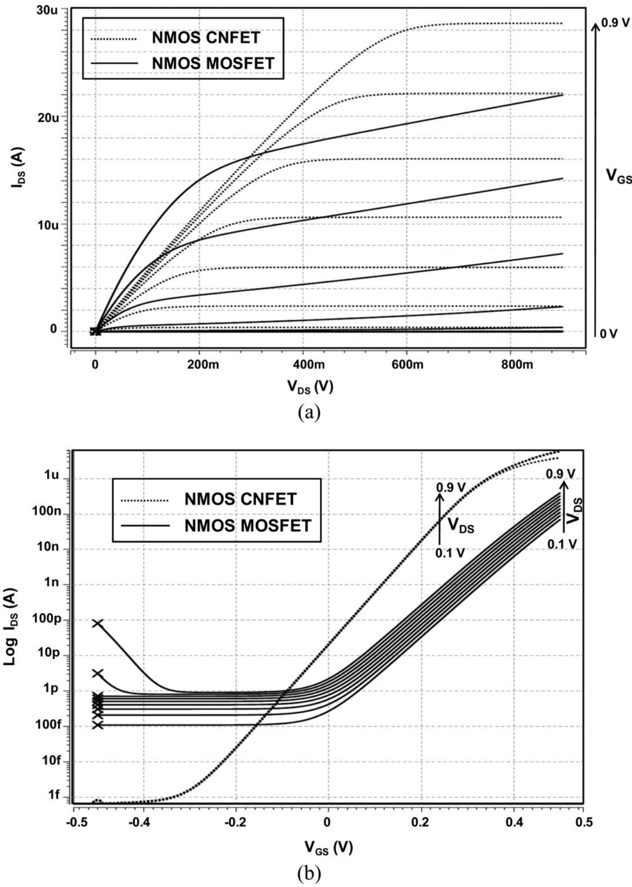


Fig. 2. Drain current of a 32-nm N-type CNFET and a 32-nm N-type MOSFET as a function of (a) drain-to-source voltage for different gate-to-drain voltage, (b) gate-to-source voltage for different drain-to-source voltage, where (n, m) of the CNFET is (17,0), the number of nanotubes of the CNFET is 2, the width of the MOSFET is 64 nm, the back-gate voltage is 0 V, and the temperature is 25 °C.

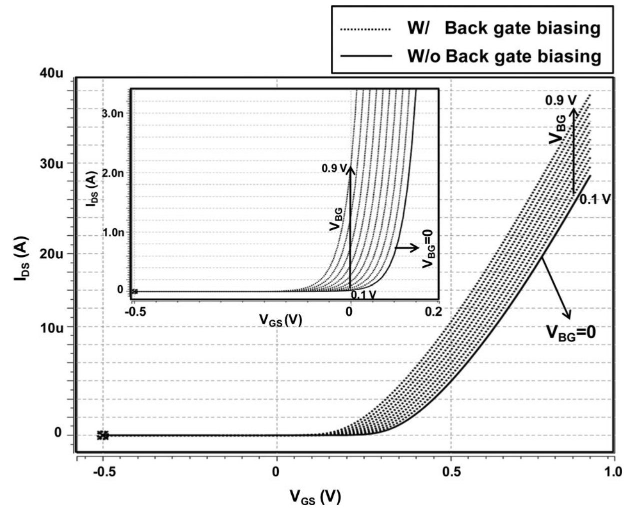


Fig. 3. Drain current of a 32-nm N-type CNFET as a function of gate-to-source voltage for different back-gate voltage, where (n, m) of the CNFET is (17,0), the number of nanotubes of the CNFET is 2, the width of the MOSFET is 64 nm, and the temperature is 25 °C.

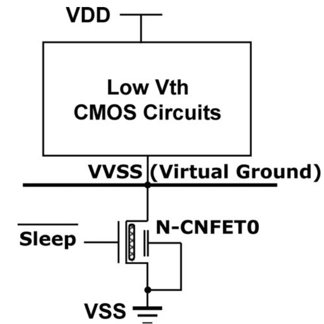


Fig. 4. Hybrid PG structure having a CNFET footer.

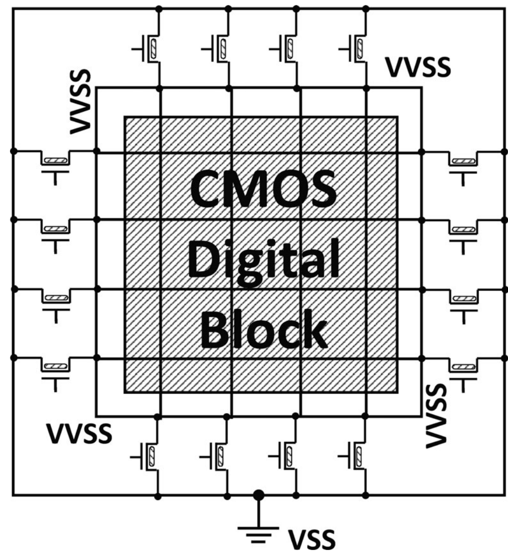


Fig. 5. Ring style PG implementations.

CNFET would be a more practical solution even in the subthreshold logic design requiring a smaller area than the MOSFET.

Fig. 3 shows the back-gate voltage $V_{\rm BG}$ impact on the drain current $I_{\rm DS}$ of a 32-nm NMOS CNFET; $V_{\rm BG}$ increases $I_{\rm DS}$ approximately by 30% depending on the top-gate voltage $V_{\rm GS}$. Especially, a small amount of drain current can be generated by $V_{\rm BG}$ at zero gate voltage. In this paper, the back-gate is deployed for the multimode PG structure and two-pass PG structure.

III. Hybrid PG Structure

This section proposes a new hybrid MOSFET/CNFET PG structure for cost-effective and reliable utilization of CNFETs. The new hybrid structure addresses the low-performance issue caused by high $V_{\rm th}$ of the conventional MOSFET PG structure at the low voltage while keeping low leakage power dissipation in sleep mode. Fig. 4 shows the hybrid PG structure diagram, where an N-CNFET (footer) is placed in series with low-$V_{\rm th}$ CMOS circuits, and the back-gate node of the N-CNFET is connected to the ground, and a PG implementation style (so-called ring-style implementation) used for the proposed hybrid PG structure is presented in Fig. 5. In the ring style

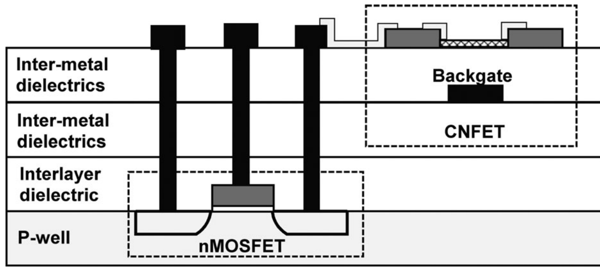


Fig. 6. Cross section of a silicon NMOS with CNFET integration.

implementation, a ring of V_{SS} surrounds the sleep transistors. A ring of sleep transistors connects V_{SS} to a virtual V_{SS} mesh that covers the silicon MOSFET digital block. The ring style switching network is the only style that can be used to power-gate an existing digital hardcore; hence, it is suitable for the proposed hybrid PG structure. Fig. 6 presents an example of hybrid MOSFET/CNT integration which is a three-mask optical lithography fabrication process suggested in [23].

The MOSFET/CNFET PG scheme is the same as the MOSFET PG scheme. However, the device parameters of the CNFET footer are different from those of the MOSFET footer. Therefore, the main issue in the hybrid PG structure is to find the optimum CNFET device parameters to achieve high speed in active mode and low leakage power in sleep mode. First of all, the optimum threshold voltage should be determined for the speed and leakage power of the PG structure because the current–voltage characteristics of the CNFETS are similar to those of MOSFET as follows [24]. First of all, the drain-to-source current of CNFET is given by

$$I_{\rm CNFET} = n \cdot g_{\rm CNT}(V_{\rm DD} - V'_{\rm SS} - V_{\rm th,CNT}) \tag{1}$$

where n is the number of nanotubes per device, $V_{\rm th,CNT}$ is the threshold voltage, $g_{\rm CNT}$ is the transconductance per nanotube, and $V'_{\rm SS}$ is the voltage drop between the inner source and the external source node. In the CNFET device, the channel threshold voltage of the CNFET device can be derived from an inverse function of the diameter of a CNFET as follows [24]:

$$V_{\rm th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{\rm CNT}} \tag{2}$$

where E_g is the band-gap energy, a (~2.49 Å) is the interatomic distance between each carbon atom and its neighbor, V_π is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, and $D_{\rm CNT}$ is the carbon nanotube diameter calculated using the following equation [24]:

$$D_{\rm CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \tag{3}$$

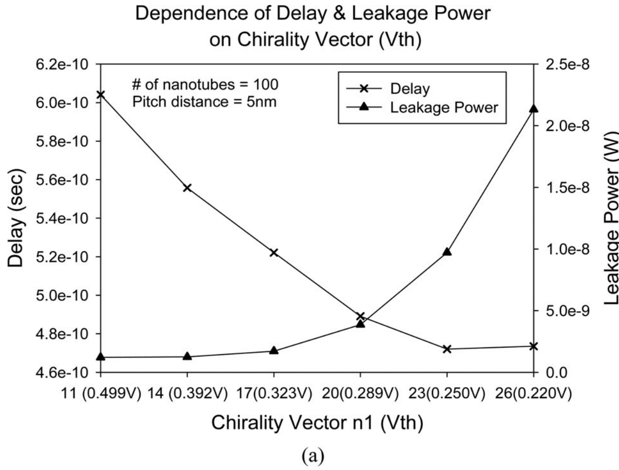
where $n1$ and $n2$ are the chirality vector which is represented by the integer pair ($n1$, $n2$).

Therefore, the diameter of CNFET given by the chirality vector ($n1$, $n2$) should be first assigned to determine the threshold voltage of CNFET. Besides this, there is a couple of more critical parameters in calculating CNFET current, which are the number of nanotubes as can be seen in (1) and the pitch between nanotubes since the screening effect between nanotubes is determined by the pitch.

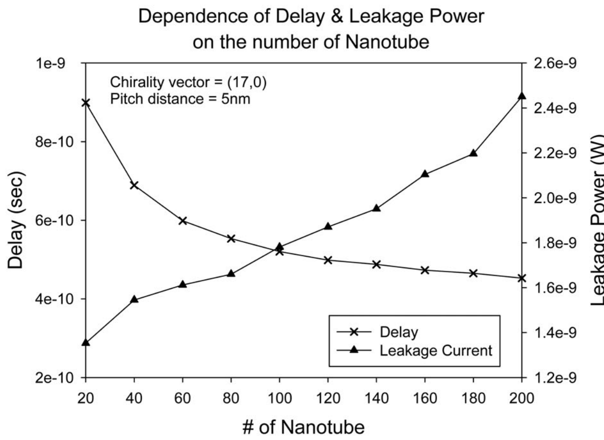
The main leakage component of CNFET in the subthreshold region is caused by the band-to-band tunneling (BTBT) mechanism through the semiconducting subbands [2], [25]. The BTBT current from drain to source is affected by $V_{\rm th}$ (chirality vector) and the number of nanotubes. The other leakage currents are relatively small and can be reduced by new device techniques such as high-k dielectric material. Fig. 7 shows the impact of CNFET device parameters (the chirality vector, the number of nanotubes, and the pitch distance) on the circuit delay and the leakage power in a hybrid PG structure consisting of a CNFET footer and 20 MOSFET inverter chains having 20 inverters per chain designed using 32 nm technology. In the simulation, the chirality vector of the footer is changed from (11,0) to (26,0), the supply voltage is 0.9 V, and the temperatures are 25 °C (for leakage measurement) and 125 °C (for delay measurement).

The simulation results show that the delay and leakage power are more affected by the chirality vector and the number of nanotubes than the pitch distance. Especially, the delay-leakage power product significantly increases at around chirality vector of (17,0). The results also show that the product has a minimum value when the number of nanotube is around 100. In order to compare the hybrid PG structure with the conventional MOSFET PG structure, the same inverter chains using the MOSFET PG structure are simulated, where the footer size is 10% of the total NMOS width in the inverter chain. The simulation results show that the delay and leakage power of the MOSFET PG structure are 0.5055 n and 1.741 nW, respectively. From these simulation results, it is demonstrated that the hybrid PG structure can decrease the delay and leakage power of the PG structure using a smaller footer (about 1% of the total NMOS width in the inverter chain) compared to its MOSFET counterpart.

As the power supply voltage decreases below 0.9 V, the advantage of the hybrid PG structure becomes manifest. Fig. 8(a) presents the simulation results showing the impact of the power supply voltage on the circuit delay of the hybrid PG and MOSFET PG. The simulation results are compared with those of the inverter chains without PG footer. The area overhead of the MOSFET PG is 10% of the total NMOS width, and the area overhead of the hybrid PG is 1% (number of nanotube = 100, pitch = 5 nm, and chirality vector = (17,0)) of the total NMOS width. As $V_{\rm DD}$ decreases below 0.7 V in active mode, the hybrid PG structure becomes faster than the MOSFET PG structure by factor of more than two (2), and its delay decreases by 70% compared to the MOSFET PG structure at 0.5 V. Moreover, the delay of the MOSFET PG structure is exponentially increased at $V_{\rm DD}$ below 0.6. In addition, as the supply voltage scales down, the wake-up time (sleep-to-active mode transition time) of the MOSFET PG structure significantly increases due to the high threshold voltage of the MOSFET footer as shown in Fig. 8(b). On the other hand, the wake-up time of the hybrid PG structure increases a little, which is small enough to be ignorable compared to the wake-up time of the MOSFET PG. These simulation results demonstrate that the proposed hybrid MOSFET/CNFET PG structure is very effective in the low-voltage region.



(a)



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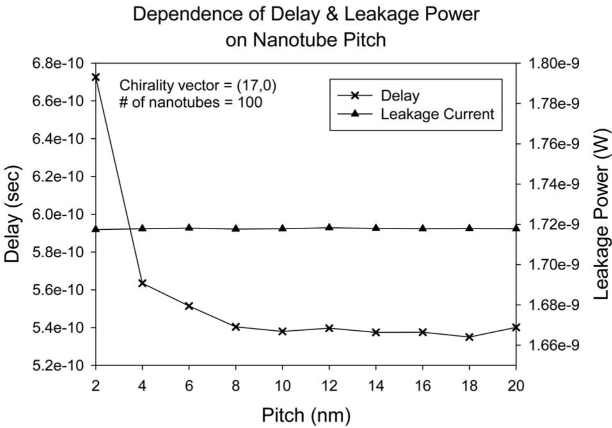
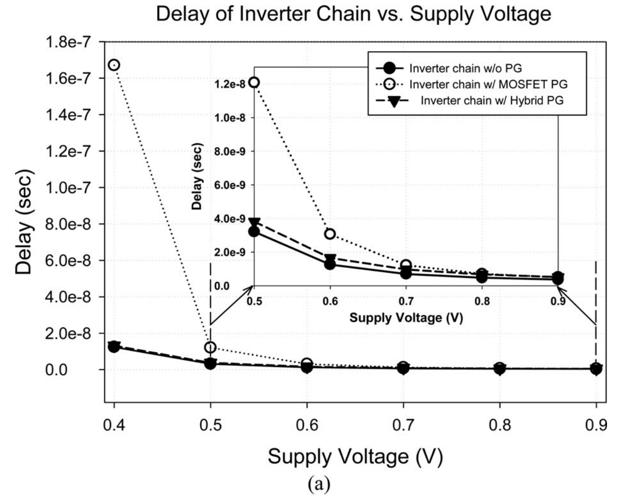
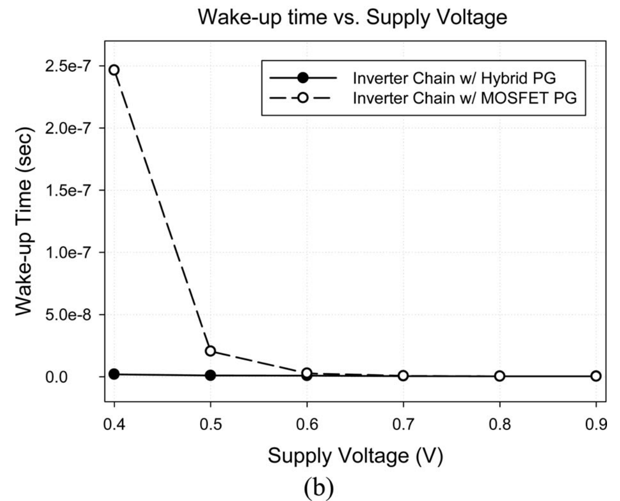


(c)

Fig. 7. Impact of CNFET device parameters on the speed and leakage power. (a) Chirality vector. (b) # of nanotubes. (c) Pitch distance.



(a)



(b)

Fig. 8. Delay and Wake-up time dependence of PG structure on supply voltage. (a) Delay dependence of PG on supply voltage. (b) Wake-up time dependence of PG on supply voltage.

IV. Imperfections and Variations

The current CNFET fabrication technique is far from ideal. CNFET has been applied only to a simple circuit design such as SRAM, ring oscillator, etc. because of the high fabrication cost and fabrication issues regarding imperfection and variability. Therefore, the fabrication of CNT at very large digital circuits on a single substrate has not been achieved. Hence, it is very important to find the best hybrid application in the large circuit design practicable in the state-of-the-art processing technology. The PG structure can be one of the best applications because in the PG structure using the hybrid MOSFET/CNFET, a large number of complex digital blocks are fabricated using low cost and reliable CMOS technology and a small number of simple sleep transistors are fabricated using state-of-the-art CNFET technology.

Although fabrication of CNFET-based sleep transistors still faces some challenges consisting of imperfection and variability, the number of sleep transistors is much smaller than that of silicon digital circuits and the structure is very simple. In order to mitigate the CNFET fabrication problems such as metallic CNTs, CNT density variations, CNT diameter variations, mispositioned and misaligned CNTS, etc., several state-of-the- art techniques have been proposed [26]–[31]. Most of these imperfections and variations are caused by nonidealities in the CNT synthesis process. For mitigation of metallic carbon nanotubes in CNFET Transistors, asymmetrically correlated CNT (ACCNT) [26], [27] as well as innovative process enhancements

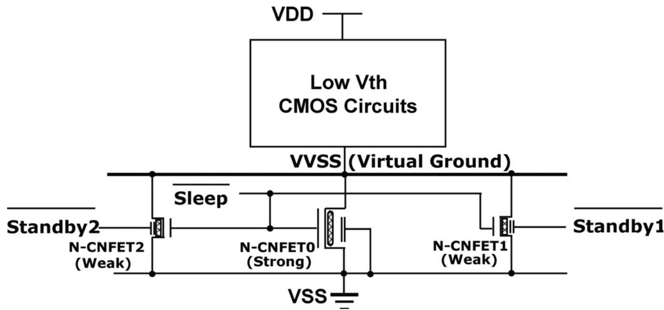


Fig. 9. Block diagram of the proposed multimode PG.

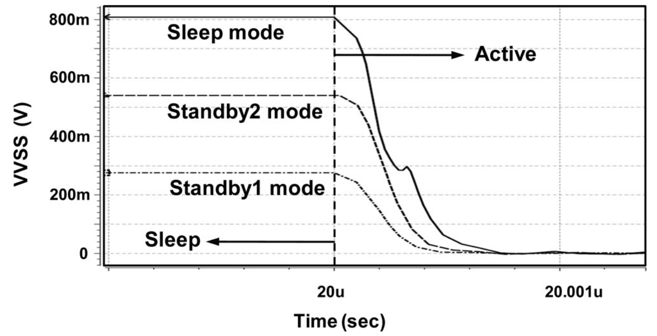


Fig. 10. Virtual ground of the multimode hybrid PG.

such as metallic CNT removal/separation [28], [29] has been proposed. In [30] and [31], novel imperfection-immune design methodologies have been developed to overcome CNT density variations and to build compact layouts while ensuring 100% functional immunity to mispositioned CNTs, respectively. In this paper, it is assumed that the CNFET-based sleep transistor is an ideal CNFET transistor using Stanford CNFET model for focusing on the hybrid design methodology.

Although the CNFET-based sleep transistor is not an ideal CNFET, the imperfections and variations of CNFET sleep transistors can be mitigated by the conventional gate-voltage controlled method [32] and/or by the selection the number of on-state sleep transistors in the active mode [33]: the gate voltage of each sleep transistor determines the performance and leakage power of the PG structure; hence, we can compensate imperfections and device variations in active and sleep mode through the conventional sleep signal controlling system. Besides the gate-voltage controlled method, the number of on-state sleep transistors also determines the performance of the PG structure in active mode. In both methods, a replica circuit for monitoring critical path such as a ring oscillator is required to detect the variations in the PG structure.

V. Multimode Power Gating

During the short mode transition time from sleep to active, the conventional PG suffers from large wake-up time and wake-up power. Especially, frequent power mode transitions during a short period cause larger wake-up power dissipation than the leakage power savings. Therefore, it is better to put logic circuits into several power saving modes which trade leakage saving for this wake-up overhead. The number of power saving modes depends on system applications, and idle cycles required to enter each power mode is determined by a tradeoff between the wake-up overhead and leakage savings. In this section, a new PG structure using the back-gate biasing shown in Section II is proposed to support four operating modes (Active, Standby1, Standby2, and Sleep). When the back-gate biasing is applied to CNFET where the top-gate voltage is zero, very small on-current is obtained as shown in Fig. 3. The current is much smaller than the regular on-current (top-gate voltage $= V_{\mathrm{DD}}$) of CNFET, but larger than the subthreshold current of CNFET.

Fig. 9 shows our new PG structure in which N-CNFET1 and N-CNFET2 having smaller size compared to N-CNFET0 are added to the hybrid PG structure shown in Fig. 4. Each power mode is easily obtained by the two control signals (Standby1 and Standby2) and threshold voltage difference between CNFET1 and CNFET2.

TABLE I
Wake-up Penalty and Leakage Current of the PG Structure

	Power-Mode		
	Standby1	Standby2	Sleep
Wake-up Time	1.53E-10	2.41E-10	2.63E-10
Avg. Wake-up Power	5.86E-06	1.98E-05	4.55E-05
Avg. Leakage Current	1.68E-07	2.16E-08	2.09E-09

In the Active mode, both control signals (Standby1 and Standby2) are set to “1,” and Sleep signal is “0,” which means that all the transistors are fully turned ON and the back-gate voltage of each CNFET is “0.” In the Standby1 mode, Sleep signal and Standby2 signal are “1,” and only Stadnby1 signal is set to “0,” which means that only N-CNFET1 is partially turned ON by the forward back-gate biasing. In the Standby2 mode, only Stadnby2 signal is set to “0,” and then N-CNFET2 is partially turned ON by the forward back-gate biasing. Although the N-CNFET1 and N-CNFET2 have the same small size, the current through N-CNFET2 is smaller than through N-CNFET1 because the smaller V_{th} (than that of N-CNFET2) is assigned to N-CNFET1 using the chirality vector of each N-CNFET. Therefore, the virtual ground (VVSS) in Standby2 mode is greater than that in Standby2 mode.Finally, in the Sleep mode, Sleep, Standby1, and Standby2 signals are changed to “1,” and all the transistors are fully turned OFF.

Fig. 10 demonstrates the effectiveness of the proposed multimode PG structure using 20 inverter chains and shows the virtual ground voltages of three different modes in the sleep-to-active transition. The simulation setup is as follows: 1) the chirality vector of N-CNFET0, N-CNFET1, and N-CNFET2 is (17,0), (19,0), and (16,0), respectively. (2) The number of nanotubes of each N-CNFET is 100, 10, and 10, respectively. (3) The pitch distance of all the N-CNFETs is 5 nm. Table I shows the wake-up time, wake-up power, and leakage current of each power mode. The results present that each power mode has different wake-up penalties and leakage savings. Based on this tradeoff between the wake-up penalty and leakage savings, a power mode should be set in the system during idle cycles.

VI. Two-Pass Power Gating

This section proposes a new two-pass PG using the hybrid CMOS/CNFET structure. The conventional two-pass PG structure consists of weak footers and strong footers, considering a tradeoff between wake-up time and rush current [34], [35]. At sleep-to-active transition time, the weak transistors are turned ON first so as to mitigate the impact of the rush currents on the strong footers. When the design is discharged (or charged) to a voltage close to zero (or $V_{\rm DD}$), all the strong footers are turned ON and are ready for normal operation as shown in Fig. 11(a). The new method is to use the back-gate biasing of CNFET power switches instead of the weak footers. The weak-footer's impact on the PG structure is the same as that of the back-gate biasing since a small on-current would be obtained by the weak footer and the back-gate biasing. Fig. 11(b) shows the proposed PG structure. At wake-up time, each back-gate is turned ON first in regular order according to the sleep signal. When the virtual ground (VVSS) is discharged to the voltage close to zero, each top gate is also turned ON in regular order. In order to show the efficiency of the proposed structure, the simulation results of the 20 inverter chains (each chain has 40 inverters using 32 nm MOFET technology) with the CNFET footers are presented in Fig. 11(c), where the chirality vector of N-CNFET footers is (17,0), the number of nanotubes of each strong footer and weak footer is 10 and 2, respectively, and the pitch distance of all the N-CNFETs is 5 nm.

Fig. 11(c) demonstrates that the new two-pass PG structure is compatible with the conventional two-pass PG. The amount of wake-up time and rush current of the new two-pass PG is almost equal to that of the conventional two-pass PG. Therefore, it is possible for the new two-pass PG to consider a tradeoff between the wake-up time and the rush current without any weak footer, which means that the new PG has less physical complexity and smaller area compared to the conventional two-pass PG. In addition, the on-current drive capability of each CNFET footer in active mode would be increased because the top-gate and the back-gate are biased at the same time, which leads to footer size reduction under the condition of a fixed gate delay.

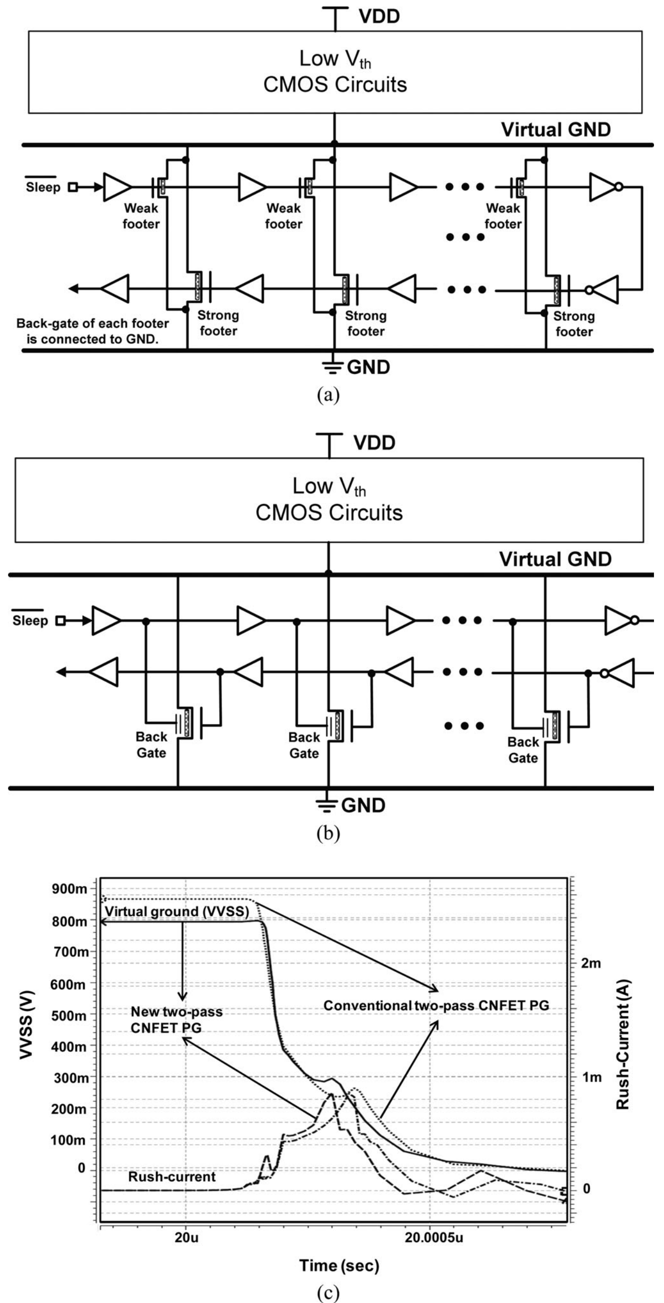


Fig. 11. Proposed two-pass PG structure. (a) Block diagram of the conventional two-pass PG. (b) Block diagram of the new two-pass PG. (c) Comparison between simulation results of the C432 circuit.

VII. Simulation Results

The proposed hybrid MOSFET/CNFET PG structure has been implemented and evaluated using ISCAS 85 benchmark circuits designed in 32 nm predictive technology model [19] at 0.9 and 0.4 V supply voltages. For NMOSFET in the ISCAS85 circuits, a high-k metal gate with $V_{\rm th0} = 0.49$ V and $t_{\rm ox} =$ 1.15 nm is used, and for PMOS in the ISCAS85 circuits, a high-k metal gate with $V_{\rm th0} = -0.49$ V and $t_{\rm ox} = 1.2$ nm is used. For PG footers in the proposed hybrid PG, the 32 nm Stanford CNFET HSPICE model [18] has been employed, where the chirality vector of the N-CNFET footer is (17,0) and the pitch distance of the N-CNFET footer is 5 nm.

To make a comparison between the proposed hybrid two-pass PG and the conventional two-pass PG structure, high-$V_{\rm th}$ voltage NMOSFET footers with $V_{\rm th0} = 0.63$ and $t_{\rm ox} = 1.6$ nm are employed for the conventional PG at 0.9 V, whereas low-$V_{\rm th}$ voltage NMOSFET footers with $V_{\rm th0} = 0.49$ and $t_{\rm ox} =$ 1.15 nm are employed for the conventional PG at 0.4 V since the high-$V_{\rm th}$ NMOSFET footers are no longer effective in the ultralow-voltage region.

In addition, to get more accurate results, a power network model is used, where L (bonding/package inductance) is 2 nH, R (supply network resistance) is 0.05 Ω, and C (supply network capacitance) is 0.05 pF [36]. The MOSFET footer size is 10% of the total NMOS width in each original logic block, whereas the size of the CNFET footer is 1% of the total NMOS width. All the simulation results have been measured using random input

TABLE II
SIMULATION RESULTS FOR ISCAS85 CIRCUITS ($V_{\mathrm{DD}} = 0.9$ V)

Logic	Normalized by Logic Block (w/o PG)		Normalized by Conventional PG (with **high-Vth NMOSFET footers**)				
	Avg. Leakage Power	Delay	Avg. Leakage Power	Delay	Wakeup Time	Rush Current	Area
C432	0.004	1.053	1.640	0.975	0.914	0.884	0.1
C499	0.001	1.074	1.449	0.986	0.769	0.917	0.1
C880	0.006	1.121	1.175	0.958	0.857	0.313	0.1
C1355	0.007	1.050	1.160	0.968	0.859	0.432	0.1
C1908	0.003	1.038	1.462	0.988	0.873	0.432	0.1
C2670	0.003	1.061	1.300	0.963	0.840	0.440	0.1
C3540	0.002	1.030	1.059	0.974	0.795	0.581	0.1
C5315	0.003	1.038	1.432	0.985	0.796	0.798	0.1
C6288	0.003	1.133	0.985	0.986	0.866	0.583	0.1
C7552	0.002	1.062	1.187	0.928	0.671	0.620	0.1
Avg. Reduction Rate	**-99.65** (%)	**6.59**(%)	**28.48** (%)	**-2.89** (%)	**-17.61** (%)	**-39.01** (%)	**-90** (%)

Note: The conventional PG in this experiment deploys high-V_{th} NMOSFET footers.

TABLE III
SIMULATION RESULTS FOR ISCAS85 CIRCUITS ($V_{\mathrm{DD}} = 0.4$ V)

Logic	Normalized by Logic Block (w/o PG)		Normalized by Conventional PG (with **low-Vth NMOSFET footers**)				
	Avg. Leakage Power	Delay	Avg. Leakage Power	Delay	Wakeup Time	Rush Current	Area
C432	0.049	1.005	0.335	0.981	1.940	0.777	0.1
C499	0.079	1.033	0.500	0.966	1.128	0.944	0.1
C880	0.047	1.028	0.353	0.977	1.132	1.112	0.1
C1355	0.050	1.041	0.271	0.961	1.262	1.272	0.1
C1908	0.030	1.011	0.288	0.990	1.114	0.905	0.1
C2670	0.032	1.041	0.280	0.802	1.063	0.862	0.1
C3540	0.029	1.019	0.221	0.982	0.99	0.845	0.1
C5315	0.035	1.040	0.274	0.981	0.946	0.969	0.1
C6288	0.037	1.047	0.332	0.775	1.143	1.065	0.1
C7552	0.029	1.006	0.238	0.991	0.745	0.735	0.1
Avg. Reduction Rate	**-95.85** (%)	**2.72**(%)	**-69.07** (%)	**-5.96** (%)	**14.64** (%)	**-5.13** (%)	**-90** (%)

Note: The conventional PG in this experiment deploys low-V_{th} NMOSFET footers.

test vectors at two temperatures (25 °C for sleep and 125 °C for active mode).

First, Table II presents the simulation results for ISCAS85 benchmark circuits at $V_{\mathrm{DD}} = 0.9$ V. The leakage power, circuit delay, wake-up time, and rush current of the proposed hybrid PG structure are normalized with respect to those of the conventional PG structure with high-V_{th} footers. Also, the leakage power and circuit delay of the proposed hybrid PG structure are normalized with respect to those of logic blocks without PG structure. The simulation results show that the proposed hybrid PG structure reduces the wake-up time by 17.61%, the rush current by 39.01%, the delay by 2.89%, and the area by 90% on average for the ISCAS circuits compared to the MOSFET PG structure, whereas the hybrid PG increases the leakage power by 28.48%. At normal supply voltage, the hybrid PG structure yields high performance, small wake-up time, and less rush current while reducing the area overhead incredibly at the cost of leakage power compared to the conventional PG structure.

Next, in order to show the efficiency of the proposed hybrid PG in the ultralow-voltage region, the PG has been evaluated at 0.4 V. In the same way as the previous experiment, the leakage power, circuit delay, wake-up time, and rush current of the proposed hybrid PG structure are normalized with respect to those of the conventional PG structure with low-V_{th} footers (the high-V_{th} NMOSFET footers should not be used due to the exponentially increased delay and increased wake-up time at the ultralow voltage). Also, the leakage power and circuit delay of the proposed hybrid PG are normalized with respect to those of logic blocks without PG structure. As shown in Table III, the simulation results show that the proposed hybrid PG structure reduces the leakage by 69.07%, the delay by 5.96%, the rush current by 5.13%, and the area by 90% on average for the ISCAS circuits compared to the MOSFET PG structure, whereas the hybrid PG increases the wake-up time by 14.64%.

At the ultralow voltage, the hybrid PG structure yields high performance while reducing the area overhead and keeping low leakage-power dissipation. Although the wake-up time is little increased, the amount can be adjusted easily using the inverter chains of the two-pass PG. In the real design situation, the conventional PG structure with low-V_{th} footers should not be deployed due to increased leakage power although it would reduce circuit delay compared to the conventional PG with high-V_{th} footers. However, the proposed PG structure would be a practicable solution for low-power circuit design with a small

delay penalty (∼3% compared to logic block) in the ultralow-voltage region.

In these experiments, only the sleep mode of four power modes is applied to the PG structure for the worst case scenario and for the comparison between the proposed hybrid two-pass PG and the conventional two-pass PG. Therefore, it is possible to improve all the simulation results if all the multiple modes are applied to the PG structure. The experimental results demonstrate that the proposed hybrid PG structure is very effective and viable in reducing the delay, leakage power, and area overhead of PG structures in the ultralow-voltage region. The results also show that the proposed hybrid two-pass PG using back-gate biasing is compatible with the conventional two-pass PG as shown in Fig. 11(c).

VIII. Conclusion

For cost-effective utilization of CNFETs, a new hybrid MOSFET/CNFET PG structure has been proposed. This new hybrid scheme makes it possible to extend the PG structure's operation range to the ultralow-voltage region. Moreover, in order to minimize wake-up penalties while keeping low leakage power, the proposed PG structure employs the four power-saving modes using the back-gate biasing of the CNFET footers. Finally, a new two-pass PG structure using the back-gate biasing and the turn-on sequence in the CNFET switches is proposed to reduce an excessive wake-up rush current. The simulation results show that the proposed hybrid PG is a viable and low-cost solution for high-energy reduction in the low-voltage nanometer regime.

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