

A CMOS Low-Power Digital Polar Modulator System Integration for WCDMA Transmitter

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Abstract—This paper presents a novel low-power design and highly cost effective chip implementation solution of digital polar modulator for WCDMA transmitters using 0.35 μm mixed mode CMOS technology. The proposed coordinate rotation digital computer (CORDIC) in the polar modulator converts rectangular coordinate to polar coordinate with significantly less hardware and power comparing to the existing computational intensive algorithm by employing hard wired pipeline strategy to increase the performance and to reduce the hardware size. The proposed CORDIC performs a sequence of elementary rotations using shift and add operations without multiplications, providing a highly cost effective solution. The separate distribution of angle constants to each adder permits a hard-wire solution instead of using a lookup table, and all the shifters are hard-wired. Linear interpolators to extend the sampling rate for WCDMA specification are used to decrease the operating frequency. The proposed approach reduces both size and power by integrating booth CORDIC and power amplifier on the same die. The measured average power consumption is 27 mW with 67 MHz clock and 3 V power supply.

Index Terms—CMOS coordinate rotation digital computer (CORDIC), low power, WCDMA.

I. INTRODUCTION

THE future of the computer and communications industries is converging on mobile information appliances such as phones, PDAs, laptops and other devices [1]. Improvements in systems-on-chip technology allow placing of a complete embedded system on a single chip with high performance, low-power, and low-cost features [2]–[6]. The state-of-the-art of the deep sub-micrometer silicon technology has permitted more than billion gates on a chip, and integration of various functions on a single chip increases bandwidth of the system and reduces RC delays and power-consumption and thus increases overall system performance. The advent of third generation standards (3G) has created new demands on multimode systems that can support various modulation formats such as CDMA, TDMA, EDGE, GSM, GPRS, and WCDMA [7].

To achieve multimode operation, transmitters must accommodate constant envelope signals as well as nonconstant envelope signals [8]. To avoid distortion of nonconstant envelopes, conventional transmitters must employ linear amplifier

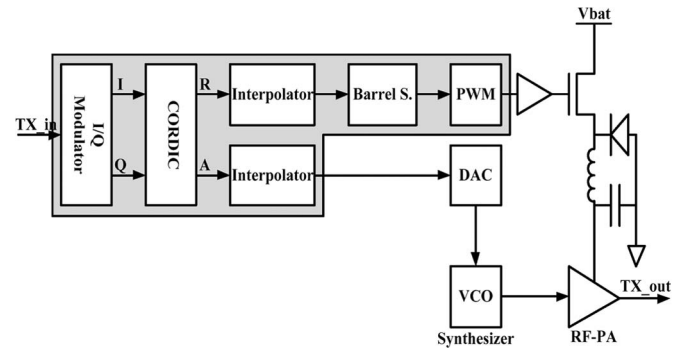


Fig. 1. Polar transmitter architecture for WCDMA.

(class-A) or use predistortion techniques to linearize slightly saturated (class-AB) amplifiers [9]. Both implementations sacrifice power efficiencies and result in decreased battery life. Furthermore, I/Q based transmitter design can be problematic in multiband operation since baseband mixing produces unwanted spurious products [10]. Additional circuitry, such as SAW filters to reject these adverse signals and minimize wideband noise, increases the size, and power consumption of the transmitter [11].

A polar modulation offers an alternative for multimode and multiband operations [12]. The conventional solutions for the implementation of polar transmitter adopted either analog approaches [8] using limiter and envelop detector or digital approaches using DSP engine [13]. The analog approaches suffer from the nonlinearity and distortion of the analog devices and would cause mismatch problem. These approaches often cause the calibration setup cost and the calibration time per device [14]. The existing digital approaches [15], [16] were implemented as a nonlinear filter in a look-up table (LUT). However, the LUT-based nonlinear filter implementations tend to increase the circuit complexity and requires significant amount of digital hardware in general. This paper addresses the hardware size and power efficiency issues of the conventional digital approaches by proposing a highly cost effective architecture and implementation.

Fig. 1 shows a high-level architecture abstraction of the polar transmitter for WCDMA transmitters. The shaded block shows the proposed polar modulator which consists of coordinate rotation digital computer (CORDIC) processor, interpolators, a barrel-shifter, and a DAC-PWM generator. The digitized amplitude envelope through amplitude modulation and the synchronized phase-modulated RF carrier through a phase modulation are recombined at the power amplifier to produce linear and efficient RF transmission [17].

Manuscript received January 4, 2011; revised March 31, 2011; accepted May 15, 2011.

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Digital Object Identifier 10.1109/TIE.2011.2158777

78 Since a rapid carrier is crucial in burst-mode communi-
 79 cation systems [18], a fast rectangular-to-polar conversion of the
 80 CORDIC processor is desired. Furthermore, the delays match-
 81 ing of amplitude and phase are crucial because the restoration
 82 of the transmitted data at the power amplifier (PA) may be
 83 imperfect if the delays are not matched. The CORDIC proposed
 84 in this paper converts rectangular coordinate to polar coordinate
 85 with significantly less hardware and power comparing to the
 86 existing computational intensive algorithm by employing hard
 87 wired pipeline strategy to increase the performance and reduce
 88 the hardware size.

89 This paper presents a highly power and area efficient
 90 WCDMA transmitter module system integration into a single
 91 chip in a sub-micrometer technology ($0.35 \mu\text{m}$) that is used
 92 for designing power amplifiers to combine both CORDIC and
 93 the PA. This allows the module and power amplifiers to be
 94 integrated on the same die, and makes the application more
 95 economical and power efficient. This paper demonstrates the
 96 efficiency of the system integration of the polar modulation
 97 with low cost hardware available for a broad market for con-
 98 sumer products. Section II describes the mathematics behind
 99 the CORDIC algorithm, and the proposed polar modulation
 100 architecture is described in Section III. The simulation and
 101 experimental results of the polar modulator are presented in
 102 Section IV, followed by the conclusion in Section V.

103 II. CORDIC ARCHITECTURE FOR POLAR MODULATION

104 There are two well-known implementations for rectangular
 105 to polar coordinate conversion to obtain the magnitude and
 106 phase of a complex number [19]. One method uses a ROM
 107 lookup table with both real and imaginary components as
 108 inputs. However, this is practical rather for lower accuracy re-
 109 quirements as the ROM size grows exponentially with increas-
 110 ing number of input bits. The other approach is the CORDIC
 111 processor [20] which can realize low-cost systems by reducing
 112 system complexity. The CORDIC arithmetic technique makes
 113 it possible to perform two dimensions rotations using simple
 114 hardware components without multipliers [21].

115 A distinct feature of the CORDIC algorithm is that it uses
 116 a sequence of elementary rotations to realize a variety of com-
 117 plicated and nonlinear elementary functions. Each elementary
 118 rotation requires simple simultaneous shift and add operations.
 119 By unfolding the iterations for elementary rotation, a pipelined
 120 CORDIC array processor can be realized [22], [23], which
 121 achieves greater speeds of computation such that many partial
 122 results can be calculated simultaneously.

123 A. CORDIC Vectoring Mode for Polar Modulation

124 The CORDIC algorithm performs a planar rotation which
 125 means transforming a vector (X_i, Y_i) into a new vector
 126 (X_j, Y_j) as shown in Fig. 2(a) [24].

127 Using matrix form, a planar rotation for a vector of (X_i, Y_i)
 128 is defined as

$$\begin{bmatrix} X_j \\ Y_j \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} X_i \\ Y_i \end{bmatrix}. \quad (1)$$

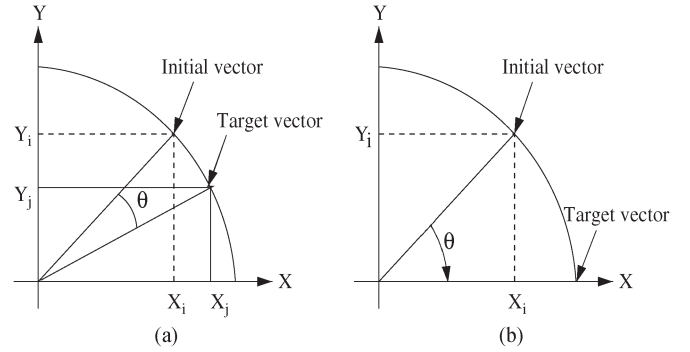


Fig. 2. Vectoring mode for polar modulation.

TABLE I
10-BITS BINARY VALUES FOR $\arctan(2^{-i})$

Step	arctan	Angle (degree)	10-bits binary
1	$\arctan(2^0)$	45.0000	7F = 00 0111 1111
2	$\arctan(2^{-1})$	26.5651	4B = 00 0100 1011
3	$\arctan(2^{-2})$	14.0362	27 = 00 0010 0111
4	$\arctan(2^{-3})$	7.1250	14 = 00 0001 0100
5	$\arctan(2^{-4})$	3.5763	A = 00 0000 1010
6	$\arctan(2^{-5})$	1.7899	5 = 00 0000 0101
7	$\arctan(2^{-6})$	0.8952	2 = 00 0000 0010
8	$\arctan(2^{-7})$	0.4476	1 = 00 0000 0001

The θ angle rotation is executed in several steps. Each step
 is defined as in Table I, and it is modified by eliminating the
 $\cos \theta_n$ factor as following:

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -\tan \theta_n \\ \tan \theta_n & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}. \quad (2)$$

Implementation of (2) requires three multiplications. Two
 multipliers are eliminated by selecting the angle steps such that
 tangent of a step is a power of 2, and dividing by a power of 2
 is implemented using a shift-right operation. The angle for each
 step is given by

$$\theta_n = \arctan \left(\frac{1}{2^n} \right). \quad (3)$$

All summed iteration-angles are equal to the rotation angle θ .
 That is

$$\sum_{n=0}^{\infty} S_n \theta_n = \theta, \quad S_n = \begin{cases} -1 & \text{if } Y_n < 0 \\ +1 & \text{if } Y_n \geq 0. \end{cases} \quad (4)$$

Let us define a variable called Z , which represents the part
 of the angle θ as given in (5).

$$Z_{n+1} = \theta - \sum_{i=0}^n \theta_i. \quad (5)$$

These equations result in

$$\tan \theta_n = S_n 2^{-n}. \quad (6)$$

Combining (2) and (6) gives

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}. \quad (7)$$

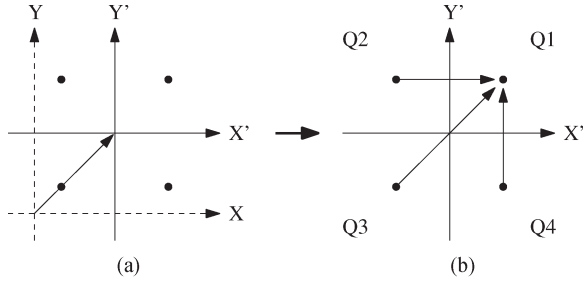


Fig. 3. Preprocessing for polar transmitter.

143 The $\cos \theta_n$ coefficient can be eliminated from the main oper-
144 ations by precomputing the final result (assume that $n = 8$).

$$K = \prod_{n=0}^{\infty} \cos \left(\arctan \left(\frac{1}{2^n} \right) \right) \approx 0.607259. \quad (8)$$

145 If the congruence constant K is set aside since it is precom-
146 puted, the calculation which the CORDIC needs to perform is
147 formulated as

$$\begin{aligned} X_{n+1} &= X_n - S_n 2^{-2n} Y_n \\ Y_{n+1} &= Y_n + S_n 2^{-2n} X_n \\ Z_{n+1} &= Z_n - S_n \arctan(2^{-n}). \end{aligned} \quad (9)$$

148 There is a special case, referred to as the vectoring mode,
149 driving Y to zero. As shown in Fig. 2(b), the CORDIC core
150 computes

$$[X_j, Y_j, Z_j] = \left[\frac{1}{K} \sqrt{X_i^2 + Y_i^2}, \quad 0, \quad \arctan \left(\frac{Y_i}{X_i} \right) \right] \quad (10)$$

151 where the arctan is precalculated as shown in Table I.

152 B. Polar Pre/Postprocessing for WCDMA Transmitters

153 Since I/Q data-streams' polarity is always positive due to the
154 DAC's input, the origin is moved to the center of the data range
155 as shown in Fig. 3(a). Then, a quadrant move is performed to
156 the first quadrant from the other quadrants in Fig. 3(b). In the
157 postprocessing, the CORDIC processor recovers the original
158 quadrant and scales the congruence constant.

159 C. Tradeoff Between Cost and Accuracy

160 There is a tradeoff between implementation costs and nu-
161 merical accuracy [25]. The accuracy of CORDIC processor is
162 dependent on the internal word length used for the three input
163 variables as well as the number of iterations. Since a reduction
164 of the number elementary iterations for a specific algorithm
165 significantly reduces the latency as well as hardware cost, it is
166 desirable to find the optimal number of iterations.

167 The internal bus width limits the maximum number of useful
168 pipelines. Therefore, the peak accuracy is achieved only after
169 "the internal bus width" iterations are determined. Extension
170 bits are added to increase accuracy. However, there are still
171 truncation errors. On the other hand, the accuracy of the rotation
172 angle is determined by how closely the input rotation angle was
173 precalculated. It is inevitable that there is the angle approxima-
174 tion error due to the finite set of angles.

III. POLAR MODULATOR ARCHITECTURE FOR WCDMA TRANSMITTERS

 175
176

Fig. 1 shows high-level architecture abstraction of a polar
177 transmitter for WCDMA transmitters. A signal can be ex-
178 pressed in polar form as a magnitude and a phase. The shaded
179 block shows the proposed polar modulator which consists of
180 quadrature phase shift keying (QPSK) modulator, a CORDIC
181 processor, two interpolators, a barrel-shifter, and a DAC-PWM
182 generator. The QPSK modulator provides I (sine) and Q
183 (cosine) data streams from low frequency serial data. The
184 CORDIC processor transforms the Cartesian coordinates (sine
185 and cosine) from the digital in-phase quadrature (I/Q) mod-
186 ulator into polar coordinates including amplitude and phase.
187 The linear interpolator generates three intermediate values for
188 the amplitude and angle to meet the sampling requirement of
189 WCDMA. The barrel-shifter produces the gain for the ampli-
190 tude. Furthermore, the DAC-PWM generator outputs a serial
191 data for the amplitude. 192

A. QPSK Modulator

193

In communication systems, information is often conveyed by
194 means of bandpass signal, which results from modulating a si-
195 nusoidal carrier. In continuous-time case, any bandpass signal,
196 $s(t)$ with carrier frequency $\omega_c = 2\pi f_c$, can be represented by
197 the unique complex signal $s_c(t)$ 198

$$s(t) = \text{Re} \left\{ |s_c(t)| e^{j\omega_c t} \right\} \quad (11)$$

where $s_c(t)$ is called the complex envelope of the modulated
199 signal. Equation (11) can be rewritten as 200

$$s(t) = |s_c(t)| \cos(\omega_c t + \theta(t)) = I(t) \cos \omega_c t - Q(t) \sin \omega_c t \quad (12)$$

where 201

$$\begin{aligned} s_c(t) &= I(t) - jQ(t) = |s_c(t)| e^{j\theta(t)} \\ |s_c(t)| &= \sqrt{I^2(t) + Q^2(t)} \\ \theta(t) &= \tan^{-1} \left(\frac{I(t)}{Q(t)} \right) \end{aligned}$$

where $I(t)$ is the in-phase component and $Q(t)$ is the
202 quadrature-phase component. 203

The characterization of continuous-time signals given above
204 can be carried over to discrete-time domain signals. Such
205 signals are obtained by sampling a continuous-time signal
206 uniformly at a sufficiently high rate and they are expressed as 207

$$\begin{aligned} s(n) &= \text{Re} \left\{ |s_c(n)| e^{j \frac{2\pi F_c}{F_s} n} \right\} \\ &= \text{Re} \left\{ |s_c(n)| \left(\cos \frac{2\pi F_c}{F_s} n + j \sin \frac{2\pi F_c}{F_s} n \right) \right\} \end{aligned} \quad (13)$$

where 208

$$\begin{aligned} s_c(n) &= I(n) - jQ(n) = |s_c(n)| e^{j\theta(n)} \\ |s_c(n)| &= \sqrt{I^2(n) + Q^2(n)} \\ \theta(n) &= \tan^{-1} \left(\frac{I(n)}{Q(n)} \right). \end{aligned}$$

209

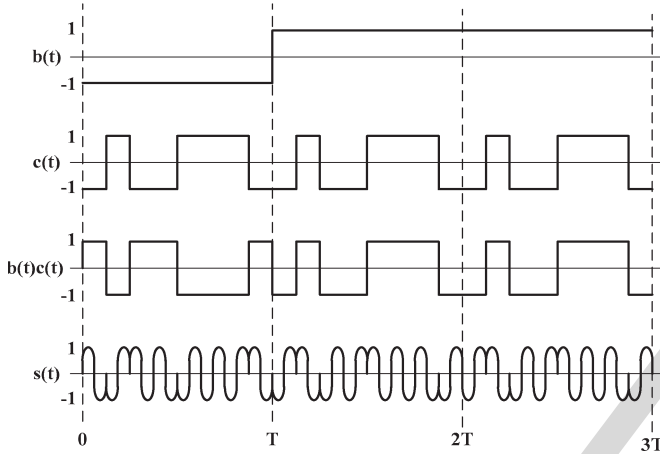
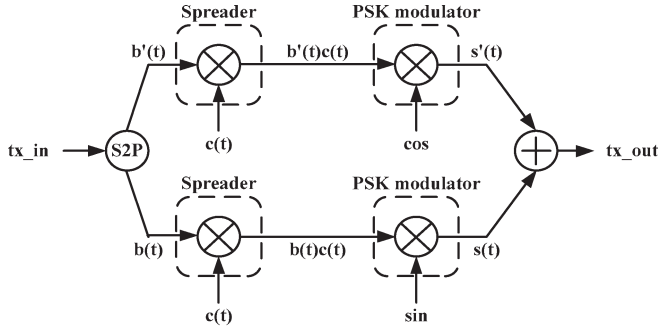


Fig. 4. QPSK modulation and waveforms.

209 The sampling rate F_s in Hz is high enough to satisfy $F_s >$
 210 $2Fc + Bc$, and Fc and Bc are the intermediate carrier fre-
 211 quency in Hz and the bandwidth of Sc in Hz, respectively. The
 212 carrier becomes a phase reference and the signal is interpreted
 213 in reference to the carrier in phase modulation (PM) which
 214 changes only the phase of the signal. The phase is referenced
 215 to the carrier in most communication systems.

216 QPSK among various possibilities for PM is the most
 217 promising candidate due to its high bandwidth efficiency. In
 218 QPSK modulation, pairs of bits are mapped in the signal
 219 constellation $\pi/2$ degrees apart. QPSK modulators provide
 220 constant amplitude, 90° vectors: 0° , 90° , 180° , and 270° . When
 221 the carrier phase varies by 180° , the phase changes cause
 222 additional symbol errors due to carrier amplitude variations.
 223 Furthermore, power amplifiers for QPSK modulation must be
 224 specified for linear operation, namely 1 dB compression and
 225 harmonic suppression.

226 The QPSK modulator consists of a serial-to-parallel con-
 227 verter, a spreader, a PSK modulator, and an adder as shown
 228 in Fig. 4. In the direct sequence spread spectrum technique, a
 229 pseudo-random number (PRN) is applied directly to the data
 230 entering the carrier modulator. The modulator, therefore, sees
 231 much higher bit rate corresponding to the chip rate of the
 232 PRN sequence. Modulating RF carrier with such code sequence
 233 produces a direct-sequence-modulated spread spectrum with
 234 $\{(\sin x)/x\}^2$ frequency spectrum, centered at the carrier fre-
 235 quency. The direct-digital synthesizer (DDS) produces sinu-
 236 soids signal at a given frequency by look-up tables. Multipliers
 237 in the QPSK modulator generate quadrature modulation, and
 238 the outputs from the multipliers are summed (tx_out) and

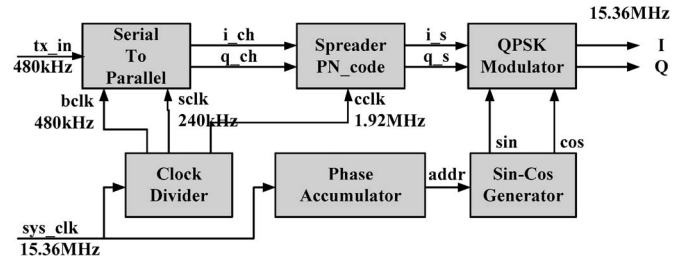


Fig. 5. Block diagram of I/Q modulator.

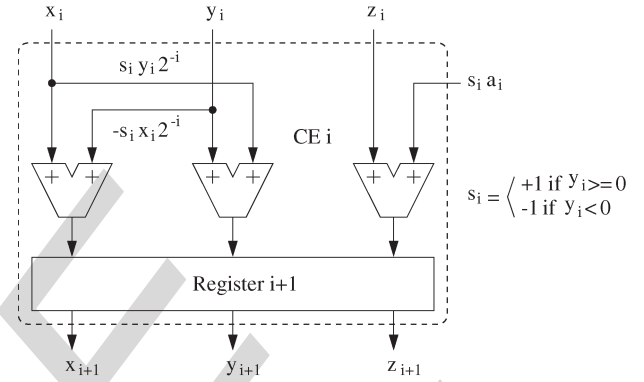


Fig. 6. CORDIC element architecture abstraction.

fed to a DAC. Fig. 4 shows the output values at each stage. 239
 Fig. 5 shows the block diagram of QPSK modulator for a polar 240
 modulator, which needs separate I and Q streams. 241

B. Rectangular to Polar CORDIC Architecture 242

CORDIC element (CE) architecture is shown in Fig. 6, where 243
 the datapath of the CE has 2-bits fixed point extension which 244
 reduces truncation errors. Cyclic convolution provides the ad- 245
 vantages of high computing parallelism and low computation 246
 complexity. A parallel structure shown in Fig. 7 consists of an 247
 array of CEs, each of which performs a computation in parallel 248
 and is separated by registers to form a pipelined structure. 249

The CE is the kernel of the CORDIC processor and its 250
 primary function is to perform (9). The rectangular to polar 251
 CORDIC accepts three input variables X_i , Y_i , and Z_i and 252
 generates the output X_j , Y_j , and Z_j . It is operated in the 253
 vectoring mode, where variable Y_i is forced to zero. In other 254
 words, the coordinate components after rotation are given and 255
 the algorithm calculates the angle of rotation. From the hard- 256
 ware implementation point of view, this operation is carried 257
 out using only shift and add operations since multiplication of 258
 any quantity by 2^{-i} is a shift of the binary representation of 259
 the quantity by i -bit to the right. As a result, all the evaluation 260
 procedures in CORDIC are computed as a rotation of a vector 261
 in three different coordinates systems with an iterative unified 262
 formulation. For example, the operations are to sum or subtract 263
 a shifted valued of X_i to Y_i to obtain Y_{i+1} , a shifted valued 264
 of Y_i to X_i to obtain X_{i+1} , and a precalculated value a_i to 265
 Z_i . Actually the above procedure identified a pseudo-rotation 266
 rather than a rotation because it ignores the congruence constant 267
 K which needs scaling operation. 268

The main components of each CE are three adders, shifter, 269
 look-up table, and a register. Since the function of the shifter in 270

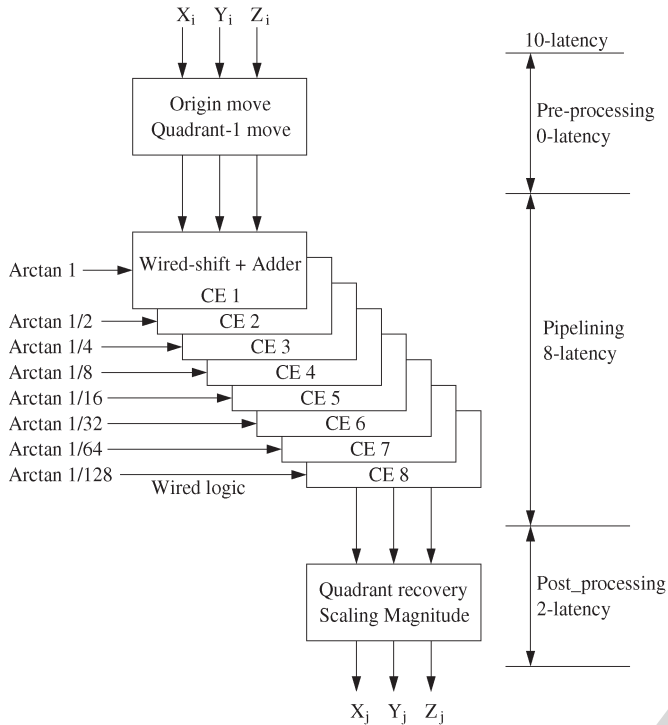


Fig. 7. CORDIC processor architecture abstraction.

271 the pipeline is fixed, the shift operation can be implemented
 272 by wiring. Moreover, the lookup table can be replaced with
 273 hardwired logic because each stage has a congregate constant
 274 instead of a lookup table. Therefore, only three adders and a
 275 register are the main components for a CE. Adopting the wire-
 276 based implementation greatly reduces the hardware cost.

277 Fig. 7 shows the entire design which consists of three mod-
 278 ules; the preprocessing, pseudo-rotation and the scaling factor
 279 blocks that are very fast parallel, and pipeline structures. Since
 280 the RF digital baseband output is unsigned binary and is the
 281 input of the CORDIC processor, the unsigned values are con-
 282 verted to signed binary by moving the origin. The preprocessing
 283 module also performs a movement to quadrant one from the
 284 other quadrants. The function of the postprocessing block is
 285 to scale the magnitude and to recover the original quadrant.
 286 To do this, the postprocessing stage consists of adders and
 287 wired-shifters.

288 C. Postprocessing for WCDMA Requirements

289 For larger word sizes, it is not economical to extend the
 290 sampling rate from 8 to 32 for WCMA input data using the
 291 direct ROM approach. Therefore, an unsigned linear interpo-
 292 lation technique is used where the distance between tabulated
 293 points is uniform. Fig. 6 shows the uniform interpolator which
 294 generates three intermediate values between two inputs. The
 295 counter selects one of the outputs, and the interpolation method
 296 reduces the clock frequency of the CORDIC and the interpo-
 297 lators except for the counter. In turn, it decreases the power
 298 dissipation of those blocks by factor of 4.

299 The output of the barrel-shifter block reflects a gain from
 300 the external inputs. There is an overflow signal which indicates
 301 the output of the DAC-PWM module is out-of-range, and the

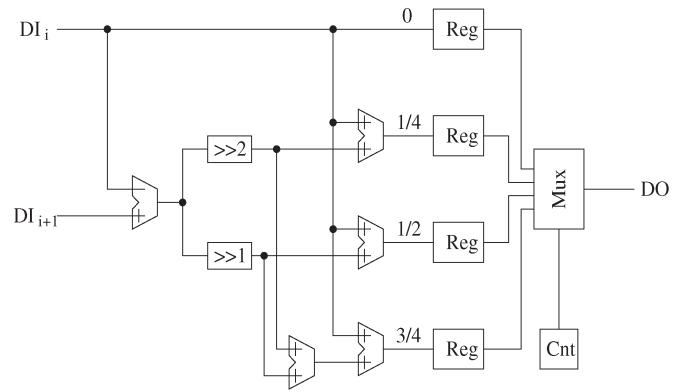


Fig. 8. Unsigned-linear interpolator.

output is fixed as the maximum value. To match the delays of 302
 the amplitude and angle, registers are used at the final stage. 303
 The angle ports have additional MUXes for serial and parallel 304
 outputs. The delay difference is less than 1 ns (Fig. 8). 305

The DAC-PWM module in Fig. 1 converts the parallel data 306
 to serial data. This makes the switch mode regulator simpler 307
 at the expense of data loss (32-sampling) and high power 308
 consumption due to high clock frequency. 309

IV. SIMULATIONS AND EXPERIMENTAL RESULTS 310

To simulate and verify the modulator, the input data is 311
 generated by digital I/Q modulator implemented using Altera 312
 Flex10K FPGA. The 10-bit CORDIC processor and other 313
 postprocessing blocks are modeled in Verilog HDL and are 314
 fully synthesized. The datapath of CORDIC core consists of 315
 0-latency preprocessing, 8-latency pipeline, and 2-latency post- 316
 processing. Cadence Verilog-XL is used for simulation and 317
 functional verification of the CORDIC processor and other 318
 postprocessing blocks. Synthesis is achieved with Synopsys' 319
 Design Compiler. Low-power clock buffers are synthesized for 320
 the clock signals of the individual stages. The automatic P&R 321
 (Place and Route) is generated using Apollo from Synopsys. 322

The design is mapped onto a $0.35 \mu\text{m}$ four metal CMOS 323
 technology. The layout used the standard cell based design flow 324
 of Apollo with 80% core utilization ($0.8 \times 0.95 \text{ mm}^2$, 10 000 325
 gates). The nominal supply voltage for core cells is 3 V. Post- 326
 layout parasitic parameters are extracted and the SPICE netlist 327
 is exported. This SPICE netlist is simulated using Nanosim 328
 from Synopsys with the same Verilog test bench used for the 329
 behavioral model. The correct timing behavior of the processor 330
 is observed. The average power consumption of the core is 331
 about 27 mW with a 67 MHz clock frequency and 3 V supply. 332
 Fig. 9 shows the silicon die photo of the digital polar modulator. 333

Table II lists the errors between the actual results and the 334
 calculations caused by truncation and limited pipeline stage. 335
 X, Y , and X', Y' are the unsigned and the signed 10-bits inputs, 336
 respectively [See Fig. 3(a)]. R is the polar magnitude from 337
 the origin (512, 512), and A is the polar phase angle whose 338
 maximum value 1024 (0 indicates 360°). The error between the 339
 calculation and the results for the modulator including channel 340
 noise is tolerable during demodulating. Fig. 10 shows an exam- 341
 ple of the phase distortion at the receiver due to the accumulated 342
 error. The error from the CORDIC can be reduced by increasing 343

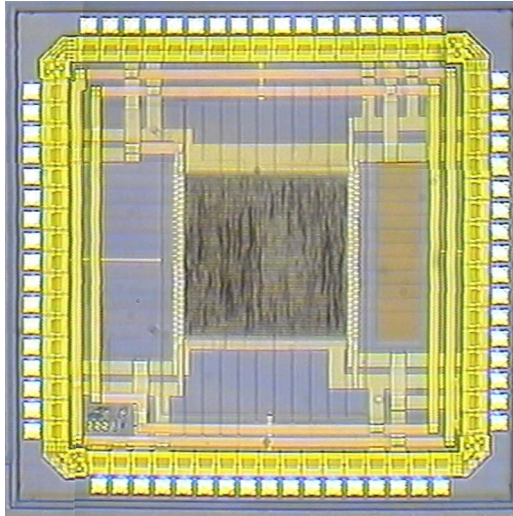


Fig. 9. Digital polar modulator die photo.

TABLE II
POST-LAYOUT SIMULATION RESULTS AND CALCULATIONS
(UNITS: ALL ANGLES ARE MEASURED IN DEGREES)

Input		Output		Calculation	
X (X')	Y (Y')	R(o)	A(o)	R(c)	A(c)
612 (100)	562 (50)	112	75	111.80	85.33
612 (100)	612 (100)	142	127	141.42	128.00
612 (100)	712 (200)	224	181	223.61	170.67
512 (0)	712 (200)	200	255	200.00	256.00
412 (-100)	712 (200)	224	331	223.61	341.33
412 (-100)	612 (100)	142	385	141.42	384.00
412 (-100)	562 (50)	112	437	111.80	426.67
412 (-100)	512 (0)	100	511	100.00	512.00
412 (-100)	462 (-50)	112	587	111.80	597.33
412 (-100)	412 (-100)	142	639	141.42	640.00
412 (-100)	312 (-200)	224	693	223.61	682.67
512 (0)	312 (-200)	200	769	200.00	768.00
612 (100)	312 (-200)	224	843	223.61	853.33
612 (100)	412 (-100)	142	897	141.42	896.00
612 (100)	462 (-50)	112	949	111.80	938.67
612 (100)	512 (0)	100	1	100.00	0.00

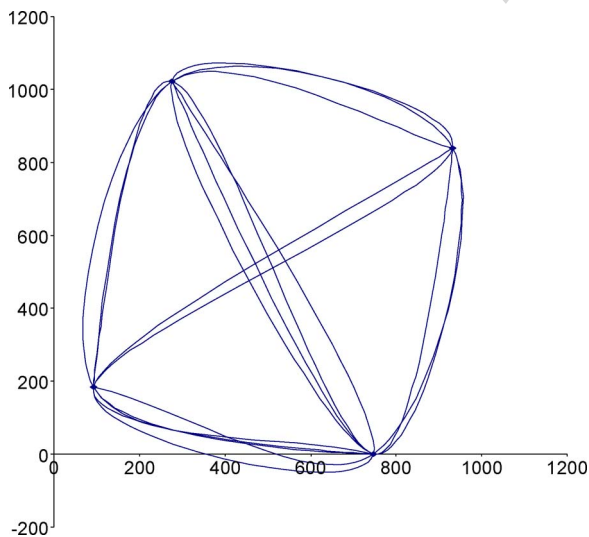


Fig. 10. Example of a QPSK constellation.

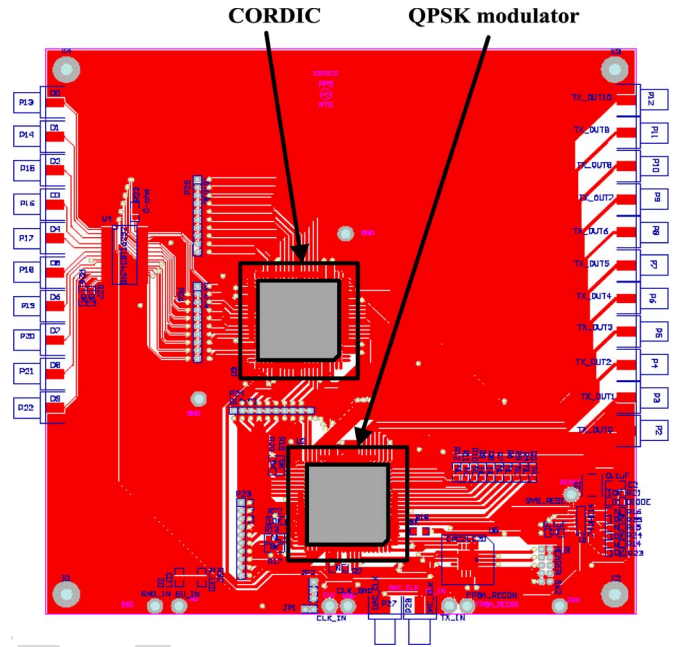


Fig. 11. Demo-board of the polar modulator (before integration).

TABLE III
IMPLEMENTATION SUMMARY OF THE PROPOSED DESIGN

Technology	0.35um CMOS
Voltage	3 V
Core layout area	0.80 x 0.95 mm ²
Chip layout area	0.89 x 1.07 mm ²
System Clock Frequency	67 MHz
Power consumption@67MHz	27 mW

TABLE IV
COMPARISON WITH THE EXISTING DESIGN

Polar Modulator	CMOS Tech.(um)	latency	Power Efficiency (mW/MHz)
Proposed	0.35	10	0.40
[26]	0.18	-	0.22
[27]	0.25	13	0.66
[28]	0.35	2	0.44

the fixed point extension and the CORDIC pipeline stages. 344
Fig. 11 shows the demo-board for polar modulation. 345

The Proposed design and implementation results are sum- 346
marized in Table III, and Table IV shows the comparisons 347
with the existing polar transmitter designs that used the same 348
level of technology (0.35 μm) [28] and the design that used 349
more advanced technologies (0.25 μm and 0.18 μm) [26], 350
[27]. As shown in the table, the proposed design in this paper 351
shows superior power efficiency than others considering the 352
technology scaling. 353

V. CONCLUSION 354

A CORDIC processor is an essential requirement for low 355
cost implementation of the polar modulator. We have proposed 356
and demonstrated novel cost effective digital polar modulator 357
system integration. Due to the proposed CORDIC's regularity 358
and simplicity, the proposed transmitter's architecture makes a 359
highly cost and power effective VLSI implementation possible. 360

361 The CORDIC architecture proposed in this paper adopts a
 362 hard wired pipeline strategy to increase the performance and
 363 reduce the hardware size. The separate distribution of angle
 364 constants to each adder also permits a hardware solution instead
 365 of using a lookup table, and all the shifters are hard-wired.
 366 Moreover, the interpolation method reduces the sampling rate
 367 of the CORDIC, and the interpolators except for the counter,
 368 in turn, decrease the power dissipation of those blocks by
 369 factor of 4. Furthermore, the delays' matching of amplitude
 370 and phase is accomplished within 1 ns. The proposed CORDIC
 371 converts rectangular coordinate to polar coordinate with sig-
 372 nificantly less hardware and power comparing to the existing
 373 computational intensive algorithm. The proposed digital polar
 374 modulator was designed, fabricated using 0.35 μm mixed mode
 375 CMOS process, and tested successfully. The modulator shows
 376 a superior functionality and performance with less power than
 377 the existing ones as demonstrated in this paper, and it is
 378 being used for CDMA applications successfully. The modulator
 379 will be a good reference for low-power communication VLSI
 380 integration, especially systems-on-chip.

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A CMOS Low-Power Digital Polar Modulator System Integration for WCDMA Transmitter

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Abstract—This paper presents a novel low-power design and highly cost effective chip implementation solution of digital polar modulator for WCDMA transmitters using 0.35 μm mixed mode CMOS technology. The proposed coordinate rotation digital computer (CORDIC) in the polar modulator converts rectangular coordinate to polar coordinate with significantly less hardware and power comparing to the existing computational intensive algorithm by employing hard wired pipeline strategy to increase the performance and to reduce the hardware size. The proposed CORDIC performs a sequence of elementary rotations using shift and add operations without multiplications, providing a highly cost effective solution. The separate distribution of angle constants to each adder permits a hard-wire solution instead of using a lookup table, and all the shifters are hard-wired. Linear interpolators to extend the sampling rate for WCDMA specification are used to decrease the operating frequency. The proposed approach reduces both size and power by integrating booth CORDIC and power amplifier on the same die. The measured average power consumption is 27 mW with 67 MHz clock and 3 V power supply.

Index Terms—CMOS coordinate rotation digital computer (CORDIC), low power, WCDMA.

I. INTRODUCTION

THE future of the computer and communications industries is converging on mobile information appliances such as phones, PDAs, laptops and other devices [1]. Improvements in systems-on-chip technology allow placing of a complete embedded system on a single chip with high performance, low-power, and low-cost features [2]–[6]. The state-of-the-art of the deep sub-micrometer silicon technology has permitted more than billion gates on a chip, and integration of various functions on a single chip increases bandwidth of the system and reduces RC delays and power-consumption and thus increases overall system performance. The advent of third generation standards (3G) has created new demands on multimode systems that can support various modulation formats such as CDMA, TDMA, EDGE, GSM, GPRS, and WCDMA [7].

To achieve multimode operation, transmitters must accommodate constant envelope signals as well as nonconstant envelope signals [8]. To avoid distortion of nonconstant envelopes, conventional transmitters must employ linear amplifier

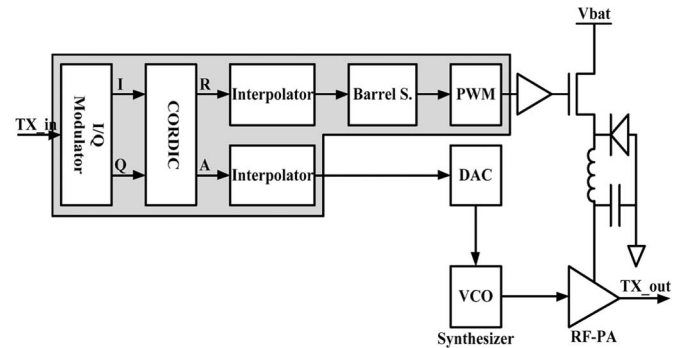


Fig. 1. Polar transmitter architecture for WCDMA.

(class-A) or use predistortion techniques to linearize slightly saturated (class-AB) amplifiers [9]. Both implementations sacrifice power efficiencies and result in decreased battery life. Furthermore, I/Q based transmitter design can be problematic in multiband operation since baseband mixing produces unwanted spurious products [10]. Additional circuitry, such as SAW filters to reject these adverse signals and minimize wideband noise, increases the size, and power consumption of the transmitter [11].

A polar modulation offers an alternative for multimode and multiband operations [12]. The conventional solutions for the implementation of polar transmitter adopted either analog approaches [8] using limiter and envelop detector or digital approaches using DSP engine [13]. The analog approaches suffer from the nonlinearity and distortion of the analog devices and would cause mismatch problem. These approaches often cause the calibration setup cost and the calibration time per device [14]. The existing digital approaches [15], [16] were implemented as a nonlinear filter in a look-up table (LUT). However, the LUT-based nonlinear filter implementations tend to increase the circuit complexity and requires significant amount of digital hardware in general. This paper addresses the hardware size and power efficiency issues of the conventional digital approaches by proposing a highly cost effective architecture and implementation.

Fig. 1 shows a high-level architecture abstraction of the polar transmitter for WCDMA transmitters. The shaded block shows the proposed polar modulator which consists of coordinate rotation digital computer (CORDIC) processor, interpolators, a barrel-shifter, and a DAC-PWM generator. The digitized amplitude envelope through amplitude modulation and the synchronized phase-modulated RF carrier through a phase modulation are recombined at the power amplifier to produce linear and efficient RF transmission [17].

Manuscript received January 4, 2011; revised March 31, 2011; accepted May 15, 2011.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIE.2011.2158777

78 Since a rapid carrier is crucial in burst-mode communi-
 79 cation systems [18], a fast rectangular-to-polar conversion of the
 80 CORDIC processor is desired. Furthermore, the delays match-
 81 ing of amplitude and phase are crucial because the restoration
 82 of the transmitted data at the power amplifier (PA) may be
 83 imperfect if the delays are not matched. The CORDIC proposed
 84 in this paper converts rectangular coordinate to polar coordinate
 85 with significantly less hardware and power comparing to the
 86 existing computational intensive algorithm by employing hard
 87 wired pipeline strategy to increase the performance and reduce
 88 the hardware size.

89 This paper presents a highly power and area efficient
 90 WCDMA transmitter module system integration into a single
 91 chip in a sub-micrometer technology ($0.35 \mu\text{m}$) that is used
 92 for designing power amplifiers to combine both CORDIC and
 93 the PA. This allows the module and power amplifiers to be
 94 integrated on the same die, and makes the application more
 95 economical and power efficient. This paper demonstrates the
 96 efficiency of the system integration of the polar modulation
 97 with low cost hardware available for a broad market for con-
 98 sumer products. Section II describes the mathematics behind
 99 the CORDIC algorithm, and the proposed polar modulation
 100 architecture is described in Section III. The simulation and
 101 experimental results of the polar modulator are presented in
 102 Section IV, followed by the conclusion in Section V.

103 II. CORDIC ARCHITECTURE FOR POLAR MODULATION

104 There are two well-known implementations for rectangular
 105 to polar coordinate conversion to obtain the magnitude and
 106 phase of a complex number [19]. One method uses a ROM
 107 lookup table with both real and imaginary components as
 108 inputs. However, this is practical rather for lower accuracy re-
 109 quirements as the ROM size grows exponentially with increas-
 110 ing number of input bits. The other approach is the CORDIC
 111 processor [20] which can realize low-cost systems by reducing
 112 system complexity. The CORDIC arithmetic technique makes
 113 it possible to perform two dimensions rotations using simple
 114 hardware components without multipliers [21].

115 A distinct feature of the CORDIC algorithm is that it uses
 116 a sequence of elementary rotations to realize a variety of com-
 117 plicated and nonlinear elementary functions. Each elementary
 118 rotation requires simple simultaneous shift and add operations.
 119 By unfolding the iterations for elementary rotation, a pipelined
 120 CORDIC array processor can be realized [22], [23], which
 121 achieves greater speeds of computation such that many partial
 122 results can be calculated simultaneously.

123 A. CORDIC Vectoring Mode for Polar Modulation

124 The CORDIC algorithm performs a planar rotation which
 125 means transforming a vector (X_i, Y_i) into a new vector
 126 (X_j, Y_j) as shown in Fig. 2(a) [24].

127 Using matrix form, a planar rotation for a vector of (X_i, Y_i)
 128 is defined as

$$\begin{bmatrix} X_j \\ Y_j \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} X_i \\ Y_i \end{bmatrix}. \quad (1)$$

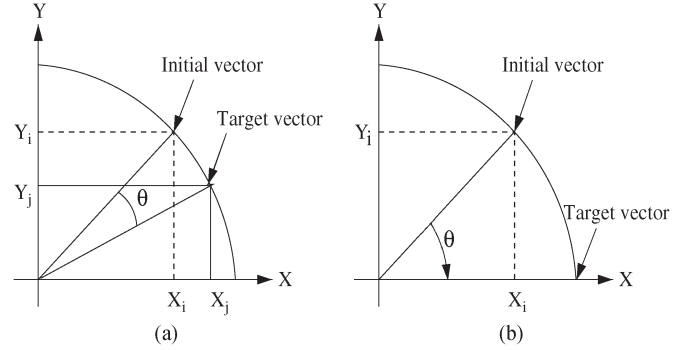


Fig. 2. Vectoring mode for polar modulation.

TABLE I
10-BITS BINARY VALUES FOR $\arctan(2^{-i})$

Step	arctan	Angle (degree)	10-bits binary
1	$\arctan(2^0)$	45.0000	7F = 00 0111 1111
2	$\arctan(2^{-1})$	26.5651	4B = 00 0100 1011
3	$\arctan(2^{-2})$	14.0362	27 = 00 0010 0111
4	$\arctan(2^{-3})$	7.1250	14 = 00 0001 0100
5	$\arctan(2^{-4})$	3.5763	A = 00 0000 1010
6	$\arctan(2^{-5})$	1.7899	5 = 00 0000 0101
7	$\arctan(2^{-6})$	0.8952	2 = 00 0000 0010
8	$\arctan(2^{-7})$	0.4476	1 = 00 0000 0001

The θ angle rotation is executed in several steps. Each step
 is defined as in Table I, and it is modified by eliminating the
 $\cos \theta_n$ factor as following:

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -\tan \theta_n \\ \tan \theta_n & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}. \quad (2)$$

Implementation of (2) requires three multiplications. Two
 multipliers are eliminated by selecting the angle steps such that
 tangent of a step is a power of 2, and dividing by a power of 2
 is implemented using a shift-right operation. The angle for each
 step is given by

$$\theta_n = \arctan \left(\frac{1}{2^n} \right). \quad (3)$$

All summed iteration-angles are equal to the rotation angle θ .
 That is

$$\sum_{n=0}^{\infty} S_n \theta_n = \theta, \quad S_n = \begin{cases} -1 & \text{if } Y_n < 0 \\ +1 & \text{if } Y_n \geq 0. \end{cases} \quad (4)$$

Let us define a variable called Z , which represents the part
 of the angle θ as given in (5).

$$Z_{n+1} = \theta - \sum_{i=0}^n \theta_i. \quad (5)$$

These equations result in

$$\tan \theta_n = S_n 2^{-n}. \quad (6)$$

Combining (2) and (6) gives

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix}. \quad (7)$$

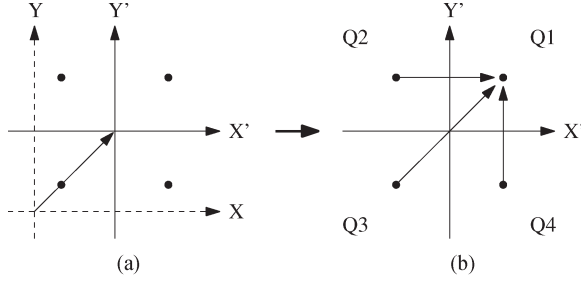


Fig. 3. Preprocessing for polar transmitter.

143 The $\cos \theta_n$ coefficient can be eliminated from the main oper-
144 ations by precomputing the final result (assume that $n = 8$).

$$K = \prod_{n=0}^{\infty} \cos \left(\arctan \left(\frac{1}{2^n} \right) \right) \approx 0.607259. \quad (8)$$

145 If the congruence constant K is set aside since it is precom-
146 puted, the calculation which the CORDIC needs to perform is
147 formulated as

$$\begin{aligned} X_{n+1} &= X_n - S_n 2^{-2n} Y_n \\ Y_{n+1} &= Y_n + S_n 2^{-2n} X_n \\ Z_{n+1} &= Z_n - S_n \arctan(2^{-n}). \end{aligned} \quad (9)$$

148 There is a special case, referred to as the vectoring mode,
149 driving Y to zero. As shown in Fig. 2(b), the CORDIC core
150 computes

$$[X_j, Y_j, Z_j] = \left[\frac{1}{K} \sqrt{X_i^2 + Y_i^2}, 0, \arctan \left(\frac{Y_i}{X_i} \right) \right] \quad (10)$$

151 where the arctan is precalculated as shown in Table I.

152 B. Polar Pre/Postprocessing for WCDMA Transmitters

153 Since I/Q data-streams' polarity is always positive due to the
154 DAC's input, the origin is moved to the center of the data range
155 as shown in Fig. 3(a). Then, a quadrant move is performed to
156 the first quadrant from the other quadrants in Fig. 3(b). In the
157 postprocessing, the CORDIC processor recovers the original
158 quadrant and scales the congruence constant.

159 C. Tradeoff Between Cost and Accuracy

160 There is a tradeoff between implementation costs and nu-
161 merical accuracy [25]. The accuracy of CORDIC processor is
162 dependent on the internal word length used for the three input
163 variables as well as the number of iterations. Since a reduction
164 of the number elementary iterations for a specific algorithm
165 significantly reduces the latency as well as hardware cost, it is
166 desirable to find the optimal number of iterations.

167 The internal bus width limits the maximum number of useful
168 pipelines. Therefore, the peak accuracy is achieved only after
169 "the internal bus width" iterations are determined. Extension
170 bits are added to increase accuracy. However, there are still
171 truncation errors. On the other hand, the accuracy of the rotation
172 angle is determined by how closely the input rotation angle was
173 precalculated. It is inevitable that there is the angle approxima-
174 tion error due to the finite set of angles.

III. POLAR MODULATOR ARCHITECTURE FOR WCDMA TRANSMITTERS

175
176

Fig. 1 shows high-level architecture abstraction of a polar
177 transmitter for WCDMA transmitters. A signal can be ex-
178 pressed in polar form as a magnitude and a phase. The shaded
179 block shows the proposed polar modulator which consists of
180 quadrature phase shift keying (QPSK) modulator, a CORDIC
181 processor, two interpolators, a barrel-shifter, and a DAC-PWM
182 generator. The QPSK modulator provides I (sine) and Q
183 (cosine) data streams from low frequency serial data. The
184 CORDIC processor transforms the Cartesian coordinates (sine
185 and cosine) from the digital in-phase quadrature (I/Q) mod-
186 ulator into polar coordinates including amplitude and phase.
187 The linear interpolator generates three intermediate values for
188 the amplitude and angle to meet the sampling requirement of
189 WCDMA. The barrel-shifter produces the gain for the ampli-
190 tude. Furthermore, the DAC-PWM generator outputs a serial
191 data for the amplitude. 192

A. QPSK Modulator

193

In communication systems, information is often conveyed by
194 means of bandpass signal, which results from modulating a si-
195 nusoidal carrier. In continuous-time case, any bandpass signal,
196 $s(t)$ with carrier frequency $\omega_c = 2\pi f_c$, can be represented by
197 the unique complex signal $s_c(t)$ 198

$$s(t) = \text{Re} \left\{ |s_c(t)| e^{j\omega_c t} \right\} \quad (11)$$

where $s_c(t)$ is called the complex envelope of the modulated
199 signal. Equation (11) can be rewritten as 200

$$s(t) = |s_c(t)| \cos(\omega_c t + \theta(t)) = I(t) \cos \omega_c t - Q(t) \sin \omega_c t \quad (12)$$

where 201

$$\begin{aligned} s_c(t) &= I(t) - jQ(t) = |s_c(t)| e^{j\theta(t)} \\ |s_c(t)| &= \sqrt{I^2(t) + Q^2(t)} \\ \theta(t) &= \tan^{-1} \left(\frac{I(t)}{Q(t)} \right) \end{aligned}$$

where $I(t)$ is the in-phase component and $Q(t)$ is the
202 quadrature-phase component. 203

The characterization of continuous-time signals given above
204 can be carried over to discrete-time domain signals. Such
205 signals are obtained by sampling a continuous-time signal
206 uniformly at a sufficiently high rate and they are expressed as 207

$$\begin{aligned} s(n) &= \text{Re} \left\{ |s_c(n)| e^{j \frac{2\pi F_c}{F_s} n} \right\} \\ &= \text{Re} \left\{ |s_c(n)| \left(\cos \frac{2\pi F_c}{F_s} n + j \sin \frac{2\pi F_c}{F_s} n \right) \right\} \end{aligned} \quad (13)$$

where 208

$$\begin{aligned} s_c(n) &= I(n) - jQ(n) = |s_c(n)| e^{j\theta(n)} \\ |s_c(n)| &= \sqrt{I^2(n) + Q^2(n)} \\ \theta(n) &= \tan^{-1} \left(\frac{I(n)}{Q(n)} \right). \end{aligned}$$

209

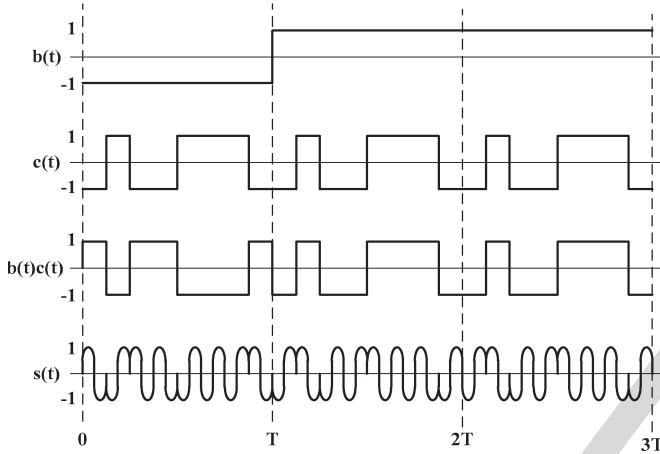
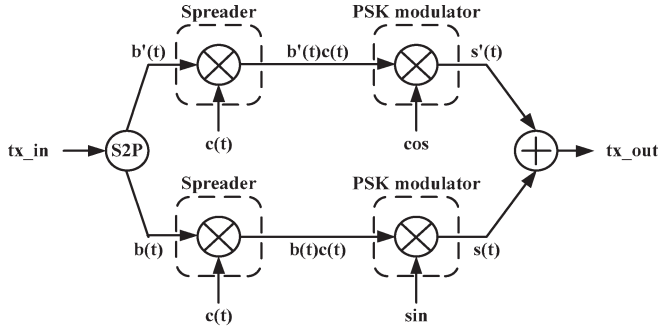


Fig. 4. QPSK modulation and waveforms.

209 The sampling rate F_s in Hz is high enough to satisfy $F_s >$
 210 $2Fc + Bc$, and Fc and Bc are the intermediate carrier fre-
 211 quency in Hz and the bandwidth of Sc in Hz, respectively. The
 212 carrier becomes a phase reference and the signal is interpreted
 213 in reference to the carrier in phase modulation (PM) which
 214 changes only the phase of the signal. The phase is referenced
 215 to the carrier in most communication systems.

216 QPSK among various possibilities for PM is the most
 217 promising candidate due to its high bandwidth efficiency. In
 218 QPSK modulation, pairs of bits are mapped in the signal
 219 constellation $\pi/2$ degrees apart. QPSK modulators provide
 220 constant amplitude, 90° vectors: 0° , 90° , 180° , and 270° . When
 221 the carrier phase varies by 180° , the phase changes cause
 222 additional symbol errors due to carrier amplitude variations.
 223 Furthermore, power amplifiers for QPSK modulation must be
 224 specified for linear operation, namely 1 dB compression and
 225 harmonic suppression.

226 The QPSK modulator consists of a serial-to-parallel con-
 227 verter, a spreader, a PSK modulator, and an adder as shown
 228 in Fig. 4. In the direct sequence spread spectrum technique, a
 229 pseudo-random number (PRN) is applied directly to the data
 230 entering the carrier modulator. The modulator, therefore, sees
 231 much higher bit rate corresponding to the chip rate of the
 232 PRN sequence. Modulating RF carrier with such code sequence
 233 produces a direct-sequence-modulated spread spectrum with
 234 $\{(\sin x)/x\}^2$ frequency spectrum, centered at the carrier fre-
 235 quency. The direct-digital synthesizer (DDS) produces sinu-
 236 soids signal at a given frequency by look-up tables. Multipliers
 237 in the QPSK modulator generate quadrature modulation, and
 238 the outputs from the multipliers are summed (tx_out) and

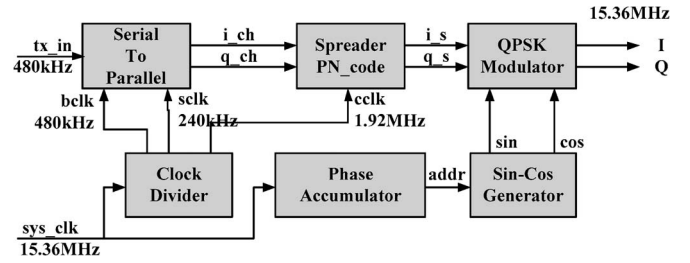


Fig. 5. Block diagram of I/Q modulator.

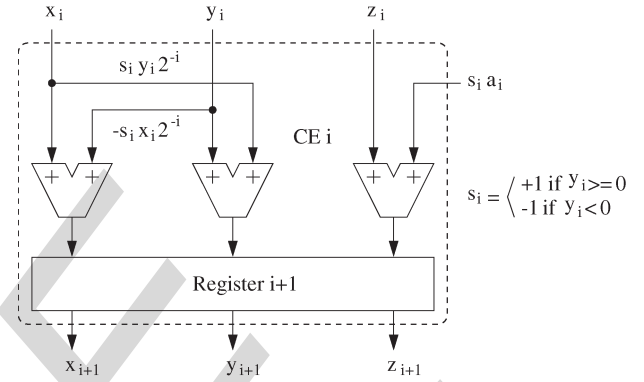


Fig. 6. CORDIC element architecture abstraction.

fed to a DAC. Fig. 4 shows the output values at each stage. 239
 Fig. 5 shows the block diagram of QPSK modulator for a polar 240
 modulator, which needs separate I and Q streams. 241

B. Rectangular to Polar CORDIC Architecture 242

CORDIC element (CE) architecture is shown in Fig. 6, where 243
 the datapath of the CE has 2-bits fixed point extension which 244
 reduces truncation errors. Cyclic convolution provides the ad- 245
 vantages of high computing parallelism and low computation 246
 complexity. A parallel structure shown in Fig. 7 consists of an 247
 array of CEs, each of which performs a computation in parallel 248
 and is separated by registers to form a pipelined structure. 249

The CE is the kernel of the CORDIC processor and its 250
 primary function is to perform (9). The rectangular to polar 251
 CORDIC accepts three input variables X_i , Y_i , and Z_i and 252
 generates the output X_j , Y_j , and Z_j . It is operated in the 253
 vectoring mode, where variable Y_i is forced to zero. In other 254
 words, the coordinate components after rotation are given and 255
 the algorithm calculates the angle of rotation. From the hard- 256
 ware implementation point of view, this operation is carried 257
 out using only shift and add operations since multiplication of 258
 any quantity by 2^{-i} is a shift of the binary representation of 259
 the quantity by i -bit to the right. As a result, all the evaluation 260
 procedures in CORDIC are computed as a rotation of a vector 261
 in three different coordinates systems with an iterative unified 262
 formulation. For example, the operations are to sum or subtract 263
 a shifted valued of X_i to Y_i to obtain Y_{i+1} , a shifted valued 264
 of Y_i to X_i to obtain X_{i+1} , and a precalculated value a_i to 265
 Z_i . Actually the above procedure identified a pseudo-rotation 266
 rather than a rotation because it ignores the congruence constant 267
 K which needs scaling operation. 268

The main components of each CE are three adders, shifter, 269
 look-up table, and a register. Since the function of the shifter in 270

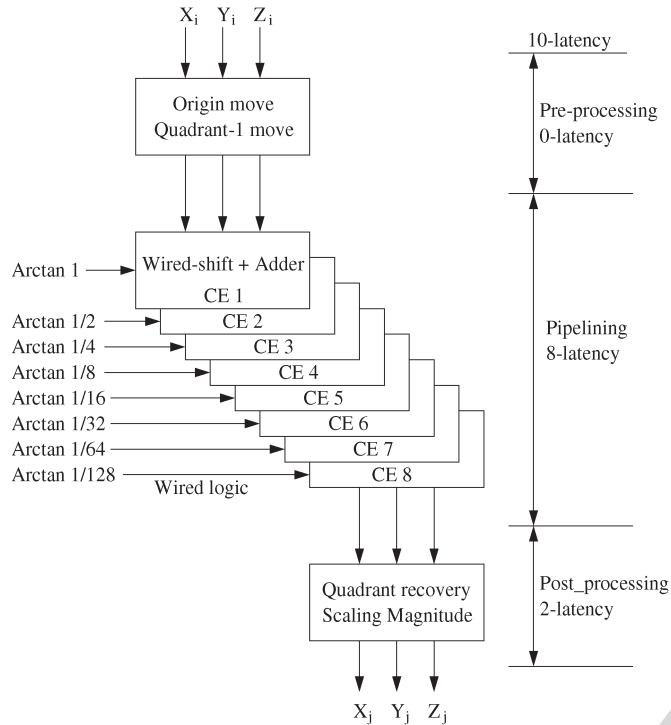


Fig. 7. CORDIC processor architecture abstraction.

271 the pipeline is fixed, the shift operation can be implemented
 272 by wiring. Moreover, the lookup table can be replaced with
 273 hardwired logic because each stage has a congregate constant
 274 instead of a lookup table. Therefore, only three adders and a
 275 register are the main components for a CE. Adopting the wire-
 276 based implementation greatly reduces the hardware cost.

277 Fig. 7 shows the entire design which consists of three mod-
 278 ules; the preprocessing, pseudo-rotation and the scaling factor
 279 blocks that are very fast parallel, and pipeline structures. Since
 280 the RF digital baseband output is unsigned binary and is the
 281 input of the CORDIC processor, the unsigned values are con-
 282 verted to signed binary by moving the origin. The preprocessing
 283 module also performs a movement to quadrant one from the
 284 other quadrants. The function of the postprocessing block is
 285 to scale the magnitude and to recover the original quadrant.
 286 To do this, the postprocessing stage consists of adders and
 287 wired-shifters.

288 C. Postprocessing for WCDMA Requirements

289 For larger word sizes, it is not economical to extend the
 290 sampling rate from 8 to 32 for WCDMA input data using the
 291 direct ROM approach. Therefore, an unsigned linear interpo-
 292 lation technique is used where the distance between tabulated
 293 points is uniform. Fig. 6 shows the uniform interpolator which
 294 generates three intermediate values between two inputs. The
 295 counter selects one of the outputs, and the interpolation method
 296 reduces the clock frequency of the CORDIC and the interpo-
 297 lators except for the counter. In turn, it decreases the power
 298 dissipation of those blocks by factor of 4.

299 The output of the barrel-shifter block reflects a gain from
 300 the external inputs. There is an overflow signal which indicates
 301 the output of the DAC-PWM module is out-of-range, and the

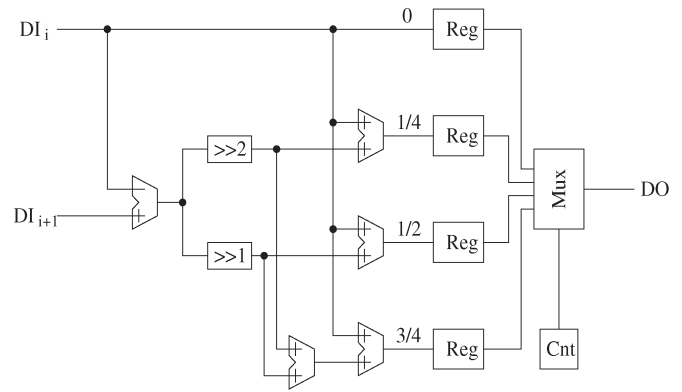


Fig. 8. Unsigned-linear interpolator.

output is fixed as the maximum value. To match the delays of 302
 the amplitude and angle, registers are used at the final stage. 303
 The angle ports have additional MUXes for serial and parallel 304
 outputs. The delay difference is less than 1 ns (Fig. 8). 305

The DAC-PWM module in Fig. 1 converts the parallel data 306
 to serial data. This makes the switch mode regulator simpler 307
 at the expense of data loss (32-sampling) and high power 308
 consumption due to high clock frequency. 309

IV. SIMULATIONS AND EXPERIMENTAL RESULTS 310

To simulate and verify the modulator, the input data is 311
 generated by digital I/Q modulator implemented using Altera 312
 Flex10K FPGA. The 10-bit CORDIC processor and other 313
 postprocessing blocks are modeled in Verilog HDL and are 314
 fully synthesized. The datapath of CORDIC core consists of 315
 0-latency preprocessing, 8-latency pipeline, and 2-latency post- 316
 processing. Cadence Verilog-XL is used for simulation and 317
 functional verification of the CORDIC processor and other 318
 postprocessing blocks. Synthesis is achieved with Synopsys' 319
 Design Compiler. Low-power clock buffers are synthesized for 320
 the clock signals of the individual stages. The automatic P&R 321
 (Place and Route) is generated using Apollo from Synopsys. 322

The design is mapped onto a 0.35 μm four metal CMOS 323
 technology. The layout used the standard cell based design flow 324
 of Apollo with 80% core utilization ($0.8 \times 0.95 \text{ mm}^2$, 10 000 325
 gates). The nominal supply voltage for core cells is 3 V. Post- 326
 layout parasitic parameters are extracted and the SPICE netlist 327
 is exported. This SPICE netlist is simulated using Nanosim 328
 from Synopsys with the same Verilog test bench used for the 329
 behavioral model. The correct timing behavior of the processor 330
 is observed. The average power consumption of the core is 331
 about 27 mW with a 67 MHz clock frequency and 3 V supply. 332
 Fig. 9 shows the silicon die photo of the digital polar modulator. 333

Table II lists the errors between the actual results and the 334
 calculations caused by truncation and limited pipeline stage. 335
 X, Y , and X', Y' are the unsigned and the signed 10-bits inputs, 336
 respectively [See Fig. 3(a)]. R is the polar magnitude from 337
 the origin (512, 512), and A is the polar phase angle whose 338
 maximum value 1024 (0 indicates 360°). The error between the 339
 calculation and the results for the modulator including channel 340
 noise is tolerable during demodulating. Fig. 10 shows an exam- 341
 ple of the phase distortion at the receiver due to the accumulated 342
 error. The error from the CORDIC can be reduced by increasing 343

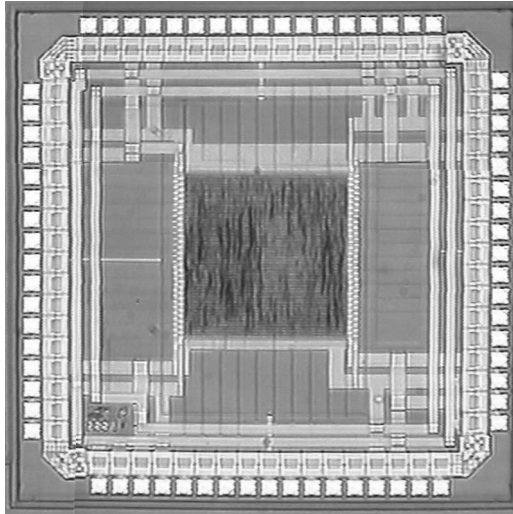


Fig. 9. Digital polar modulator die photo.

TABLE II
POST-LAYOUT SIMULATION RESULTS AND CALCULATIONS
(UNITS: ALL ANGLES ARE MEASURED IN DEGREES)

Input		Output		Calculation	
X (X')	Y (Y')	R(o)	A(o)	R(c)	A(c)
612 (100)	562 (50)	112	75	111.80	85.33
612 (100)	612 (100)	142	127	141.42	128.00
612 (100)	712 (200)	224	181	223.61	170.67
512 (0)	712 (200)	200	255	200.00	256.00
412 (-100)	712 (200)	224	331	223.61	341.33
412 (-100)	612 (100)	142	385	141.42	384.00
412 (-100)	562 (50)	112	437	111.80	426.67
412 (-100)	512 (0)	100	511	100.00	512.00
412 (-100)	462 (-50)	112	587	111.80	597.33
412 (-100)	412 (-100)	142	639	141.42	640.00
412 (-100)	312 (-200)	224	693	223.61	682.67
512 (0)	312 (-200)	200	769	200.00	768.00
612 (100)	312 (-200)	224	843	223.61	853.33
612 (100)	412 (-100)	142	897	141.42	896.00
612 (100)	462 (-50)	112	949	111.80	938.67
612 (100)	512 (0)	100	1	100.00	0.00

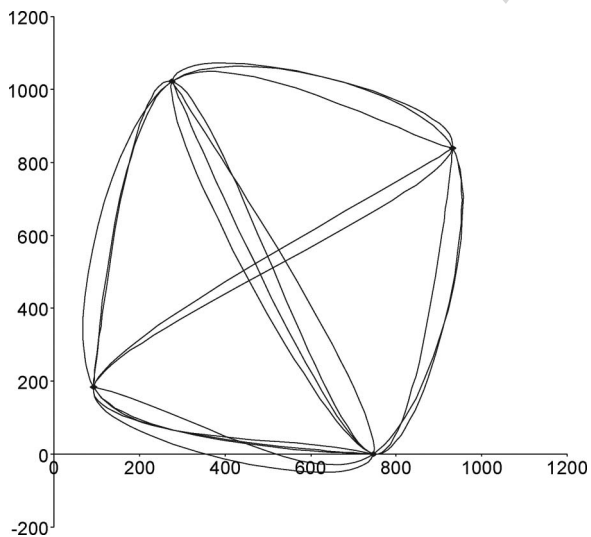


Fig. 10. Example of a QPSK constellation.

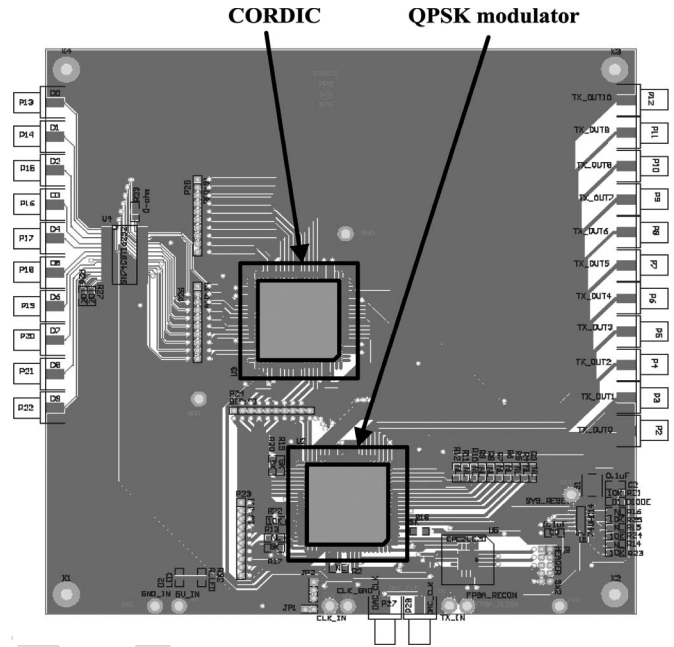


Fig. 11. Demo-board of the polar modulator (before integration).

TABLE III
IMPLEMENTATION SUMMARY OF THE PROPOSED DESIGN

Technology	0.35um CMOS
Voltage	3 V
Core layout area	0.80 x 0.95 mm ²
Chip layout area	0.89 x 1.07 mm ²
System Clock Frequency	67 MHz
Power consumption@67MHz	27 mW

TABLE IV
COMPARISON WITH THE EXISTING DESIGN

Polar Modulator	CMOS Tech.(um)	latency	Power Efficiency (mW/MHz)
Proposed	0.35	10	0.40
[26]	0.18	-	0.22
[27]	0.25	13	0.66
[28]	0.35	2	0.44

the fixed point extension and the CORDIC pipeline stages. 344
Fig. 11 shows the demo-board for polar modulation. 345

The Proposed design and implementation results are sum- 346
marized in Table III, and Table IV shows the comparisons 347
with the existing polar transmitter designs that used the same 348
level of technology (0.35 μm) [28] and the design that used 349
more advanced technologies (0.25 μm and 0.18 μm) [26], 350
[27]. As shown in the table, the proposed design in this paper 351
shows superior power efficiency than others considering the 352
technology scaling. 353

V. CONCLUSION 354

A CORDIC processor is an essential requirement for low 355
cost implementation of the polar modulator. We have proposed 356
and demonstrated novel cost effective digital polar modulator 357
system integration. Due to the proposed CORDIC's regularity 358
and simplicity, the proposed transmitter's architecture makes a 359
highly cost and power effective VLSI implementation possible. 360

361 The CORDIC architecture proposed in this paper adopts a
 362 hard wired pipeline strategy to increase the performance and
 363 reduce the hardware size. The separate distribution of angle
 364 constants to each adder also permits a hardware solution instead
 365 of using a lookup table, and all the shifters are hard-wired.
 366 Moreover, the interpolation method reduces the sampling rate
 367 of the CORDIC, and the interpolators except for the counter,
 368 in turn, decrease the power dissipation of those blocks by
 369 factor of 4. Furthermore, the delays' matching of amplitude
 370 and phase is accomplished within 1 ns. The proposed CORDIC
 371 converts rectangular coordinate to polar coordinate with sig-
 372 nificantly less hardware and power comparing to the existing
 373 computational intensive algorithm. The proposed digital polar
 374 modulator was designed, fabricated using 0.35 μm mixed mode
 375 CMOS process, and tested successfully. The modulator shows
 376 a superior functionality and performance with less power than
 377 the existing ones as demonstrated in this paper, and it is
 378 being used for CDMA applications successfully. The modulator
 379 will be a good reference for low-power communication VLSI
 380 integration, especially systems-on-chip.

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