

# Analysis and Design of Nanoscale CMOS Storage Elements for Single Event Hardening with Multiple Node Upset

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**Abstract**—The occurrence of a single event with a multiple node upset is likely to increase significantly in nanoscale CMOS due to reduced device size and power supply voltage scaling. This current work presents a comprehensive treatment (model, analysis and design) for hardening storage elements (memories and latches) against a soft error resulting in a multiple node upset at 32nm feature size in CMOS. A novel 13T memory cell configuration is proposed, analyzed, and simulated to show a better tolerance to the likely multiple node upset. The proposed hardened memory cell utilizes a Schmitt trigger design. As evidenced in past technical literature and used in this current work, simulation of all node pairs by current sources results in an assessment similar to 3D device tools; the simulation results shows that the proposed 13T improves substantially over DICE in the likely and realistic scenarios of very diffused or limited charge sharing/collection. Moreover, the 13T cell achieves a 33% reduction in write delay and only a 5% (9%) increase in power consumption (layout area) compared to the DICE cell (consisting of 12 transistors). The analysis is also extended to hardened latches; it is shown that the latch with the highest critical charge has also the best tolerance to a multiple node upset. Among the hardened latches, the Schmitt trigger designs have the best tolerance and in particular, the transmission gate configuration is shown to be the most effective. Simulation results are provided using the predictive technology file for 32nm feature size in CMOS. Monte Carlo simulation confirms the excellent multiple node upset tolerance of the proposed hardened storage elements in the presence of process, voltage, and temperature variations in their designs.

**Index Terms**—Memory Design, Nanotechnology, Radiation Hardening, Soft Error.

## I. INTRODUCTION

AS CMOS is moving into nanometric feature sizes, novel circuits have been proposed. The operation of these circuits exploits the high device density while meeting other performance metrics (such as power consumption and delay).

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Scaling of CMOS has been made possible by improved fabrication/manufacturing as well as design techniques; however the reliable operation at nanometric feature sizes is of significant concern. The amount of charge stored on a circuit node is becoming increasingly smaller due to the lower supply voltage and the smaller node capacitance. This makes circuits more susceptible to spurious voltage and charge variations caused by *externally induced phenomena*, such as cosmic ray neutrons and  $\alpha$ -particles [1]. These energy particles travel through the silicon bulk and create minority carriers that may be collected by the source/drain diffusion. They alter voltage values [2] and data integrity could be changed [3] if storage cells, such as memories and latches are affected by the occurrence of this type of event. This event may result in a transient fault (TF); if a TF is latched by a sampling element (latch), then this may result in a so-called soft error (SE) [4]. The soft error rate (SER) is defined as the rate at which a device (circuit or system) encounters SEs on a predictive basis. SER is expected to be significantly higher for CMOS in the deep submicron/nano ranges [5].

Many approaches have been proposed to deal with TFs in storage elements, such as error correcting codes, temporal redundancy, and hardened circuit design. Among them, *hardening* has been utilized for low-cost design to tolerate single SE and TF in memories and latches [6] - [9]. An example of an hardening design approach has been reported in [6] and is commonly known as DICE. The DICE cell is shown in Fig.1

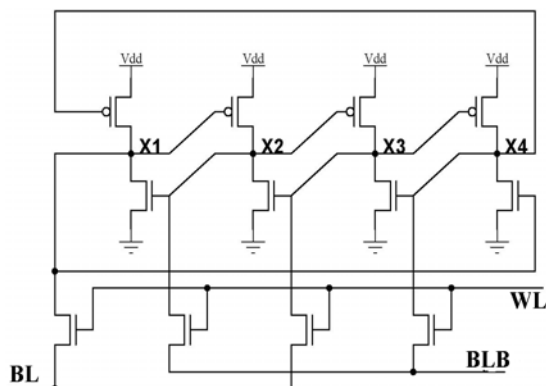


Figure 1. DICE cell proposed in [6]

and uses twice the number of transistors of a standard storage cell (i.e. 12T vs. 6T) to achieve tolerance against a TF affecting any single node. The advantage of this design is that it does not require an increase in the size of the transistors or the capacitance of some nodes. In the DICE cell, the single node that is affected by a TF can be driven back to its previous state by the other transistors. A different hardened memory cell requiring 11 transistors (i.e. 11T) has been proposed in [10]; the single node affected by a TF can be driven back by using novel access and refreshing circuits. Theoretically, these two cells are immune to any amount of charge collected at any single node. However, as device size shrinks, spacing between nodes decreases significantly and the charge generated from a single event strike may diffuse to affect adjacent nodes. As circuits are scaled down in size, the multiple node upset scenario is likely to require new designs for hardening storage cells. Therefore, differently from the reference work [11] in which the multiple-bit upset tolerance is considered, the objective of this study is to investigate the *multiple node upset tolerance* of existing hardening (single-bit) cells (memories and latches) and propose new hardening designs with better multiple node upset tolerance. Charge sharing/collection is considered in the multiple node upset modeling; using [12] – [14] simulation of all node pairs (as attaining similar results to 3D device tools) shows that the proposed design outperforms DICE in the realistic scenarios of (diffused and limited) charge sharing/collection among two adjacent nodes.

This technical paper is organized as follows. Section II deals with modeling soft errors in nanometric circuits. Multiple node upset modeling and tolerance of existing hardened memory designs are analyzed in Section III. This multiple node upset modeling technique is presented in [12] and its correctness has been verified by 3D device simulation tools. A new 13T design of the hardened memory cell is presented in Section IV and it is shown to have a better tolerance to a multiple node upset. Relevant figures of merit such as delay, layout and power are analyzed and assessed in Section V. Section V also presents a simulation-based assessment of variations and their effects on the proposed 13T SRAM cell. Section VI details different Schmitt trigger based designs of a latch for the multiple node upset scenario and evaluates them by HSPICE versus existing (single-node hardened) latch designs. Finally, Section VII concludes this study.

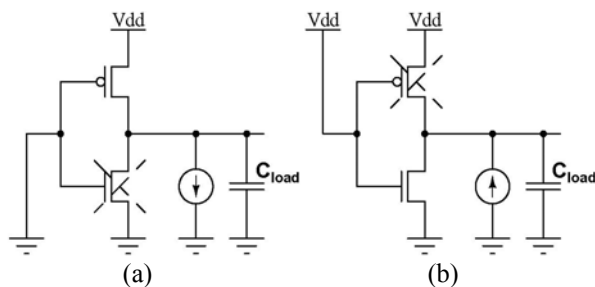


Figure 2. Equivalent circuits used for simulation of (a) negative and (b) positive glitches

## II. SOFT ERROR MODELING

A soft error is said to occur when the collected energy  $Q$  at a particular node is greater than the critical charge,  $Q_{crit}$ , i.e.  $Q_{crit}$  is the minimum charge that needs to be deposited at the sensitive node of a storage cell to flip (change) the stored bit (data). In the model of [15], the SER is given by:

$$SER \propto N_{flux} \times CS \times e^{\frac{-Q_{crit}}{Q_s}} \quad (1)$$

where  $N_{flux}$  is the intensity of the neutron flux,  $CS$  is the area of the cross section of the node, and  $Q_s$  is the charge collection efficiency that strongly depends on doping.  $Q_{crit}$  is proportional to the node capacitance and the supply voltage. In (1),  $Q_{crit}$  exhibits an exponential relationship with the soft error rate; therefore,  $Q_{crit}$  has been widely used as a metric for assessing soft error occurrence. The charge at a single node (due to cosmic ray neutrons or  $\alpha$ -particle hits) generates a large transient current at that node; therefore, a critical charge generated on such node can be modeled as a current pulse for HSPICE simulation.

Fig. 2 shows the soft error model of [16]. This model is also used in this current work for HSPICE simulation. In this figure, with no loss of generality and correctness, soft errors resulting in a signal glitch occur at the inverter. Fig.2 (a) shows the case in which the normal output value for the inverter is high and a soft error occurring at the NMOS transistor generates a negative pulse, whereas Fig.2 (b) shows the case in which the normal output value for the inverter is low and soft error occurring at the PMOS transistor generate a positive pulse.

The soft error on the critical node is modeled as a current source injected to that node. For multiple node injection, multiple current sources are applied to the circuit nodes. A multiple node upset occurs when in the presence of a single event more than one node are affected in the storage element and additional charge is collected by those nodes. It is also important to note that only the scenario of any two-node upset is modeled in this current work. In the occurrence of a single event, a multiple node upset scenario with more than two nodes is unlikely to cause a significant state change due to the extensive charge diffusion occurring in the storage element and wider spread of the incident strike [11]. Therefore, the node that collects the primary portion of the charge is referred to as the *primary node*, while the node that collects the remaining portion of the charge is referred to as the *secondary node*. To simulate the charge collection on two adjacent nodes, the charge is deposited simultaneously on node pairs using multiple current sources [12]; this simulation-based approach has been verified to yield the same correct results as a 3D device modeling approach [12].

## III. EXISTING HARDENED MEMORY DESIGNS

In this section, the single node hardened capabilities of two existing memory cell designs (i.e. DICE and 11T) are evaluated with respect to a multiple node upset scenario. The charges on

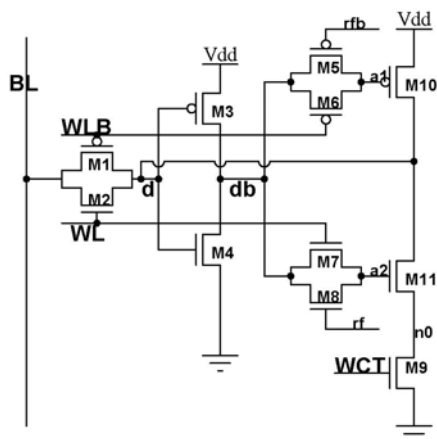


Figure 3. 11T hardened memory cell

the primary and secondary nodes are found to assess by HSPICE simulation the tolerance of these designs to this new scenario.

#### A. DICE Cell

As shown in Fig.1, the DICE cell uses twice the number of transistors of a standard storage cell. The DICE cell has two states, the 0 state ( $X1=0, X2=1, X3=0, X4=1$ ) and the 1 state ( $X1=1, X2=0, X3=1, X4=0$ ). In any of these two states upon the occurrence of a soft error (on a single node), the state of the node is always driven back to its original value. For example, in the 0 state, if the node struck by a particle is  $X2$ , the state of  $X2$  goes from 1 to 0. However, this strike will not propagate along the feedback loop due to the interlocked configuration. Meanwhile, the state 0 stored in  $X1$  can restore the state of  $X2$ ; however, when a single event (strike) occurs on multiple nodes, the DICE cell is unable to drive back the original state. For example, in the 0 state, if the node struck by a particle is  $X2$ , the state of  $X2$  goes from 1 to 0. Meanwhile, if node  $X1$  is also affected by the strike, then it goes from 0 to 1. In this case, due to the strike on  $X1$ , the state of  $X2$  will not be restored and a soft error is said to occur. Simulation results show that if there is a strike on  $X1$ , a very small amount of charge on  $X2$  can change the state of the DICE cell.

#### B. 11T Hardened Cell

A single node hardened memory cell has been proposed in [10] and shown in Fig.3. The basic storage element used in this memory cell relies on the hardening scheme of [8]. In the memory cell of Fig.3, its feedback loop is cut off by the transistors  $M5, M6, M7,$  and  $M8$ , i.e. for a single node upset, a transient pulse cannot be propagated along this loop back to its starting point. The gates of the PMOS and NMOS transistors are separated from the hardened nodes  $a1$  and  $a2$ . Signal regeneration at  $a1$  and  $a2$  is controlled by the transistors  $M5$  and  $M8$ . In this cell, the access pass gates ( $M1$  and  $M2$ ) are connected to node  $d$  instead of nodes  $a1$  and  $a2$  to prevent the high leakage current from  $BL$  to change the data stored in the memory cell. A TF on  $a1$  or  $a2$  will not change the data stored in the memory cell. A NMOS write control transistor is added

to this memory cell for the write operation. As discussed in [17], a single ended SRAM cell operates correctly when writing a “0” as data, but it may encounter problems when writing a “1”. Therefore, a write control transistor is added between  $M11$  and ground to write a “1” [17]. With this write control transistor, the hardened memory cell consists of eleven transistors, i.e. one transistor less than the DICE cell configuration. The 11T memory cell is unable to restore the state of the node when a single event causes a multiple node upset. Similar to the DICE cell, the 11T cell has two states, the 0 state ( $d=0, db=1, a1=1, a2=1$ ) and the 1 state ( $d=1, db=0, a1=0, a2=0$ ). If nodes  $a2$  and  $d$  are affected by a strike, the state of the 11T memory cell will be changed, i.e. it has limited tolerance under a single event with a two node upset.

#### C. Multiple Node Upset Modeling

In the past a multiple node upset has been evaluated using 3D device simulation and a single current source [12]. Recently, it has been shown that two independent current sources in HSPICE can correctly model a multiple node upset using circuit level simulation. To investigate the tolerance to the single event scenario with a multiple node upset outlined previously, two independent current sources are applied to the cell nodes to find the most vulnerable node pairs for a storage element such as a memory cell or a latch. In this current work, this is referred to as the *critical pair*; the critical pair defines two types of information: (a) the nodes that are affected by the soft error and its transient fault; (b) the original and final states of the nodes. In theory for a memory cell with  $N$  nodes, there are at most  $2N(N-1)$  combinations; in practice the number of combinations is much less as dependent on the cell functionality and circuit structure. For example, a conventional 6T cell has two internal nodes that may be affected by a particle strike, hence there are four combinations. For the DICE cell, there are 24 combinations, but only transient faults on adjacent nodes will cause a multiple node upset (due to its feedback feature). So, the number of combinations for the DICE cell is reduced to 16. For the 11T memory cell of in Fig.3, particles striking the NMOS transistor produce only negative current pulses and particles striking a PMOS transistor produce only positive current pulses. So, a particle striking node  $a2$  can turn transistor  $M11$  off, but it can never turn it on, i.e. node  $a2$  can only go from state 1 to 0, but never from 0 to 1. Similarly, a particle striking node  $a1$  can turn transistor  $M10$  off, but it can never turn it on. Therefore, the number of combinations of the 11T cell is 12.

The process for finding the critical pair of a hardened storage element starts from the critical node (as the node with the lowest critical charge). This node is therefore identified as the *primary node*. All node combinations with the primary node are then simulated and the critical node pair is found. However, for the 11T and the DICE memory cells, they are fully immune to a single node upset. In this case, simulation of all possible combinations must be performed to find the critical pair. The exhaustive pair-wise node simulation of these memory cells has been performed and the results show that the critical pair for the

DICE cell is “x1 1->0 (i.e. the state of node x1 changes from 1 to 0), x4 0->1”, and the primary node for this pair is node x1. Similarly, the critical pair for the 11T memory cell is “a2 1->0, d 0->1”. Simulation results show that the 11T memory is more vulnerable to a multiple node upset compared with DICE. To improve its tolerance to a multiple node upset, two transistors are added to the 11T memory cell, yielding a 13T memory design, which will be described in more detail in the next section.

#### IV. PROPOSED HARDENED MEMORY CELL

A new hardened memory cell is proposed in this current work to improve the tolerance to a multiple node upset. Its design is shown in Fig. 4. In the 11T memory cell, the critical pair of the cell is “a2 1->0, d 0->1”, i.e. when node a2 stores a state 1 and a charge is collected on the primary node a2, a transient fault causes the node to change from state 1 to state 0. At the same time under this scenario, charge is also collected by the secondary node d; this causes the node to change from state 1 to state 0. Simulation results show that in order to improve the tolerance to a multiple node upset, it is important to improve the critical charge on the secondary node.

It is well known in electronic circuit design that a Schmitt trigger affects the switching threshold of an inverter depending on the direction of the input transition. The Schmitt trigger configuration introduced in [18] is achieved with a feedback mechanism to increase the switching threshold of the input inverter [18]. Since the transition on node d is from 1 to 0, in the proposed design the feedback mechanism is used only in the pull-down path to improve the critical charge on the secondary node, i.e. node d.

As shown in Fig.4, two additional transistors are added to the 11T memory cell, yielding a 13T design. The operation of the 13T memory cell is similar to the 11T memory cell. The refresh signals rf and rfb are connected to the gates of M8 and M5 to regenerate the states at nodes a1 and a2. The complementary periodic refresh signals rf and rfb are used to regenerate the states on nodes a1 and a2. As the read wordline is always connected to the memory cell, then these two signals can be used to control the pass gate transistors to block the feedback

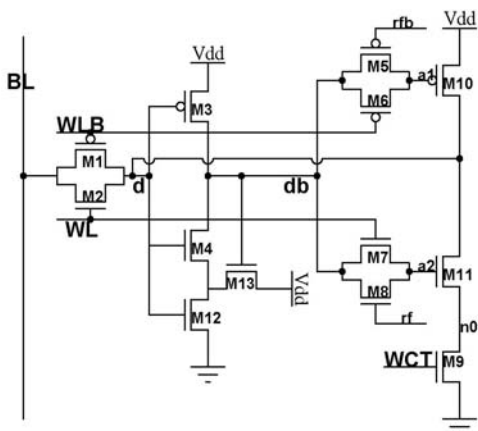


Figure 4. Proposed 13T hardened memory cell

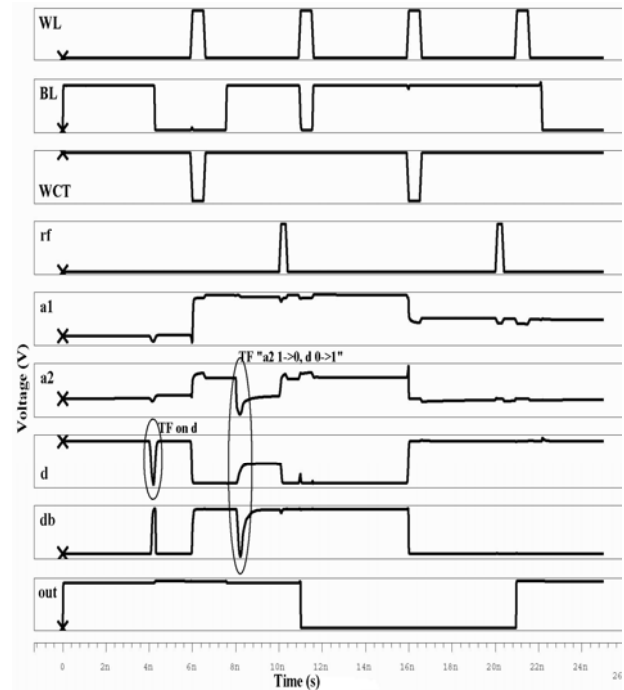


Figure 5. Timing diagram of the proposed 13T memory cell

loop.

Fig.5 shows the timing diagram of the proposed 13T memory cell. When WL is high, the transistors M7 and M6 are on, and the cell acts as a normal memory element. When WL is low, the transistors M7 and M6 are off, and the feedback loop is cut off. The refresh signals, rf and rfb, are generated by the read select signal. When a column is selected for read, the rf and rfb signals are generated by a complementary pulse generator to refresh the data at the nodes a1 and a2 and ensure that the correct signal is read by the bitline BL.

As the access transistors M1 and M2 are used for both (read and write) operations, the refresh transistors M5 and M8 and the refresh signals rf and rfb ensure a correct read operation. As shown in Fig.5, when the memory stores “1” and a TF occurs, node d can be restored, i.e. the TF will not propagate along the feedback loop. When the memory stores “0” as data, a2 is “1”. Consider the scenario in which a TF of large charge occurs on node a2 and a small TF occurs on node d prior to the read operation, thus driving node a2 to a “0” state and node d to a “1” state. The state of node d will be temporarily changed to an intermediate state (i.e. between “0” and “1”) because a2 is unable to hold the state of node d. In this case, the state of node a2 needs to be restored to drive node d to the correct state. Else, during the read operation, M6 and M7 are on. The “0” state on node a2 will change the data on nodes db and a1 to the “0” state, resulting in a data change on d to a state “1” (its correct value is “0”). If there is no refresh prior to the read operation, an error occurs during the read operation if a TF strikes on node a2. Therefore, the refresh signals rf and rfb generated by the read select signal are connected to M8 and M5 to refresh the memory cell before the read operation. The refresh operation is performed by a pulse generator circuit sited at every column to

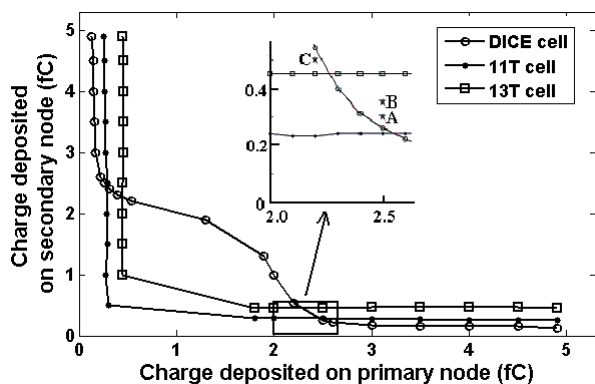


Figure 6. Critical charge plot on the critical pair for DICE cell, 11T hardened cell and 13T hardened cell

provide the refresh signal; once the column is accessed for a read operation, the refresh signal is generated to refresh the memory cells.

Simulation results using HSPICE show that adding the refresh transistors and the refresh circuit to the proposed hardened cell will only increase the average power consumption by 0.8% of an individual memory cell during the read access [10]. The power dissipation of this pulse generator circuit (consisting of a dozen transistors) is very small and therefore negligible compared to the entire memory array [10]. It is important to note that the read column select signal for generating  $r_f$  and  $r_{fb}$  must arrive earlier than the read wordline. This condition is always valid in the proposed design.

## V. EVALUATION

In this section, different figures of merit as related to critical charge, area, power dissipation and delay are assessed to compare the proposed memory cell with other schemes found in the technical literature.

### A. Multiple Node Upset Tolerance

The simulation of a multiple node upset starts with identifying the critical pair of the circuit. After finding the critical pair of each memory cell, the curve of the primary node charge versus the secondary node charge is plotted at 0.9V power supply and room temperature. Compared to the 11T cell, the 13T cell has one more node due to the two additional transistors. As described in Section III.C, the number of combinations for the 13T cell is 20. Simulation shows that the same condition as for the 11T cell is also applicable to the 13T cell, i.e. the critical pair of the 13T cell is still “a2 1->0, d 0->1”. Fig.6 shows the simulation results for the single event scenario with a multiple node upset. This plot is generated by HSPICE simulation to provide a criterion to quantify the tolerance to a multiple node upset, i.e. the area under the curve corresponds to the tolerance. Any combination of charge in the node pair that falls above (below) the curve will (not) result in an upset [12]. Therefore, a large area under the curve means a better tolerance to a multiple node upset. It is also can be observed in Fig. 6 that the curves do not intersect the X and Y axes, thus implying that DICE, 11T, and 13T cells are tolerant to any single node upset

(i.e. when the charge deposited on one node is 0).

As shown in Fig.6, using the Schmitt trigger configuration, the tolerance of a multiple node upset of the 13T cell is improved significantly compared with the 11T memory cell. The area under the curve is significantly increased compared with the 11T cell, making it comparable to the area of the DICE cell. In the 11T and 13T memory cells, the feedback loop is cut off when the cell is holding data, therefore, when the charge on the primary node is large enough to change the state of the primary node, the tolerance to a single event causing a multiple node upset of the memory cell is mostly determined by the critical charge on the secondary node. As shown in Fig.6, the Schmitt trigger configuration is employed in the 13T cell to efficiently increase the critical charge on the secondary node. Fig. 6 shows that the proposed 13T cell has better tolerance to a single event when charge sharing is very diffused or limited in a node pair (i.e. DICE will have better tolerance when charge sharing/collection is nearly uniform), i.e. limited (diffused) charge sharing corresponds to collection of a high (low) charge at primary node and low (high) charge at secondary node. It has been shown [13] that in practical designs and layouts, these are the likely cases of occurrence at nanometric scale sizes.

### B. Area, Power and Delay

The proposed hardened memory has thirteen transistors (13T) compared to the memory cell of [10] with eleven transistors and the DICE cell with twelve transistors. Additional transistors consume more power depending on technology. In the proposed hardened memory cell, the write operation can be slowed down due to the transistors required for blocking the feedback loop. In the 11T and 13T memory cells, the size of the access transistors is therefore, increased to improve performance.

The areas of the 11T hardened memory cell, the 12-transistor hardened DICE memory cell, and the 13T hardened memory cell are compared at 32nm CMOS technology (using the predictive model data of [19] and MOSIS deep sub-micrometer rules [20]). For fair comparison, the total width of the 11 transistors of the proposed cell is the same as the DICE configuration (with 12 transistors). So, the width of the access transistors M1 and M2 in Fig.4 is twice the width of the access

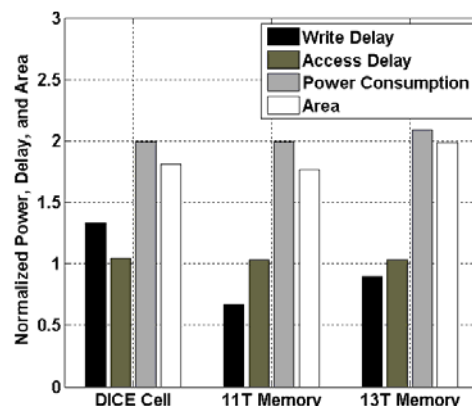


Figure 7. Performance, power, and area comparison of the DICE, 11T and 13T cells

transistors of the DICE cell. Fig.7 shows the write delay, the access delay, the power consumption, and the area of the 11T memory cell, the DICE cell (12T), and the proposed 13T memory cell. The write delay shown in Fig.7 is the average of the write “0” delay and the write “1” delay. The access delay shown in Fig.7 is the average of the read “0” delay and the read “1” delay. All four figures of merit have been normalized to the ones for the conventional (unhardened) 6T memory cell. Due to the large access transistors, the delay performance of the 11T and 13T memory cell is improved, at a higher power consumption, and larger area. In Fig.7, the proposed 13T cell is 33% faster than the DICE cell, with only a 9% larger area and a 5% power penalty.

For nanometric technologies, the shorter distance between nodes likely results in the diffusion of charges from the hit node to adjacent nodes (i.e. larger is the distance, lower is the occurrence of a multiple node upset). Therefore, charge collection at multiple nodes is due to sharing as caused by the cell layout. Layouts of the DICE and the proposed 13T memory cells are shown in Fig. 8. The minimum distances for the critical pair for the DICE (x1 to x4) and the 13T cells (d to a2) are also shown in Fig. 8. The area of the 13T cell is 9% higher than the area of the DICE cell; however, the distance of the critical pair (d, a2) in the 13T cell is 14% longer than the distance of the critical pair (x1, x4) in the DICE cell. As the collected charge is related to node distance [14], then charge will diffuse to adjacent nodes when a particle strikes at a critical location, i.e. collection with high (low) charge at the primary node and low (high) charge at secondary node. Therefore, the layout of the proposed 13T memory cell is also consistent with the scenario that charge sharing/collection will result in a substantial difference between values at the primary and secondary nodes. This confirms the advantages of the proposed design over DICE for charge sharing/collection (as already evidenced in the plot of Figure 6).

### C. Parameter Variations

As CMOS technology scales down into the nano ranges, variations are a serious concern due to uncertainty in device and interconnect characteristics. Variations negatively impact the speed, stability, and power consumption of traditional SRAM designs [21]. In this section, the multiple node upset tolerance of the proposed hardened memory cell is evaluated in the presence of process, voltage, and temperature (PVT) variations.

To model PVT variations by Monte Carlo simulation, parameters including voltage, temperature, and process (threshold voltage and channel length) are swept and simulations are run using a  $\pm 5\%$  Gaussian distribution with variation at the  $\pm 3$ -sigma level. Three node charge pairs, marked as A (2.5fC, 0.3fC), B (2.5fC, 0.35fC), C (2.2fC, 0.5fC) in Fig.6, are selected for simulation. These three pairs are selected because they are close to the crosspoints of the curves (between parenthesis, the first number denotes the charge on the primary node, while the second number denotes the charge on the secondary node). The charge injected to the nodes is also

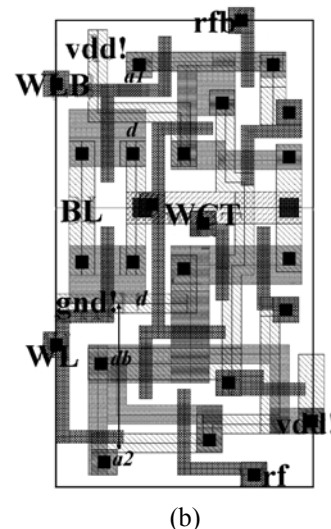
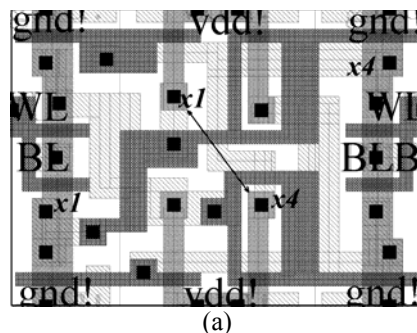


Figure 8. Layout of a) DICE cell; b) Proposed 13T cell

modeled using a  $\pm 5\%$  Gaussian distribution with variation at the  $\pm 3$ -sigma level. It is expected that at the first two charge pair points (A and B), the 13T memory cell will have a better multiple node upset tolerance, while the DICE cell will have a better multiple node upset tolerance for the third charge pair

TABLE I.  
FAILURE PROBABILITY OF MEMORY CELLS WITH PVT VARIATIONS

Memory Cell	# of tolerated trials (A: $Q1=2.5fC, Q2=0.3fC$ )	Failure probability
DICE cell	19040/50000	61.92%
11T cell	39250/50000	88.15%
13T cell	50000/50000	0%
Memory Cell	# of tolerated trials (B: $Q1=2.5fC, Q2=0.35fC$ )	Failure probability
DICE cell	12458/50000	75.08%
11T cell	66/50000	99.87%
13T cell	50000/50000	0%
Memory Cell	# of tolerated trials (C: $Q1=2.2fC, Q2=0.5fC$ )	Failure probability
DICE cell	30099/50000	39.80%
11T cell	0/50000	100%
13T cell	0/50000	100%

point (C). The Monte Carlo simulation results are shown in Table I; samples of 50,000 trials were simulated for each memory cell at the A, B, C charge pairs. The ratio of the number of trials in which the cell does not tolerate the multiple node upset over the total number of trials (i.e. 50,000) is referred to as the *failure probability* and is reported in Table I. The results of Table I confirm very good tolerance of a single event with a multiple node upset for the hardened cells in the presence of PVT variations, i.e. if in Fig. 6 the charge pair is located under the curve, then the presence of PVT variations does not affect its hardening capability to tolerate a multiple node upset.

### VI. HARDENED LATCHES

In this section, the multiple node upset scenario and previous analysis are extended to harden latches as type of storage elements.

#### A. Hardened Latches

A soft error masking latch using a Schmitt trigger circuit

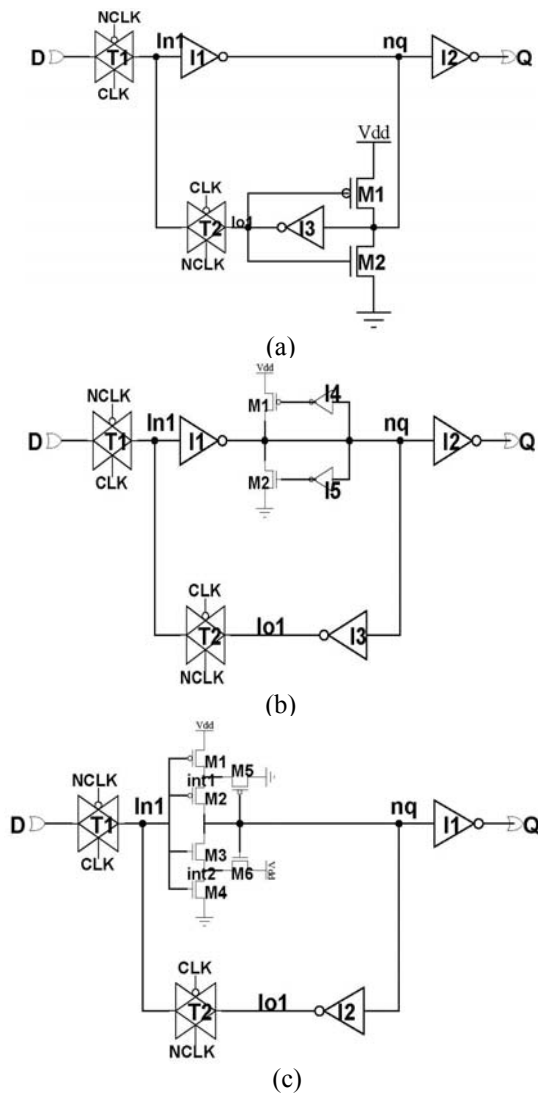


Figure 9. Schematic of a) SEM-latch; b) Modified SEM-latch; c) ST latch

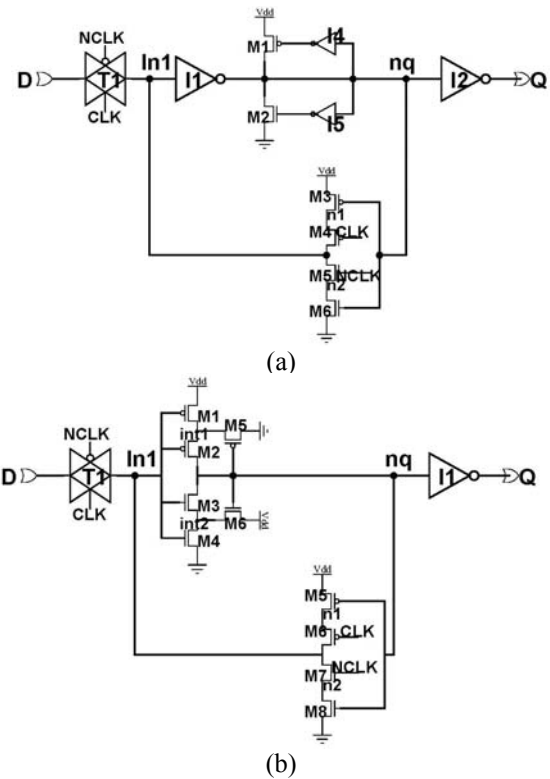


Figure 10. a) Cascode M-SEM latch; b) Cascode ST latch

(SEM-latch) has been proposed in [9]. As reported in [22], the critical charge,  $Q_{crit}$ , is estimated only at specific nodes having the lowest  $Q_{crit}$ . Such node is referred to as the critical node and can be identified by simulation. For the SEM-latch, the critical node is node In1. As shown in Fig.9.a, transistors M1 and M2 are added to the reference latch to make a Schmitt trigger. When CLK is high and NCLK is low, the SEM-latch is transparent. When CLK is low and NCLK is high, transistors M1 and M2 make an inverter in parallel with I1. The equivalent gate capacitance at node In1 is increased, thus also increasing the critical charge at node In1. A Modified SEM latch has been proposed in [3] to achieve a further increase in critical charge, the circuit configuration of the Modified SEM latch (M-SEM latch) is shown in Fig.9.b. Simulation shows that a 13% critical charge improvement is achieved by the Modified SEM-latch because the positive feedback loop from M1 and M2 no longer exists when a transient fault occurs on node In1 and it will not amplify the transient pulse. An alternative hardened Schmitt trigger (ST) based latch has also been proposed in [3] and shown in Fig.9.c. In the ST latch, node In1 is connected to a Schmitt trigger made of six transistors [18]. When node In1 is low, node nq is high, M6 is on, and node int2 is charged. If a strike on a node goes from low to high to change the state of node nq, the charge at node int2 needs to be discharged first. A similar scenario occurs when there is a negative pulse striking node In1. Therefore as proposed in this current work, this Schmitt trigger can provide better tolerance to soft errors due to the charge at nodes int1 and int2. The ST latch achieves 29% critical charge improvement compared to the SEM latch.

TABLE II.  
CRITICAL CHARGE, DELAY, POWER COMPARISON BETWEEN HARDENED LATCHES AT 0.9V POWER SUPPLY AND ROOM TEMPERATURE

Latch	$Q_{crit}$ (fC)	Power Consumption (nW)	Area ( $\mu m^2$ )	Clock to Output delay (ps)
SEM-latch	2.33	206.7	2.284	49.19
Modified SEM-latch	2.63	217.7	2.6112	50.75
Cascade M-SEM latch	2.84	213.8	2.6112	50.45
ST latch	3.00	212.9	2.393	54.40
Cascade ST latch	3.44	209.6	2.393	53.90

Furthermore, as reported in [23], the cascode configuration shown in Fig. 10 provides a better capability to exit the metastable state than the transmission gate configuration due to the reduced Miller effect that will degrade performance when used for a small-signal amplifier. Therefore, the Modified SEM latch and the ST latch can utilize the cascode feedback (Fig. 10); simulation results show an 11% critical charge improvement compared to its transmission gate counterpart. The critical charge, power, delay performance, and area of the hardening latches in Fig.9 and Fig. 10 are shown in Table II. The ST latch and the Cascade ST latch have a higher critical charge than the SEM latch and the Modified SEM latch, while the Modified SEM latch has the largest area due to its highest transistor count. Due to the increase in input node capacitance on the ST latch, the clock to output delay of the ST latch is the highest among all hardened latches.

### B. Multiple Node Upset Tolerance

As device scaling reduces the feature size, the multiple node upset scenario is also becoming a concern for latch design. The

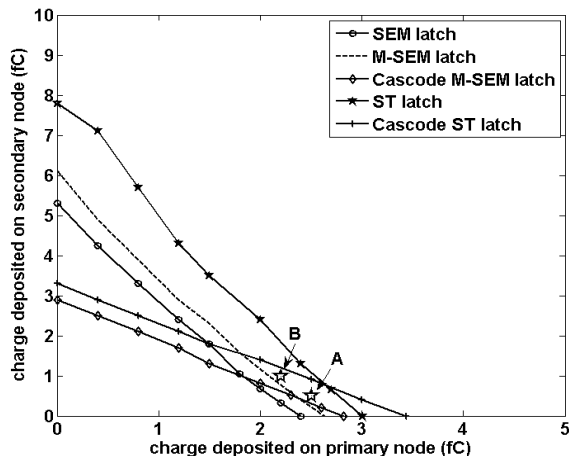


Figure 11. Primary node charge versus secondary node charge of hardened latches

TABLE III.  
FAILURE PROBABILITY OF LATCHES WITH PVT VARIATIONS

Latch	# of tolerated trials (A: $Q1=2.5fC, Q2=0.5fC$ )	Failure probability
SEM latch	501/30000	98.33%
M-SEM latch	8843/30000	70.52%
Cascade M-SEM latch	5456/30000	81.81%
ST latch	28872/30000	3.76%
Cascade ST latch	28612/30000	4.63%
Latch	# of tolerated trials (B: $Q1=2.2fC, Q2=1.0fC$ )	Failure probability
SEM latch	664/30000	97.79%
M-SEM latch	10032/30000	66.56%
Cascade M-SEM latch	957/30000	96.81%
ST latch	29624/30000	1.25%
Cascade ST latch	18556/30000	38.15%

mode and analysis methodology presented previously for memory cells can also be applied to existing hardened latches to evaluate their multiple node upset tolerance. As hardening is achieved by increasing the capacitance of the critical node of the latch, it is expected that higher the critical charge is, the better is the multiple node upset tolerance of the latch. Similar to memory cells, critical pairs are identified first in the proposed hardening process. The primary nodes are the critical nodes of the hardened latches, and HSPICE simulation has been performed on all single node hardened latches in Fig.9 to establish the secondary nodes. Simulation results show that for the hardened latches of Fig.9, the critical pairs are always the same, i.e. “ln11->0, lo1 1->0”. For the Modified SEM-latch and the ST latch in Fig.9, the transmission gate feedback can be replaced by a cascode feedback, yielding a Cascade Modified SEM-latch and a Cascade ST latch. For the Cascade Modified SEM-latch and the Cascade ST latch, the critical pairs are “ln1 1->0, n2 1->0”, where node n2 is the internal node in the cascode feedback (Fig. 10).

Similar to the multiple node upset scenario for memory cells, critical pairs are also established for the various latch designs; the plot of the primary node charge versus the secondary node charge is then found by simulation [12] (Fig.11). As for the memory cells, larger the area under the curve better is the tolerance to a multiple node upset. Fig. 11 shows that the curves intersect the X and Y axes, thus resulting in a single node charge upset (i.e. when the charge deposited on the other node is 0). Table II shows that the cascode configuration has a higher critical charge than the transmission gate configuration for both the M-SEM latch and the ST latch. However as shown in Fig. 11, the transmission gate configuration has a better tolerance to a multiple node upset (i.e. a larger area under the curve). For the cascode configuration of Fig.10.b, the voltage on node n2 is lower than  $V_{dd}$ , while in the transmission gate configuration of Fig.9.c, the voltage on lo1 is  $V_{dd}$ . Moreover, the capacitance

on node n2 of Fig.10.b is smaller than on node lo1 of Fig.9.c (node n2 only has only two transistors and node lo1 has four transistors). So, it is easier for the node n2 to change its current state than node lo1. Hence, the transmission gate configuration is best because it has better multiple node upset tolerance than the cascode configuration.

### C. Parameter Variations

The multiple node upset tolerance of the hardened latches is also evaluated in the presence of PVT variations. To model PVT variations by Monte Carlo simulation, the same conditions for the parameters (voltage, temperature, and process) as for the memory cells are used. Two node charge pairs, marked as A (2.5fC, 0.5fC) and B (2.2fC, 1.0fC) in Fig.11, are selected for simulation because they are located between the curves of the ST latches and the SEM latches. As in the simulation of the memories, the amounts of charge injected to the nodes are modeled with a  $\pm 5\%$  Gaussian distribution with variation at the  $\pm 3$ -sigma level. The simulation results in the presence of PVT variations are shown in Table III; the two selected node charge pairs are located under the curve of the Cascode ST latch and the ST latch, and above the curve of the other hardened latches; therefore, the failure probability of the SEM latch, the Modified SEM latch, and the Modified SEM latch should be significantly higher than the failure probability of the ST latch and the Cascode ST latch. The simulation results reported in Table III confirm the expected results. Hence, at least in theory, the hardened latches with a high critical charge will have a better multiple node upset tolerance. The presented simulation results have confirmed that the Cascode ST latch and the ST latch have a better multiple node upset tolerance than the hardened latches of Fig.9.a, Fig.9.b, and Fig.10.a.

## VII. CONCLUSION

This work has presented a model, analysis and assessment for hardening a memory cell in the presence of a single transient fault/soft error resulting in a multiple node upset. The likely scenario of a multiple node upset has been considered and new designs of storage elements have been proposed based on a novel methodology. This methodology, whose correctness has been verified in [12] (yielding similar results to 3D device simulation), relies on the so-called critical pair; the critical pair allows establishing the plot of the primary node charge versus the secondary charge such that the area under this curve defines the tolerance to a single event with a multiple node upset for a hardened storage element.

A novel 13T memory cell configuration has been proposed, analyzed, and simulated using the predictive technology file and MOSIS for soft error hardening under the multiple node upset scenario. This cell utilizes two additional transistors to a previous design [10] with a Schmitt trigger configuration to increase the critical charge at the secondary node. Tolerance, power consumption, area and delay of this 13T design have been compared with existing hardened designs such as DICE. Using HSPICE, simulation results have confirmed that the proposed memory cell accomplishes the best multiple node

upset tolerance, and impressive performance (delay and power consumption) compared with previous hardened designs. Under a single event with a multiple node upset, simulation has established that the proposed cell outperforms always the 11T cell of [10]. Compared with DICE, the proposed cell has better tolerance provided that charge sharing/collection are very diffused or limited (as encountered in practical designs [13]). The performance of the proposed design is also retained under PVT variations. A similar analysis has also been pursued for hardening latches; additionally, this current work has shown that a cascode configuration has a higher critical charge than a transmission gate configuration in both the M-SEM latch and the ST latch. However, the transmission gate configuration has better multiple node upset tolerance than the cascode configuration due to the larger node capacitance and the higher voltage level at the secondary node.

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