IMPLEMENTATION OF A 1VOLT SUPPLY VOLTAGE CMOS SUBBANDGAP REFERENCE CIRCUIT

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ABSTRACT

This paper presents a CMOS subbandgap reference circuit with 1V power supply voltage. To obtain subbandgap reference voltage with 1Volt supply voltage, threshold voltage reduction and subthreshold operation techniques are aggressively used. Large Δ V_{BE} ($100mV$) as well as 90dB operational amplifier are used to circumvent amplifier offset problem. This circuit is implemented using 0.5 μm CMOS standard process without special process modification and its size is 1370 μm $\times$ 1390 μm. The temperature coefficient of this circuit is 17 ppm from -40 °C to 125 °C after resistor trimming, and the minimum operation power supply voltage is 0.95V. The measured total current consumption is below 10μA and the measured output voltage is 0.631V at room temperature.

1. INTRODUCTION

Bandgap reference voltage circuit is one of the most widely used analog circuits [1] [2]. As process technologies go into deep sub-micron eras and the demand for battery operated-portable equipments is increased, supply voltage has to be scaled down. This low supply voltage requires new circuit technology for designing bandgap reference voltage circuit. The conventional bandgap reference voltage circuit requires at least $1.25V$ or higher supply voltage, since its output voltage is around $1.25V$. The stable operation of bandgap reference circuits is very difficult to obtain under $1.5V$ supply voltage level because of the voltage, temperature, and process variation (PVT variation) as well as design margin.

To keep up pace with supply voltage requirement of modern state-of-art CMOS process, several subbandgap reference voltage circuits have been proposed [2] [3] [4]. However, these circuits did not use the standard CMOS process. Since these approaches require specialized modeling and characterization of devices other than cost issue, standard CMOS subbandgap reference voltage circuit is in high demand. In this paper, a new subbandgap reference circuit, which uses the standard CMOS process without any process modification or special device, is proposed.

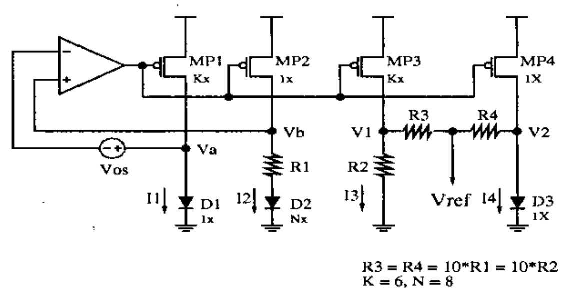

Fig. 1. Proposed bandgap reference voltage circuit

A new bandgap reference core circuit is proposed in Section II, followed by its sub-blocks in Section III. Section IV demonstrates the experimental results from 0.5 μm CMOS implementation. Finally, Section V concludes the paper.

2. PROPOSED SUBBANDGAP REFERENCE VOLTAGE CORE CIRCUIT

Threshold voltage(V_{TH}) has been a major bottleneck to implement a subbandgap reference voltage circuit that operates under $1.2V$ with standard CMOS process. Though advanced IC fabrication process would be used to implement a subbandgap voltage reference circuit, V_{TH} could not be scaled with any other process parameters [5]. Therefore, two methods are considered to circumvent V_{TH}'s limit in this paper.

(1) Threshold voltage reduction - this method uses body effects of transistor. Body effect is caused by voltage difference between source and substrate. Given a PMOS transistor in Nwell process, if the potential of source is higher than that of substrate, V_{THP} can be reduced. To force a proper voltage at the substrate, a bulk bias circuit is used. However, this method cannot be applied to reduce V_{THN}. V_{THN} can be reduced by large channel width transistor in conjuntion with minimal channel length.

(2) Subthreshold operation - The other way to bypass

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V_{TH}'s bottleneck is to use subthreshold operation. If transistors operate at subthreshold region, V_{TH} is no longer significant bottleneck of subbandgap reference voltage circuit design.

Based on the aforementioned techniques, a new subbandgap reference voltage circuit shown in Fig. 1 is proposed. The conventional diode voltage-current relation is given by

$$V_D = V_T \ln \frac{I_D}{I_S} \tag{1}$$

where
V_D: diode voltage
I_D: diode current
I_S: saturation current
V_T: thermal voltage $\left(= \frac{kT}{q}\right)$
In Fig. 1,

$$V_b = V_a - V_{os} \tag{2}$$

Using Eq. (1),(2) and current relations, The output voltage of subbandgap reference voltage is given by

$$V_{ref} = \frac{1}{2} \times \{KV_T \ln(KN) + V_{D_3} - KV_{os}\} \tag{3}$$

The advantages of this circuit are; (1) This circuit uses large ΔV_{BE} to reduce the effect of amplifier input offset problem [6]. In conventional bandgap reference circuit, ΔV_{BE} is around $54mV$(8:1 cathode area ratio). Using a current mirroring, proposed circuit's ΔV_{BE} is $100mV$(48:1). (2) Since this approach takes average voltage outside the feedback loop, it helps stability problem due to loading and error tolerances within the closed feedback loop. (3) The proposed architecuture reduces the total sources of error down to three components matching relationships. The three device mathchings required are diodes, resistors and interdigitated PMOS while the conventional architectures require three or more resistors matchings in addition to the heavy dependency on voltage gain and amplifier offset voltage to generate the V_{BE} and PTAT components. (4) This circuit is true subbandgap reference voltage circuit. The errors are averaged instead of being summed or divided as in the case with alternative circuits. (5) The temperature sensitivity of this circuit is a half of conventional bandgap reference voltage circuit.

3. SUB-BLOCKS FOR PROPOSED BANDGAP REFERENCE VOLTAGE CIRCUIT

3.1. Current Source

A conventional PTAT current source is shown in Fig. 2(a) proposed by Vittoz et al. [3]. V_R is dropped across the resistor in the source of an NMOS on a current mirror loop.

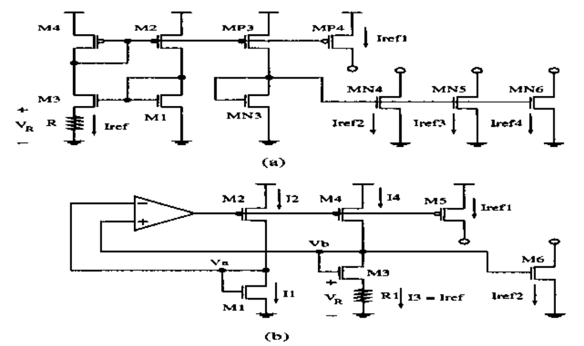

Fig. 2. current source circuit: (a) conventional current source (b) proposed current source

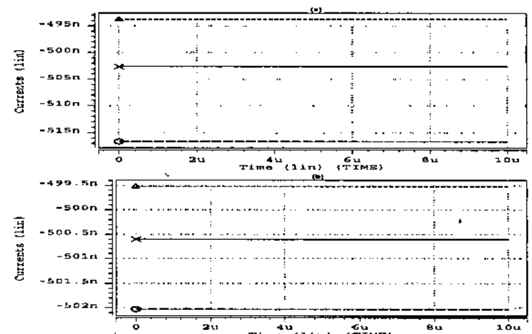

Fig. 3. Monte Carlo Simulation result: (a) conventional current source (b) proposed current source

However, this circuit shows poor performance due to process variation. To overcome this problem, the new current source circuit shown in Fig. 2(b) is proposed.

In a weak inversion region, if $V_D >> V_T$ and $V_S = 0$ are assumed, I_D current is given by

$$I = SI_{D_0} e^{\frac{V_G}{nV_T}} \tag{4}$$

where
I_{D_0}: the characteristic current
S: the ratio of width to length of transistor
n: slope factor of the transistor
$V_{D,G,S}$: drain, gate and source voltage of MOS transistor
Using equation(4) and current relations between transistors, the equillibrium voltage becomes

$$V_R = V_T \ln\left(\frac{S_3}{S_1}\frac{S_2}{S_4}\right) \tag{5}$$

Finally, I_{ref} is given by

$$I_{ref} = \frac{V_R}{R_1} = \frac{V_T}{R_1} \ln\left(\frac{S_3}{S_1}\frac{S_2}{S_4}\right) \tag{6}$$

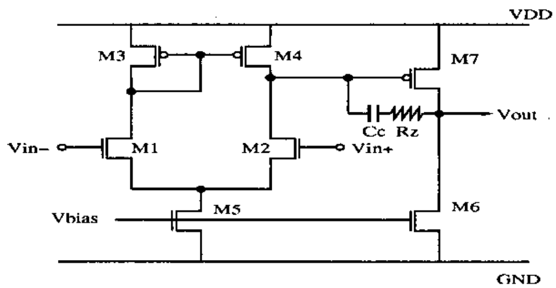

Fig. 4. Operational amplifier for subbandgap core circuit

Since the loop gain of this circuit is sufficiently large due to the operational amplifier, the process related sensitivities are significantly reduced. Fig. 3 shows that Monte Carlo simulation results of two circuits;(a) conventional circuit, (b) proposed circuit. In this simulation, the reference current is $500nA$ and V_{TH} is selected as a variable process parameter. The current variation of the proposed current circuit is from $499.03nA$ to $501.77nA$, and the current variation of the conventional current circuit ranges from $489.81nA$ to $519.34nA$ (more than an order of magnitude improvement).

3.2. Operational amplifier

In order to reduce the effects of offset voltage and PVT variation, it is desirable to increase the DC loop gain as high as possible. To acheive high gain, a conventional 2 stage operational amplifier operated at subthreshold region is used. Though this operational amplifier looks like a conventional 2 stage operational amplifier, current source and operational amplifier operate at subthreshold region. Therefore, it shows a distinct gain characteristics. The gain of 2 stage amplifier in Fig. 4 is given by

$$A_{dc} = g_{m1} \left(r_{o2} \| r_{o4}\right) \times g_{m7} \left(r_{o6} \| r_{o7}\right) \quad (7)$$

where
A_{dc} : the total gain of 2 stage amplifier
g_m : transconductance of each amplifier
r_o : output resistance of transistor Using Eq.(4) and (7), the DC gain becomes

$$A_{dc} = \left(\frac{\ln S}{nR_1}\right) \left(r_{o2} \| r_{o4}\right) \times \left(\frac{\ln S}{nR_1}\right) \left(r_{o6} \| r_{o7}\right) \quad (8)$$

where
S: a current source area ratio $\left(= \frac{S_3 S_2}{S_1 S_4}\right)$. Since the temperature term is canceled, the gain is affected only by the temperature slope of the Early voltage or channel length modulation. These terms are weakly dependent only on temperature. Therefore, the gain is relatively constant and independent of temperature and process variations.

Table 1. Electrical characteristics of Operational Amplifier

Specifications		Unit
Supply Voltage	2.2	V
Supply Current	520	nA
BW	20	KHz
Gain	90	dB
Phase Margin	60	$Degree$
Slew Rate	0.015	$V/\mu S$

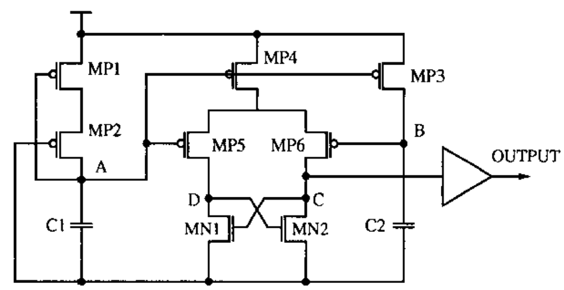

Fig. 5. Proposed Power-On-Reset circuit

3.3. Power-On-Reset circuit

Conventional bandgap reference voltage circuit has two stable operating states, "off" and "the bandgap potential". To avoid stable "off" state, "start-up circuit" is usually used. When the start-up circuit is used for battery-powered system, the main issue is "How to eliminate the stand-by current?" The other issue of start-up circuit is stability. When a second wraparound closed loop is used to implement a start-up circuit, the potential for oscillation or improper operation is greatly increased. Therefore, a open-loop and zero stand-by current start-up circuit is strongly required. To satisfy these requirements, power-on-reset(POR) circuit shown in

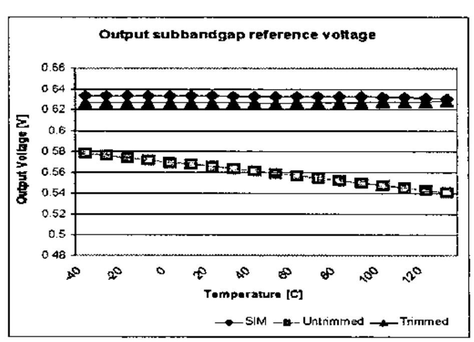

Fig. 6. The measured output voltage Vs. Temperature

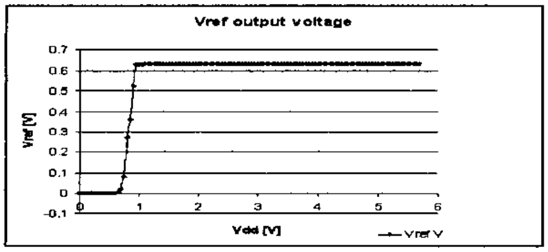

Fig. 7. The measured output voltage Vs. Vdd

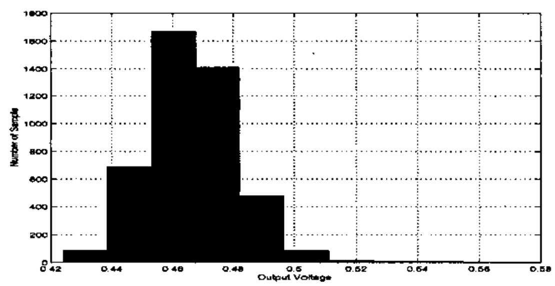

Fig. 8. The histogram of subbandgap reference circuit before trimming

Fig. 5 is designed in this paper. The basic idea of the POR circuit is to use two RC circuits (MP1-MP2-C1, MP3-C2) that have different RC time constant. When the power supply comes up, a comparison between these two time constants determines when the power is high enough to ensure a proper subbandgap operation.

4. EXPERIMENTAL RESULT

The proposed subbandgap reference voltage circuit is implemented using 0.5μm standard CMOS process. The size of subbandgap reference voltage circuit is 1370 μm $\times$ 1390 μm. The measured output voltages with/without trimming and simulated output voltage of subbandgap reference voltage are shown in Fig. 6. The maximum and minimum output voltages after trimming are $0.6268V$ and $0.6283V$, respectively. The maximum current consumption is below 10μA and the temperature coefficient of measured subbandgap reference voltage circuit is 17 ppm from -40 °C to 125 °C. Fig. 7 shows the output voltage variation when the supply voltage changes from 0 to 6V. The minimum operating voltage is 0.95V. Fig. 8 shows the histogram of output voltage of subbandgap reference circuit before trimming. The center of histogram is slightly moved toward the lower voltage due to amplifier offset voltage. The total number of sample is 4437. The micro photograph of subbandgap reference voltage circuit is shown in Fig. 9.

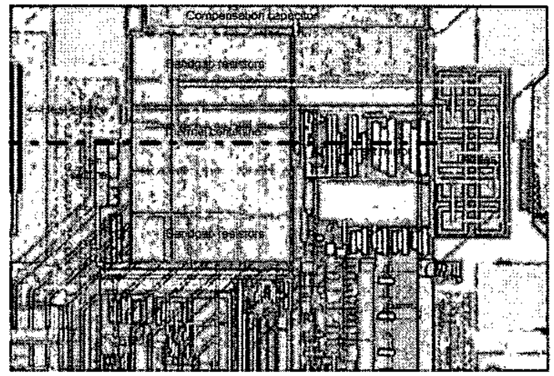

Fig. 9. Photograph of proposed subbandgap reference voltage circuit

5. CONCLUSION

A new subbandgap reference voltage circuit for very low power supply voltage operation in standard CMOS technology is proposed and verified in silicon. V_{ref} is generated by the average of two voltages which are provided by independent outerloop of subbandgap core circuit. In this architecture, one to one resistor matching is used, therefore, improved matching is obtained(traditional resistor matching requirement is 10:1). And this architecture also helps reduce the sensitivity to amplifier gain and offset. The proposed subbandgap reference voltage circuit is applied to power management IC successfully.

6. REFERENCES

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