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Statistical Characterization of Partially-Depleted SOI Gates

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Abstract − *This paper presents a novel statistical characterization methodology for accurate timing analysis for Partially Depleted Silicon-On-Insulator (PD-SOI) digital circuits. The proposed methodology is applied to ISCAS85 benchmarks circuits, and the results show that the error is within 5% comparing to HSpice simulation results.*

Keywords − *SOI (Silicon on Insulator), Statistical Modeling, Statistical Analysis, Cell Characterization, Timing Analysis.*

I. INTRODUCTION

Partially-Depleted Silicon-on-Insulator (PD-SOI) has become one possible technology to improve the performance of VLSI systems because it offers many advantages over the bulk CMOS, such as shorter delay, smaller area, lower parasitic capacitances, lower power, latch-up immunity, and reduced short channel effect[1]. However, the floating body of the PD-SOI leads to uncertainty in its behavior, and the uncertainty complicates timing analysis or simulation of digital circuits. The potential of the floating body with respect to ground is a function of many factors including the circuit topology and switching history. A consequence of this "history effect" is that the delay through a particular circuit or path cannot be predicted without full knowledge of the prior states and transitions of the circuit-information that static timing tools do not posses. The history effect on delays is highly dependent on circuit topology, environment, and other factors.

Therefore, traditional timing analysis tools must be enhanced to include the unique characterization of PD-SOI. Several researches have been published on new timing analysis tools for PD-SOI in logic level and transistor level [2]-[4]. However, they just considered the worst-case delay in PD-SOI digital circuits, or the simplest approach by a state-diagram model ignoring the uncertainty in the characteristic of PD-SOI. This paper presents a new statistical approach for propagation delay of PD-SOI digital circuits.

The remainder of this paper is organized as follows. Section II illustrates the floating body effect of PD-SOI MOSFET. In Section III, statistical timing model and analysis for PD-SOI gates is described. Results from the experimental timing analysis on ISCAS85 benchmark circuits are listed and compared with Monte Carlo methods in Section IV followed by conclusion in Section V.

II. FLOATING BODY EFFECT OF PD-SOI MOSFET

The body potential is determined by capacitive coupling and dynamically changing the threshold voltage which results in higher speed than the bulk MOSFET. It is known as "history effect" or "switching history" in SOI MOSFET [1]. In case of static steady-state conditions, the body potential is changed by source-body diode, drain-body diode, and impact ionization near drain region. Under dynamic switching conditions, the body potential depends on the switching history on the instantaneous node voltage. The history effect causes the variation of threshold voltage of a PD-SOI device, which determines its propagation delay. The delay of PD-SOI can be different depending on the initial condition, switching history, slew rate, pulse width, and frequency of data [2]-[4].

Figure 1 shows the different variation of propagation delay based on previous states of a device. In this figure, the four fundamental states of PD-SOI inverter are introduced, which are Pull_Up_Fast, Pull_Down_Slow, Pull-Down_Fast, and Pull_Up_Slow. They are obtained from two different input waveforms.

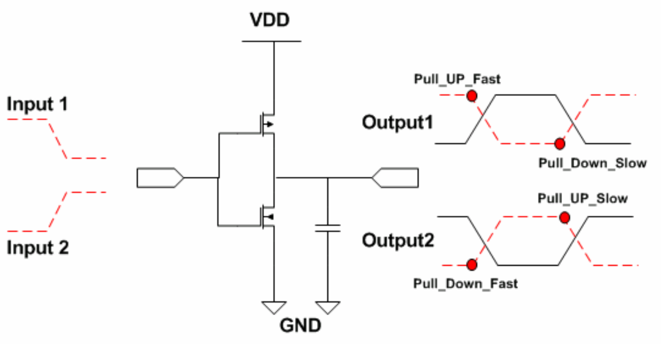


Fig. 1. Four Fundamental Delays.

During Pull_Up_Fast and Pull_down_Fast transition, the propagation is fastest because the body potential of PMOS and NMOS reaches its peak value since its drain-source is the largest.

Similarly, during Pull_Down_Slow and Pull_Up_Slow, the propagation delay is slower than that of the previous switching because the accumulated body potential in NMOS and PMOS is smaller comparing to the previous switching. The conventional propagation delay methodology is to calculate the average time of the output rise and fall delay. However, the methodology is too rough to represent the uncertainty of

PD-SOI gates. In this paper, a new statistical methodology is suggested to represent the uncertainty.

III. STATISTICAL TIMING MODEL AND ANALYSIS FOR PD-SOI GATES

Statistical timing analysis methodology is a common technology for timing analysis of high-speed VLSI circuits considering the process parameter variations. A statistical analysis takes the device parameter varying probability into consideration, and propagates the probability through circuit-path [5]-[9]. In this paper, the concept of the statistical methodology is used for the floating body of PD-SOI. Figure 2 presents the new methodology for accurate timing analysis. At first, random signal is generated using Matlab, which can decide the percentage of logic High and Low in input data. Using the random signal, look-up tables are generated according to the input slew rate, load capacitance, gate size, Probability Density Function (PDF) of output, and switching activity of input. Referred to the look-up tables, the propagation delay is calculated, and the analyzer is implemented in C language.

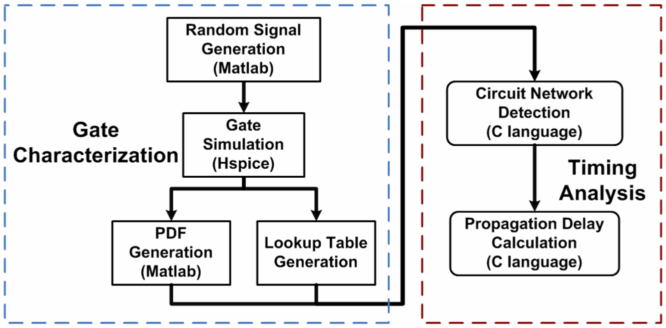


Fig. 2. Statistical Timing Analyzer for PD-SOI.

A. Statistical timing modeling for PD-SOI Gates

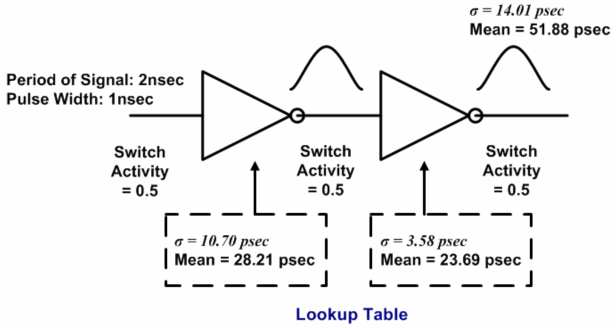
In order to make the lookup tables for statistical timing analysis, the random variables as parameters of timing analysis should be determined. The delay of basic inverter analysis is given by

$$t_d = \left(\frac{1}{2} - \frac{1 - \frac{V_{th}}{V_{DD}}}{2} \right) t_{tr} + C_L \cdot \frac{V_{DD}}{2 I_D} \tag{1}$$

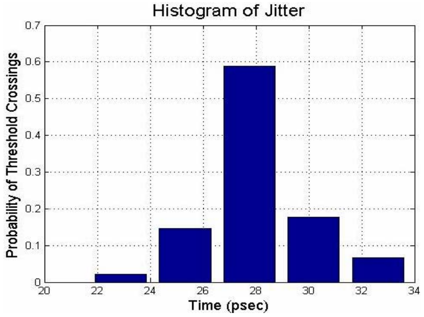
where V_{th} is threshold voltage, t_{tr} is the input waveform transient, and C_L is load capacitance. [10]

Three variables (v_{th}, t_{tr}, and C_L) can control the speed of the inverter. In SOI MOSFET, threshold voltage is a function of switching history, pulse width, and frequency of input waveform. t_{tr} and C_L are functions of input transition time, size of MOSFET, and fanout capacitance. The mean value, variance, and covariance data are generated by Monte Carlo simulation in Hspice, and the PDF is also computed using the values in Matlab. All the data is stored in the lookup table.

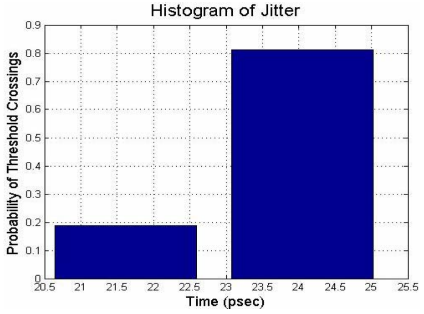
Figure 3 shows an example of the new statistical methodology. Before timing analysis, the look-up tables of inverter A and B are generated, where the standard deviations and mean values of inverter A and B are (10.70 psec, 28.21 psec) and (3.58 psec, 23.69 psec) respectively. Figure 3 (b) and (c) present the PDF of each inverter. The measured PDF of the output is shown in Figure (d), where the standard deviation and mean value are 14.01 psec and 51.88 psec respectively. The result shows the summation of PDFs of each inverter is almost the same as the measured PDF of output.



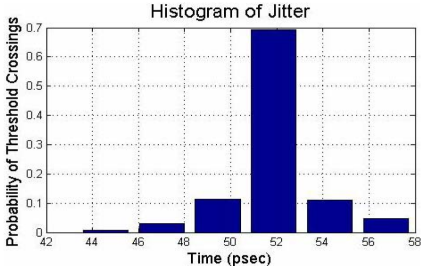
(a) Example Circuit.



(b) PDF of 1st Inverter



(c) PDF of 2nd Inverter



(d) PDF of Output

Fig. 3. Examples of Statistical Timing Analysis.

B. Statistical Timing Analysis

Conventional static timing analysis uses a corner-based methodology for worst-case analysis that is often too pessimistic and grossly conservative. On the other hands, statistical timing analysis using random variables offers a better timing estimation for SOI gates. There are two main streams in the statistical timing analysis methodologies.

The first is path-based algorithms [6][7]. They consider the correlations from both path sharing and global parameters. Therefore, they are accurate and have the ability to realistically capture correlations. However, they have a worst case computation complexity that grows exponentially with respect to circuit size. These algorithms can be considered as depth-first search of the timing graph.

The other is block-based algorithms which can be thought of as breadth-fist search and has linear complexity. Assuming that N is the number of nodes and M is the number of global variations in the timing graph, they can be simply represented using a canonical timing model [8][9]. It is given by

$$X = \mu x + \sum_{i=1}^{N} \alpha_{x,i} R_i + \sum_{j=1}^{M} \beta_{x,j} G_j \tag{2}$$

where R_i is the local and independent variation only related with nodei, G_j is the jth global variation, $\alpha_{x,i}$ and $\beta_{x,j}$ are the corresponding sensitivity factors.

Due to simple approach and linear complexity of the second methodology, the block-based algorithm is used in this paper. The statistical arrival time distribution at the gate output can be calculated by Max, Min, Mean value, variance, and covariance for the resulting random variables from (2).

The Max operation (delay) of gate with two variables is given by

$$Max(x, y) = x + Max(0, y - x) \tag{3}$$

where x and y is random variables.

The mean values of the $Max(x,y)$ is as follows.

$$Mean(Max(0, y - x)) = Mean(x) + Mean(Max(0, y - x)) \tag{4}$$

where

$$\begin{aligned} &Mean(Max(0, y - x)) \\ &= \mu + \sigma \cdot Mean(Max(-\frac{\mu}{\sigma}, \frac{(y - x) - \mu}{\sigma})) \end{aligned} \tag{5}$$

where μ is the mean and σ is the standard deviation.

Finally, the variation can be computed by

$$\begin{aligned} &Var(Max(x, y) \\ &= Var(x) + Cov(x, Max(0, y - x)) + Var(Max(0, y - x)) \end{aligned} \tag{6}$$

The above equations can be easily computed via lookup-table, and the Min operation is almost identical. All the detail calculation is referred to [11].

Once the aforementioned operations are available, they can be used to compute the statistical arrival time at each node from primary inputs to primary outputs using depth-first search. If the searching meets new_level, a new statistical propagation delay is calculated and added to lookup table. And also, the unnecessary variables are removed from lookup table. If the order of searching is unnecessary_level, the output arrival time for the gate is removed. The above algorithm is shown in the following psudo-code.

```
Algorithm 1 Statistical Timing Analysis
Sort gate delay graph
Setup delay variables from lookup table for each gates
For level =1 : primary output level
    For each gate, if current_level=new_level
        Compute and add arrival time into lookup table
        Remove unnecessary variables form lookup table
    End
    For each gate, if current_level=unnecessary_level
        Remove arrival time from lookup table
    End
End
Save mean and variance tables for primary output
```

IV. EXPERIMENTAL RESULTS

The proposed statistical timing analysis for PD-SOI has been implemented in Matlab, Hspice, and C language and ran on Intel Petium-4 PC (2.93GHz) with 1Gbyte memory. The algorithm is proved by the results for various ISCAS85 benchmark circuits. The circuit is designed using Hspice in a 0.15μm BSIMSOI3.2 technology to make the lookup table for random variables. The variables are characterized by Monte Carlo simulation with 50 repetitions in Hspice assuming all variation sources in PD-SOI MOSFET. The primary inputs have the characterization of Gaussian distribution. Table I shows the summary of the average propagation time in each case of Monte Carlo simulation and the proposed method. The first column shows the measured circuits, and the second column is the number of gates of the circuits. The third is the error rate between Monte Carlo simulation and the proposed method. The fourth and sixth column represents the CPU simulation time for each method. Finally, the fifth and seventh column is the estimated propagation delay for each method. The delay is estimated at the confidence level of 97%. The accuracy of the proposed method is within 5% difference comparing to Hspice (Monte Carlo Simulation) results. In addition, the simulation time of the proposed method is much faster than that of Monte Carlo simulation.

The figure 4 shows the PDF for circuit C432 where the PDF of Monte Carlo simulation is interpolated. As shown in the figure, the proposed method has almost the same distribution as the Monte Carlo simulation.

Table I. Experimental Results for ISCAS85 Benchmarks.

Circuit	# of gates	error (%)	Monte Carlo Simulation		Proposed Method	
			CPU time (sec)	Delay (psec)	CPU time (sec)	Delay (psec)
C432	280	3.10	7007.18	17.27	5.03	17.80
C499	373	4.70	9090.32	14.22	5.12	14.90
C880	641	3.78	12830.12	19.87	12.34	19.12
C1355	717	3.77	17070.68	19.39	20.63	20.12

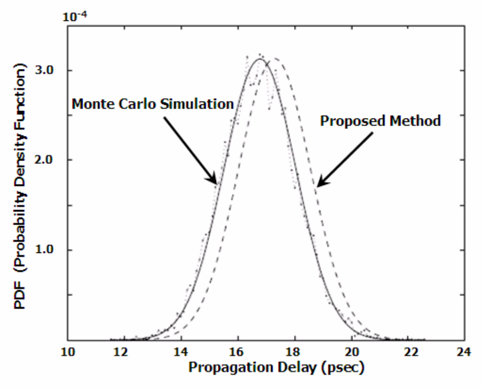


Fig. 4. PDF(Probability Density Function) for C432 circuit

V. CONCLUSION

PD-SOI MOSFET is the state-of-the-art technology for high performance and low power. However, the floating body in the PD-SOI causes the uncertainty of propagation gate delay due to History Effect. The conventional static timing analysis cannot estimate exactly the propagation delay without considering the History effect. This paper presents a new statistical characterization methodology for the accurate timing analysis for PD-SOI CMOS digital circuits. Using the statistical characterization, a new statistical timing analysis is developed and experimented by ISCAS85 benchmark circuits.

The experimental results show that the proposed method has high accuracy and efficiency. In addition, this methodology can be applied to transistor-level timing analysis and noise analysis tools.

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