



SET-based nano-circuit simulation and design method using HSPICE

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Abstract

This paper presents a simulation and design method for complementary SET-based nano-circuits from a practical circuit design point of view. HSPICE behavioral implementation of modified Lientschnig's SET model based on the orthodox theory and the Birth–Death Markov chain is demonstrated and verified with Coulomb characteristics. It shows reduced CPU time, improvement of accuracy, and more compatibility with other SPICE softwares on both Windows and Unix platforms. The proposed design methodology presents how to build static CMOS-like SET circuits, and demonstrates that conventional CMOS circuit design methodologies are all applicable to SET circuit designs based on the methodology. HSPICE simulation results show that, for 1 M Ω junction resistance, the power consumption of a SET NAND2 gate is less than 0.3 pW, and the propagation delay for a SET XOR2 gate is 29.8 ns while driving a 10 aF load.

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1. Introduction

Traditional CMOS technology has dominated for several decades. However, as silicon devices go into sub-100 nm regime, defined by the National Science Foundation as nanotechnology regime, problems such as short channel effects, ultrathin gate leakage, doping fluctuations, and increasingly difficult and expensive lithography will arise. To maintain the trend of Moore's Law and technology's advances in nanoscale regime, novel nanoelectronic solutions [1–7] will be needed to surmount the physical and economic barriers of current technologies. Among them, single-electron tunneling transistor (SET) has been attracting more and more attention because of its ultra small size, extremely low power dissipation, and similar device structure to a MOSFET. While fabrication and modeling techniques [8–13] for SETs are getting matured, developing

SET-based circuit design tools and methodologies for practical circuit designers becomes very urgent and necessary.

SIMON [11] and MOSES [14] are popular SET simulation tools based on the orthodox theory, which was first presented by Dimitri Averin and Konstantin Likharev [15] in 1985, using Monte Carlo method for SET circuit simulations [16] and evaluations of other simulators [12,13]. However, they are not SPICE compatible and do not support CMOS/SET hybrid circuits. MIB [12,17], a quasi-analytical model, is implemented in SMARTSPICE through its Verilog-A interface, but it is not as convenient as using SPICE model. Yu et al. developed SPICE Macromodel [13], however, it is not based on the orthodox theory, and it is hard to design circuits using real device parameters associated with a certain fabrication technology. Recently, Lientschnig has presented a SET model [18] based on the orthodox theory and solving the Master equation. The model was implemented in PSPICE[19] recursively using many PSPICE user and build-in functions of node voltage or current and branch instructions.

Compared with conventional CMOS transistors, SETs have shown flexible gate control due to their double gate

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structure, and the characteristic of periodic current with gate voltage makes a single SET structure appropriate for both PMOS- and NMOS-like devices. This will make CMOS-like SET-based circuit designs possible by using only a single SET structure but working in different regions. There have been several researches published dealing with basic logic gate design such as inverter and NOR gates [13,18, 20–22], however, there is no prior work on how to bias or size SETs so that the desired device characteristics can be achieved. Most research work has focused on device fabrication and modeling using experimental data or assumptions. As a result, it is hard for circuit designers to design complex SET circuits beyond XOR2 gate.

This paper presents a new HSPICE behavioral model modified from Lientschnig’s SET model and a design methodology for SET circuits to extend the PSPICE model to HSPICE and other SPICE simulators for both PC and Unix users, to reduce simulation time, and to make the simulation more stable and accurate. HSPICE behavioral modeling is illustrated in Section 2, and a general method for SET circuit designs based on SET I - V curves and the static CMOS circuit design method is described in Section 3. SET circuit design examples and simulation results will then be given in Section 4, followed by conclusions in Section 5.

2. HSPICE behavioral modeling of SET

The electrostatic energy, ΔE , to move an electron from a quantum node i to another quantum node f as shown in Fig. 1 is given by the following [23]

$$\Delta E = -e(V_f - V_i) + (C_{ii}^{-1} - 2C_{if}^{-1} + C_{ff}^{-1})e^2/2, \quad (1)$$

where C_{ii} , C_{ff} , C_{if} are capacitances of node i and f with respect to ground, and the capacitance between them. If one node is connected to a voltage source, for example node f , C_{ff}^{-1} and C_{if}^{-1} will be modeled equal to 0 [23].

Fig. 2 shows the capacitive-gate SET equivalent circuit, in which single electrons are manipulated one by one through two tunneling junctions under the control of bias and gate voltages applied to the quantum island(o). The top and bottom terminals are assumed without quantum effects and denoted as drain(d) and source(s), respectively in analogy to the MOSFET transistor. The background charges are ignored in the circuit because their effects are determined by the fabrication process. They are assumed in this paper much smaller than the applied charges in the future SET.

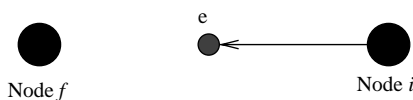


Fig. 1. Move an electron between quantum nodes.

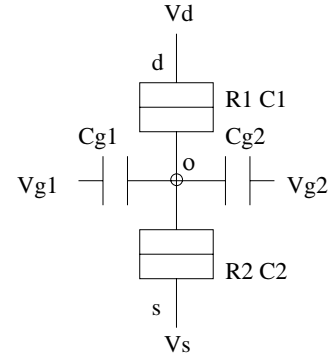


Fig. 2. The capacitive-gate SET schematic circuit.

A single-electron tunneling event can happen only if a transition produces a negative change in electrostatic energy. Because the event takes very short time, even though co-tunneling may happen, the probability of it is quite small. For simplicity, co-tunneling is ignored in the model and could be included in the future. In such a case, four tunnel events can happen

$$d \rightarrow o : \Delta E_{do} = -e(V_o - V_d) + C_{\Sigma}^{-1}e^2/2 \quad (2)$$

$$o \rightarrow d : \Delta E_{od} = -e(V_d - V_o) + C_{\Sigma}^{-1}e^2/2 \quad (3)$$

$$s \rightarrow o : \Delta E_{so} = -e(V_o - V_s) + C_{\Sigma}^{-1}e^2/2 \quad (4)$$

$$o \rightarrow s : \Delta E_{os} = -e(V_s - V_o) + C_{\Sigma}^{-1}e^2/2, \quad (5)$$

where $C_{\Sigma} = C_1 + C_2 + C_{g1} + C_{g2}$ is the total capacitance of the island.

The junction tunnel rate, $\Gamma(\Delta E)$, is formulated based on the orthodox theory and given by [18,23]

$$\Gamma(\Delta E) = \frac{\Delta E}{e^2 R_T (e^{\Delta E/k_B T} - 1)}, \quad (6)$$

where R_T is the tunnel resistance, k_B is Boltzmann’s constant, and T is temperature in Kelvin. For zero temperature

$$\Gamma(\Delta E) = \begin{cases} 0 & \Delta E \geq 0 \\ -\frac{\Delta E}{e^2 R_T} & \Delta E < 0. \end{cases} \quad (7)$$

There would be four tunnel rates associated with the four tunnel events and electrostatic energies.

2.1. State transition diagram

The orthodox theory illustrates the tunnel rate of one electron tunneling through a potential barrier in a single-electron circuit. For many-electron tunneling, the formalism of statistical mechanics and stochastic processes must be included.

If a state k is defined in terms of k extra electrons on the quantum island, the state transition process for a SET is

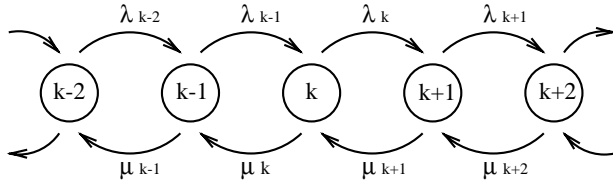


Fig. 3. State transition diagram of a SET.

exactly modeled by the Birth–Death Markov chain [24] shown in Fig. 3, in which the birth rate λ_k is the total tunnel rate that results in an increment of an extra electron on the dot, i.e. a transition to state $k + 1$, while the death rate μ_k is the total tunnel rate that changes the current state k to state $k - 1$. The state probability p_k is calculated by Eqs. (8)–(10) and will be used in calculating SET current in a 11-state window

$$\lambda_k = \Gamma_{do} + \Gamma_{so} \quad (8)$$

$$\mu_k = \Gamma_{od} + \Gamma_{os} \quad (9)$$

$$p_k = p_{k-1} \frac{\lambda_{k-1}}{\mu_k}. \quad (10)$$

2.2. Model implementation

Lientschnig’s SET model structure is simplified and presented in Fig. 4, where the SET is modeled by a voltage controlled current source calculating the SET current based on the orthodox theory and the Birth–Death Markov chain. This structure makes the simulation better convergence than the one in [18] because there is no capacitance coupling between the quantum island and the gates. The voltage of the quantum island is used only as an internal variable of the model, and the way to calculate SET current in G_1 is improved by considering the average current of both junctions.

Since HSPICE only supports a function of parameters, for a function of voltage and/or current variables, it is implemented by a voltage- or current-controlled source. The advantage of this method is that it is more compatible with other SPICE softwares. To implement recursive function

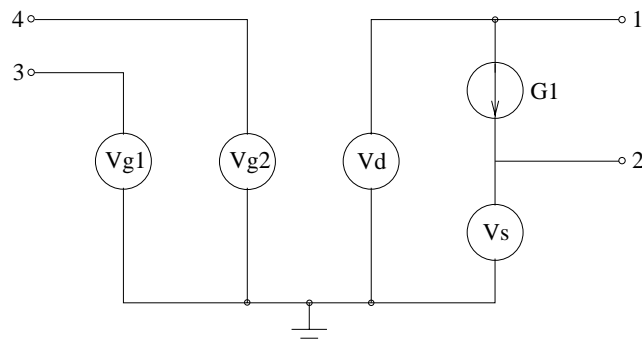


Fig. 4. SET model structure.

calling, function extension is adopted. Fig. 5 shows the HSPICE implementation. Voltage source E_2 in Eq. (12) calculates the most probable electron state n , which is just the opposite of the most probable charge state in [18]

$$E_1 : V_Q = \frac{Q_0 + C_1 V_d + C_2 V_s + C_{g1} V_{g1} + C_{g2} V_{g2}}{e} \quad (11)$$

$$E_2 : V_n = V_Q - \frac{C_{\Sigma}(R_1 V_s + R_2 V_d)}{e(R_1 + R_2)}. \quad (12)$$

E_3 is used to round V_n towards the nearest integer value to simulate the number of extra electrons on the dot using the HSPICE *int* function. As in [18], 11 states are used and can be extended to more states. For simplicity, Fig. 5 only shows three states. E_4 – E_{27} calculate electrostatic energies and tunnel rates formulated by Eqs. (2)–(7). Probabilities of states $n - 1$ and $n + 1$ are calculated by E_{28} and E_{29} according to Fig. 3 and Eqs. (8)–(10), while the state probability of state n is 1. The voltage source E_{30} adds all probabilities together for probability normalization. G_1 in Eq. (13) calculates the current of the island as follows:

$$G_1 : I_{SET} = \sum_n eP(n) \frac{\Gamma_{so}(n) - \Gamma_{os}(n) + \Gamma_{od}(n) - \Gamma_{do}(n)}{2}. \quad (13)$$

2.3. Model verification

The proposed model was first verified by Coulomb blockades and Coulomb oscillations, which are the most typical I – V characteristics of SET and the best indications of how well the model performs. For verification and simplification purposes, gate-2 is biased at 0 V while gate-1 and the drain are used for voltage sweepings. Simulation results in Fig. 6 show clear Coulomb blockades with respect to gate-1 voltage (A) and temperature (B). Fig. 7 gives Coulomb oscillations of swept drain voltage (A) and temperature (B). In addition, Fig. 8 shows the most probable state of the island, i.e. the number of extra electrons on the island, with a bigger drain voltage sweeping range.

Those simulation results of the model match qualitatively with the experimental and simulation data from [8,11, 17,18]. As an example, Fig. 9(a) and (b) from [17] shows the SET currents with respect to V_{gs} and V_{ds} of the MIB model. In (a), for $V_{ds} = 30$ mV the current is from 0 nA to about 7.5 nA, while the HSPICE model gives the current from 3.8 to 7.6 nA. In (b) for $V_{ds} = \pm 60$ mV, the SET currents are about ± 15 nA for all V_{gs} , while the HSPICE model gives ± 14 nA under the same temperature. The quantitative difference between models can be reduced if they are both based on a matured SET fabrication process.

Further verification will be based on SET circuits presented in the following sections.

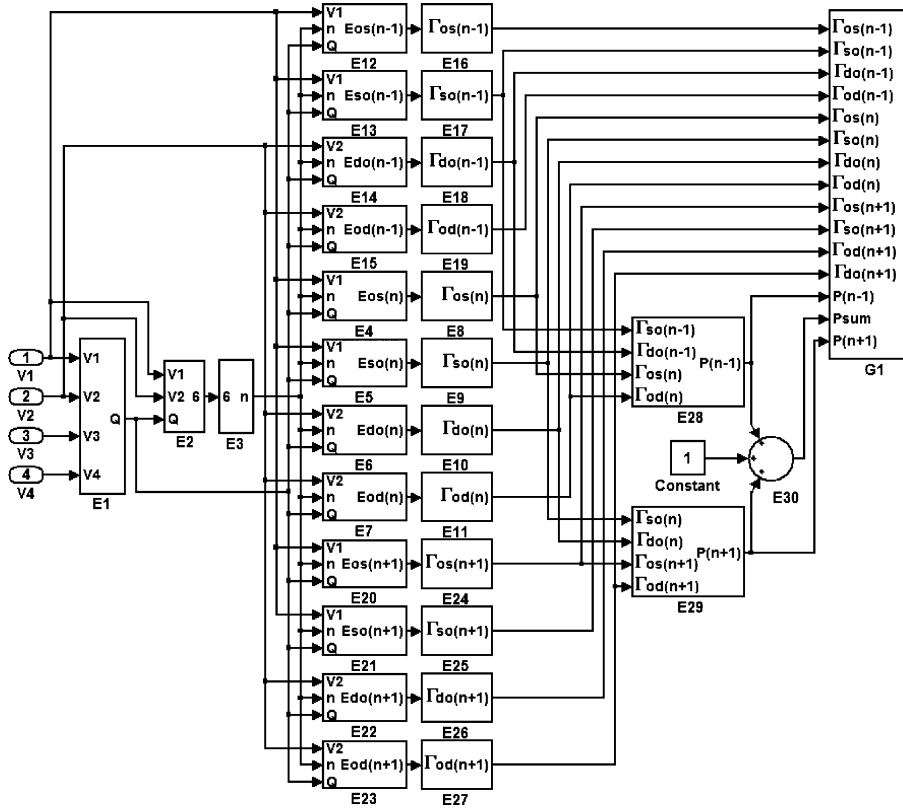


Fig. 5. HSPICE behavioral implementation of SET (three states).

2.4. Performance comparison

The model is compared with Lientschnig’s PSPICE model using the same computer with a Pentium 4 CPU in terms of simulation time. The PSPICE is a Lite Version 9.2, while HSPICE is the Hspui for Windows 2001.2 Version 1.0. All other conditions are the same. Simulation time is compared and given in Table 1, which shows that

the HSPICE model is faster than the PSPICE model under the specific simulation conditions.

Fig. 10 shows our HSPICE simulation result of the currents of junction 1, junction 2, and the average current of both junctions for a SET transistor. From (A), it is clear that all three currents are almost the same, which means using the current of either junction as SET current gives almost the same result. However, the zoomed curve in (B) shows

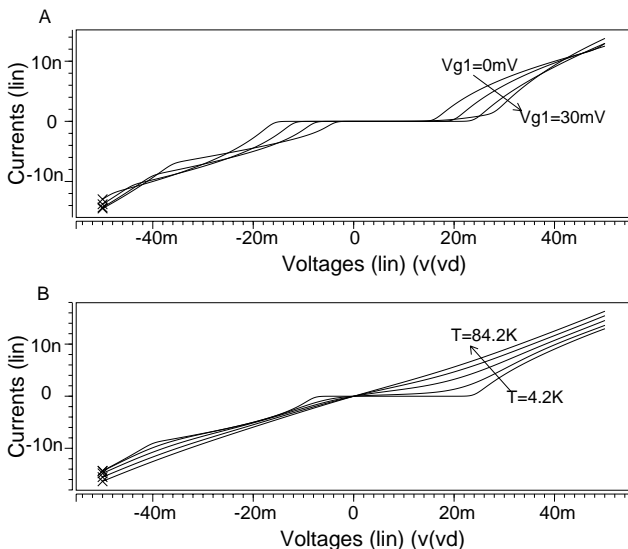


Fig. 6. Coulomb blockades of swept Gate-1 voltage (A) and temperature (B).

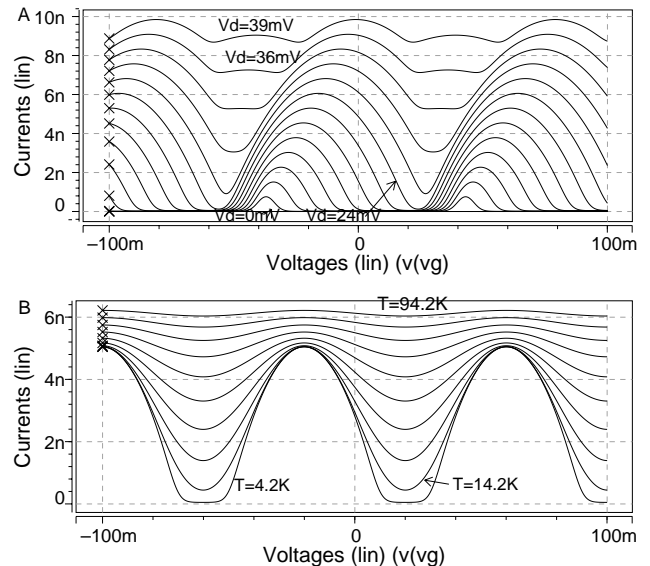


Fig. 7. Coulomb oscillations of swept drain voltage (A) and temperature (B).

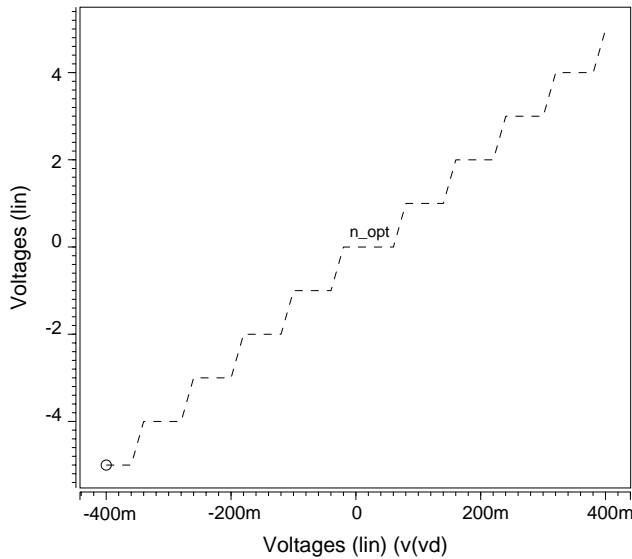


Fig. 8. State of the island.

that in some cases junction 1 and junction 2 have different currents, so that the average of them will give a more accurate description of SET current. Although the error is only around $4f/13p=0.031\%$ in our simulation case, using the average current of both junctions improves accuracy.

3. Complementary SET-based circuit design considerations

Electrical and device parameters can be used for designing a SET-based circuit. Electrical parameters include gate voltages and bias voltages for drain and source. For digital circuits, the voltage level of logic 1 is usually the same as the supply voltage. Therefore, the supply voltage should be determined first in choosing electrical parameters. The next step is to consider biasing issue. Because gate-1 is usually used as the input to a SET, while drain and source are determined by the circuit connections, V_{g2} can be biased for design purposes.

Dimensions of junctions, gates, and the island are the parameters that can be controlled by circuit design engineers. However, device parameters are given to circuit designers by device engineers, and they can affect electrical parameters.

3.1. Specifying supply voltage range

Fig. 7(A) shows the periodic SET current versus V_{g1} under different drain voltages. The junction capacitance is 1 aF and the junction resistance is equal to 1 M Ω . The capacitances for gates are both 2 aF. These curves can be used to determine the range of the drain voltage, i.e. the supply voltage, but should satisfy the following constraints:

- (1) There should be off regions where the transistor is shut off, because for CMOS design, either PMOS or NMOS must be turned off when the other is on. Based on this constraint, a SET supply voltage range from 0 to 24 mV can be concluded.
- (2) The maximum current should be bigger than the required current so that there is some current margin. Changing the junction resistance can also change the SET current, but in order to localize electrons on the quantum island, the junction resistance R_T should be limited by *opaque barriers* [20]

$$R_T > \frac{h}{e^2} \cong 26 \text{ k}\Omega, \tag{14}$$

where h is Planck's constant.

3.2. Biasing SET

A SET can work either as a PMOS- or a NMOS-like device by biasing gate-2 at different voltages. Fig. 11 shows that the SET is changing from PMOS-like devices to NMOS-like devices while gate-2 voltage is sweeping from 0 V to 20 mV. For the case where gate-2 voltage is 0 V, the SET transistor is conducting as the voltage on gate-1 is 0 V, but it turns off gradually as the voltage on gate-1 goes to

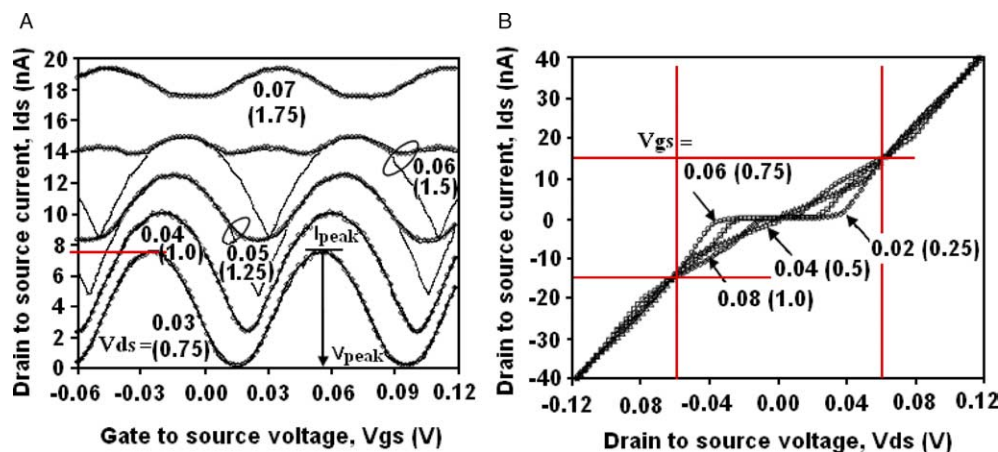


Fig. 9. SET currents of the MIB model.

Table 1
Comparison of simulation time

Gate	# of SETs	Lientschnig's model (s)	HSPICE model (s)
NAND2	4	202	24
NOR2	4	132	34
XOR2	8	296	50

higher. In such a case, the transistor works like a PMOS-like transistor. On the other hand, when gate-2 voltage is biased at 20 mV, the SET transistor works like a NMOS-like transistor. Therefore, according to design requirements, gate-2 can be biased at a certain voltage to get the desirable PMOS- or NMOS-like SET device.

However, in digital circuits, gate-2 is not possibly biased at any voltage but 0 V and the supply voltage. In such cases, sizing gate-2 capacitance can be used to slightly shift the current waveforms as shown in Fig. 12 to get desirable working regions. Not only these two design parameters, but also other parameters such as gate-1 and junction dimensions can be used as design parameters.

As an example, if gate-2 capacitance is sized to 2 aF, the same as the simulation case in Fig. 11, considering the drain voltage requirement described in Section 3.1, a practical choice for SET supply voltage and gate-2 biasing voltage can be 20 mV, which gives almost the same conducting current for both PMOS- and NMOS-like SETs. This 20 mV voltage is used for both SET power supply and logic 1 in this paper.

4. Building CMOS-like static SET circuits

Fig. 13(A) and (B) show a CMOS-like SET NAND2 gate and a XOR2 gate. The junction resistance and capacitance

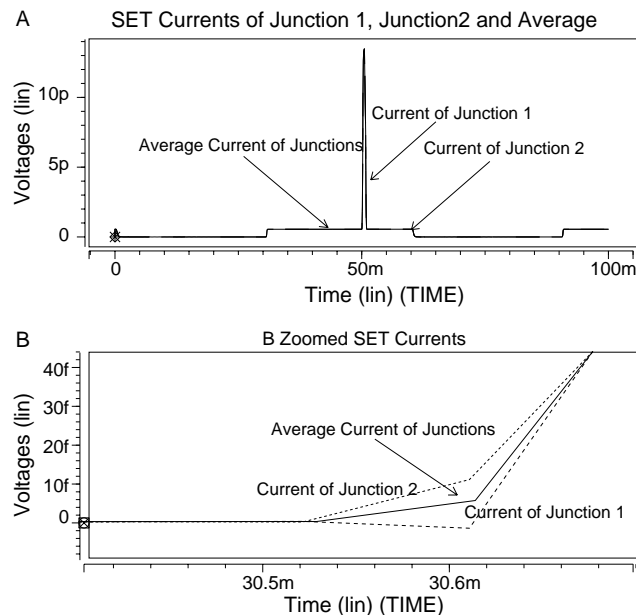


Fig. 10. Comparison of currents.

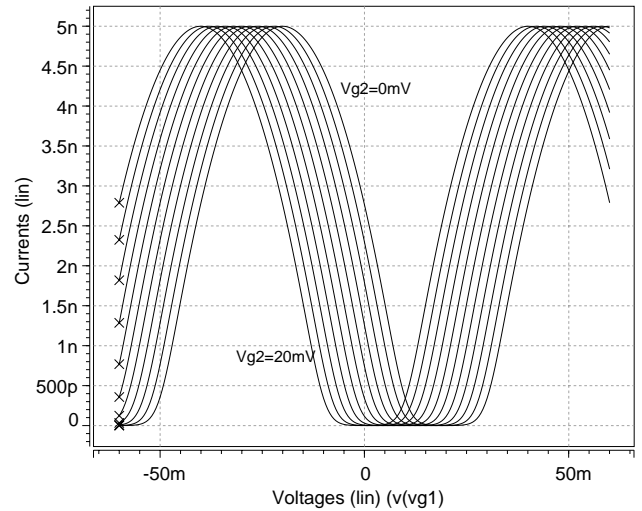


Fig. 11. Biasing Gate2 voltage.

for all the SETs are 1 MΩ and 1 aF, respectively. Although the number of transistors, for example in the XOR2 gate, is more than that in [25], the SET XOR2 gate shares the same circuit structure with a conventional CMOS XOR2 gate. This means the CMOS circuit design method can be applied to very complicated SET circuit designs. Fig. 14 shows the NAND2 gate simulation result. The first three curves from the top are inputs and output, and the fourth curve is the supply current. The power consumed by the SET NAND2 gate is very low and less than 15 pA × 0.02 V = 0.3 pW. Fig. 15 shows a logic verification and output delay measurement of a step input of the XOR2 gate. The propagation delay for driving a typical 10 aF load of the XOR2 gate is 29.8 ns, which is reasonable considering that both the supply voltage and the device size of SET are much smaller than those of CMOS transistors.

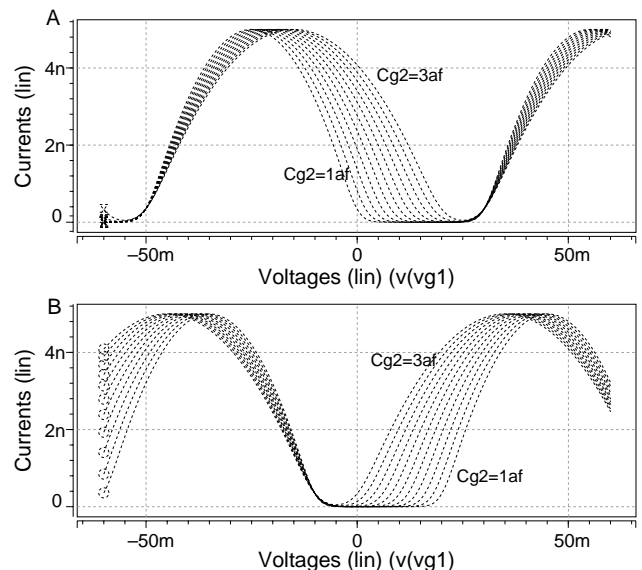


Fig. 12. Sizing Gate-2 capacitance (A) $V_{g2} = 0V$, (B) $V_{g2} = 20 mV$.

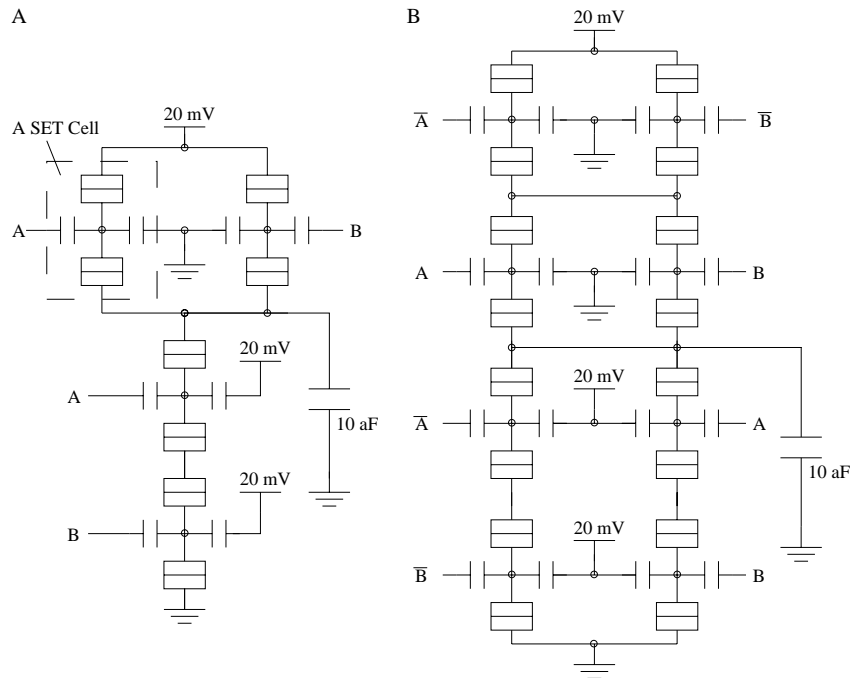


Fig. 13. (A) NAND2 Gate and (B) XOR2 Gate.

5. Conclusions

The HSPICE model presented in this paper provides a way to simulate and design SET and CMOS/SET hybrid circuits in HSPICE environment for both Windows and Unix users. The model can also be modified easily to apply to other SPICE softwares. It is not only a new implementation of Lientschnig’s PSPICE model in another environment, but also a faster, more stable, and more accurate tool. The future work for the model may include the physical parameter extraction based on a matured SET fabrication process.

The SET circuit design method described in this paper presents the idea of how to design complicated SET circuits

based on the static CMOS design method. Simulation results of two SET gates show very low power consumption and reasonable propagation delay. More complicated SET circuits and CMOS/SET interface circuits have already been tested and verified, and they will be published in another paper. Furthermore, not only the static CMOS design method, but also other CMOS circuit design methodologies can be possibly migrated to SET circuit designs based on this idea.

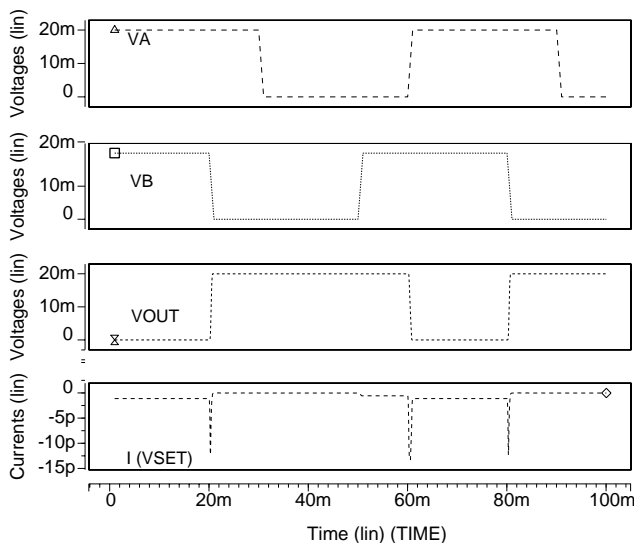


Fig. 14. Simulation result of the SET NAND2 Gate.

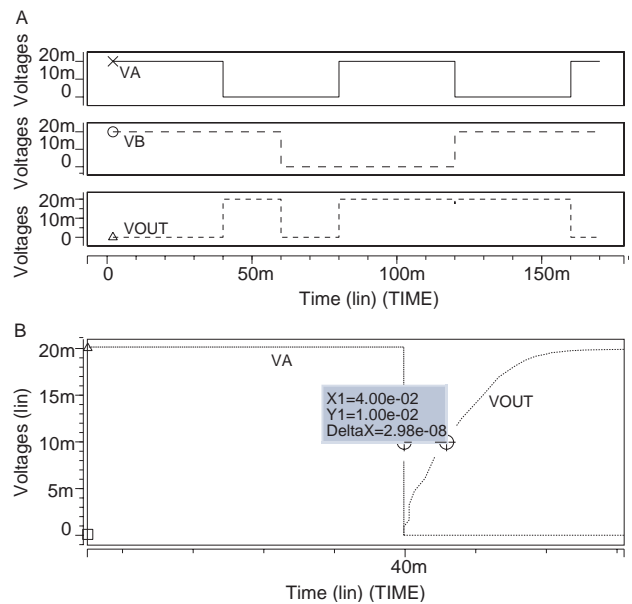


Fig. 15. (A) Logic verification and (B) delay measurement, of the SET XOR2 Gate.

Acknowledgements

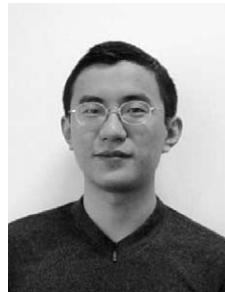
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References

- [1] B. Yu, L. Chang, S. Ahmed, et al., FinFET scaling to 10 nm gate length, *Int. Electron. Devices Meet.* 2002; 251–254.
- [2] R. Martel, V. Derycke, J. Appenzeller et al., Carbon nanotube field-effect transistors and logic circuits, *ACM SIGDA DAC*, 2002.
- [3] J. Redwing, T. Mayer, S. Mohney et al., Semiconductor nanowires: building blocks for nanoscale electronics, *NSF Nanoscale Science and Engineering Grantees Conference*, December 2002.
- [4] W.C.B. Peatman, E.R. Brown, M.J. Rooks, et al., Novel resonant tunneling transistor with high transconductance at room temperature, *IEEE Electron. Device Lett.* 15 (7) (1994).
- [5] P. Hadley, Single-electron tunneling devices, *AIP Conference Proceedings*, 427, Woodbury, New York, 1998, pp. 256–270.
- [6] I. Amlani, A.O. Orlov, G. Toth, et al., Digital logic gate using quantum-dot cellular automata, *Science* 284 (1999) 289–291.
- [7] Y. Chen, G.-Y. Jung, D.A.A. Ohlberg, et al., Nanoscale molecular-switch crossbar circuits, *Nanotechnology* 14 (2003) 462–468.
- [8] D.-H. Kim, S.-K. S., et al., Fabrication of single-electron tunneling transistors with an electrically formed coulomb island in a silicon-on-insulator nanowire, *J. Vac. Sci. Technol.* 20 (4) (2002) 1410–1418.
- [9] D.L. Klein, R. Roth, A.K.L. Lim, et al., A single-electron transistor made from a cadmium selenide nanocrystal, *Nature* 389 (1997) 16.
- [10] E.S. Soldatov, V.V. Khanin, A.S. Trifonov, S.P. Gubin, et al., Room temperature molecular single-electron transistor, *Phys. Usp.* 41 (2) (1998) 202–204.
- [11] C. Wasshuber, H. Kosina, S. Selberher, Simon—a simulator for single-electron tunnel devices and circuits, *IEEE Trans. Comput.-Aided Des. Integrated Circuits Syst.* 16 (9) (1997) 937–944.
- [12] S. Mahapatra, A.M. Ionescu, K. Banerjee, A quasi-analytical set model for few electron circuit simulation, *IEEE Electron. Device Lett.* 23 (6) (2002) 366–368.
- [13] Y.S. Yu, S.W. Hwang, D. Ahn, Macromodeling of single-electron transistor for efficient circuit simulation, *IEEE Trans. Electron. Devices* 46 (8) (1999) 1667–1671.
- [14] Single-electronics group at stony brook. moses, <http://hana.physics.sunysb.edu/set/software/index.html>
- [15] D.V. Averin, K.K. Likharev, Single electronics: a correlated transfer of single electrons and cooper pairs in systems of small tunnel junctions, in: *Mesoscopic Phenomena in Solids*, 1991, pp. 173–271.
- [16] C.H. Hu, J.F. Jiang, Q.Y. Cai, A single-electron-transistor-based analog/digital converter, in: *IEEE Conference on Nanotechnology*, August 2002, pp. 487–490.
- [17] S. Mahapatra, V. Vaish, C. Wasshuber, et al., Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design, *IEEE Electron. Device Lett.* 51 (11) (2004) 1772–1782.
- [18] G. Lientschnig, I. Weymann, P. Hadley, Simulating hybrid circuits of single-electron transistors and field-effect transistors, *IEEE-NANO*, 2002.
- [19] <http://qt.tn.tudelft.nl/research/set/spice/index.html>
- [20] A.M. Ionescu, M.J. Declercq, et al., Few electron devices: towards hybrid cmos-set integrated circuits, in: *The 39th Conference on Design automation*, 2002, pp. 88–93.
- [21] T. Yamanaka, T. Morie, M. Nagata, et al., A single-electron stochastic associative processing circuit robust to random background-charge effects and its structure using nanocrystal floating-gate transistors, *Nanotechnology* 11 (3) (2000) 154–160.
- [22] C.P. Heij, P. Hadley, J.E. Mooij, Single-electron inverter, *Appl. Phys. Lett.* 78 (8) (2001).
- [23] C. Wasshuber, *Computational Single-Electronics*, Springer, Wien, 2001.
- [24] A. Leon-Garcia, *Probability and Random processes for Electrical Engineering* 2nd Edition, Addison-Wesley, Reading, MA, 1994, pp. 476–477.
- [25] M.M. Dasigenis, I. Karafyllidis, A. Thanailakis, A Single-electron XOR gate, *Microelectron. J.* 32 (2001) 117–119.



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