

Clock Grid Simulation Using Transient S-parameter Modeling

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Abstract – Clock grid networks are now common in most high performance microprocessors. This paper presents a new effective modeling and analyzing methodology for clock grid using scattering parameter. It also describes an efficient approach to find the optimum clock grid specification, such as the width and space of the grid metal line. The interconnection of the clock grid is modeled by RC passive elements. The results show that the error is within 10% comparing to Hspice simulation results.

Keywords – Scattering Parameter(S-parameter), Clock Grid, Clock Distribution.

I. INTRODUCTION

For high performance microprocessors, clock grid is an effective alternative to distribute clock signals. However, detailed analyses of clock grids are computationally expensive due to the distributed and dispersive nature of the grids. To simulate and analyze the clock grids, the large number of internal nodes or RC elements overwhelms any circuit simulator. Especially, the simulation and analysis time using Spice-like simulator for the clock grid is excessively long because of many meshes of clock wires.

Several researches have been presented on fast algorithm for the clock grids [1]-[4]. They tried to solve the long simulation time problem by RC network reduction method using moment technology like Asymptotic Waveform Evaluation (AWE) [5]. In addition, RC lumped model was used to represent the clock grids. However, as VLSI systems reach several GHz, the interconnection suffers from high frequency effects such as skin effect, dielectric loss, reflection, and crosstalk. To implement an efficient and accurate modeling and simulation method addressing the issues, a frequency-dependent parameter is required. And also, the detailed inner working of each node in the clock network is usually of little interests to the system design, so the nodes need not to be explicitly represented into computational models.

Scattering parameter [6] is a promising candidate to overcome the problems and satisfy the requirements. It is well suited for the characterizing and modeling of linear clock networks in high frequency.

In this paper, the S-parameter based micromodel for the clock grid using s-parameter is proposed. On the basis of the

model, the effect of the wire-width variation and grid size on clock skew is presented.

The rest of this paper is organized as follows. Section II describes the characterizing and modeling of the clock grid. Section III presents the proposed simulator using s-parameter and the basic grid model. In Section IV, results from the proposed method ranging from 4x4 to 128x128 are given and compared with Hspice simulation followed by conclusion in Section V.

II. CHARACTERING AND MODELING FOR CLOCK GRID

Clock distribution has been a great challenge in the high speed VLSI designs because distribution of the clock network all over the chip with near zero skew becomes a very difficult task. The clock grid is used to achieve the high speed of a clock with the minimum skew and the fast rise time independent of the challenges of the deep submicron technology. It can also reduce the coupling effect, transmission line effect, power collapsing and sensitivity on process variation. The clock grid is typically implemented using the top two metal layers. The grid lines on the same layer are parallel to each other. The grid lines on the two different layers are orthogonal to each other. The end nodes of grid lines on each layer are connected to each other via metal contacts. One end of the contact forms the clock driving node [7][8].

The clock signal arriving on this node drives the gate loads on the chip. A simple RC distributed wire model is used for the modeling of a grid structure. The whole grid structure is composed of grid elements. Each grid element is a segment of wire connecting the two successive nodes. A RC model is established for each grid element. The contact interconnecting the two layers of grid lines is modeled with a contact resistance. Figure 1 shows the basic model for the clock grid which is a crossing point of two grid lines. The model consists of four RC π -models and a metal contact resistor. The edges of the grids are driven by buffered source-clock signals. On a typical chip, there are a number of gates that are driven by clock signals derived from the clock grid nodes.

Even though the model is generated, the delay calculation and skew analysis for the clock grid is very hard and time consuming because of many simultaneous switching drivers and tremendously many parasitic elements. To make efficient analysis and fast simulation for the clock grid, this paper proposes a signal flow graph using S-parameter.

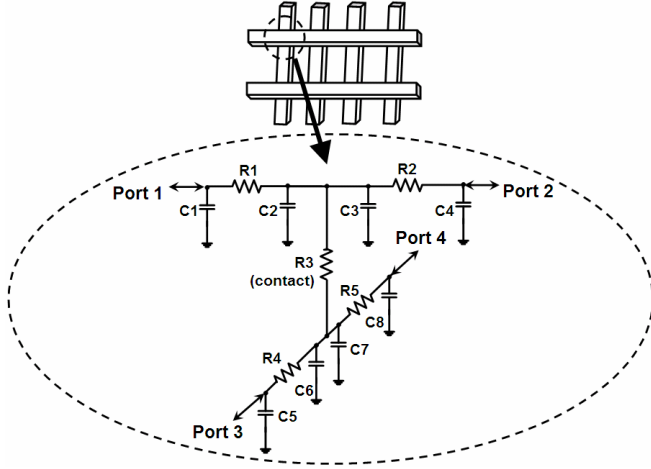


Fig. 1. Basic Model for Clock Grid

III. CLOCK GRID SIMULATOR USING S-PARAMETER

In the Fig. 1, the model has 4-port inputs and 4-port outputs, and can be characterized by 4 x 4 scattering matrix as the following equation.

$$\begin{pmatrix} port1 \\ port2 \\ port3 \\ port4 \end{pmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & s_{14} \\ s_{21} & s_{22} & s_{23} & s_{24} \\ s_{31} & s_{32} & s_{33} & s_{34} \\ s_{41} & s_{42} & s_{43} & s_{44} \end{bmatrix} \times \begin{pmatrix} port1 \\ port2 \\ port3 \\ port4 \end{pmatrix} \quad (1)$$

where all the ports is used as both input and output.

Scattering parameters are a powerful way to describe and model interconnection. They can be measured directly at high frequencies and they exists for all distributed-lumped circuit elements including open and short circuits. And also, the parameters describe transmission lines which are critical in today's high-speed designs. A scattering matrix is employed to relate outgoing waves to incoming waves of a multi-port [9].

Each S-parameter can be obtained from the measured S-parameter in Hspice or the calculated S-parameter from Z-parameter of a single interconnection model [6]. For an N-port component, the S-parameter matrix can be defined as

$$S_{ji}(s) = \left. \frac{b_j}{a_i} \right|_{a_k=0, k \neq i} \quad i, j = 1, 2, \dots, n \quad (2)$$

where s is the complex frequency, a_i and b_i are the incoming voltage wave at port i and the outgoing wave at port j , respectively.

Based on the basic grid element and a single interconnection model, the total clock grid can be partitioned

as shown in Fig. 2, where each small black box is the basic model for the clock grid in Fig. 1.

Assuming that Cell 1 and Cell 2 are connected to gates as output loads, all the S-parameters of the other Cells are calculated using the signal flow graphs [10]. From the Cell 1 and Cell 2 point of view, the calculated S-parameters of the other cells are the effective S-parameter for the whole clock system. Once the effective S-parameter is calculated, Hspice can easily simulate Cell 1 and Cell 2, and measure the skew from input and output load.

The Mason's signal flow graph can be applied to S-parameter networks. Assuming that the network has two ports, the graph is shown in Fig. 3, where Γ_S and Γ_L are input and output reflection coefficients.

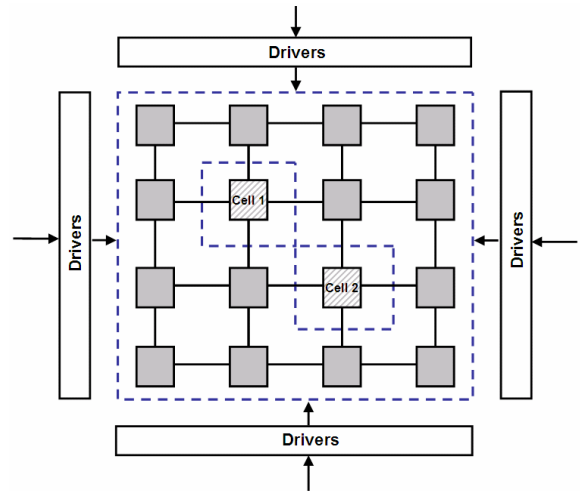


Fig. 2. Partition Method for Clock Grids

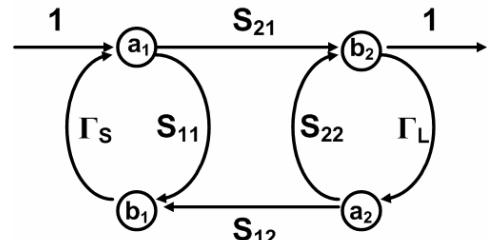


Fig. 3. Mason's Signal Flow Graph of Two Port Network

Using the graph, the transmittance of the network is calculated and it is given by

$$\frac{b_1}{a_1} = \frac{S_{11}(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{(1 - S_{22}\Gamma_L)} \quad (3)$$

where a_1 is the source node and b_1 is the sink node.

There are a few simple rules to simplify the graph as follows.

- (1) The serial paths in the graph are represented by multiplying the weight of the paths.
- (2) The branches joining common nodes are represented by adding the weight of the branches.
- (3) The loop can be removed by dividing the weight of every other edge entering the node by $(1 - \text{the weight of the loop})$.

The proposed simulator is made up of interfacing between Matlab and Hspice as shown in Fig. 4.

In Hspice, S-parameters from two port RC model are extracted, and the extracted S-parameter is added to a lookup table in Matlab. Once the lookup table is created, the entire signal flow graph based on the output load locations is generated. Except the cells with output loads, microcells for all cells are created in Matlab. Finally, Hspice uses the microcells as models, and simulates them with load cells in time.

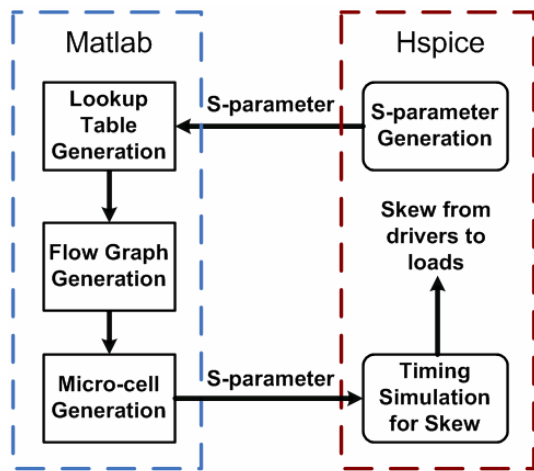


Fig. 4. Block Diagram of the Proposed Simulator

IV. EXPERIMENTAL RESULTS

The proposed S-parameter based simulator for clock grid has been implemented in Matlab and Hspice, and the simulation was run on 500 MHz UltraSPARC-IIe with 500Mbyte memory. In [11], the wire capacitance is the average of all the interlayer capacitances, and the wire resistance is the sheet resistance times the ratio of its length and width. The contact resistance between the two layers of the grid lines takes the value of 2 ohm. The contact resistance between the clock node and the gate takes the value of 10 ohm. The source clock signal buffers are sized to the extent that the rise and fall times of the worst case clock signal are within 10% of the cycle time of the source clock signal, and the buffers are designed in a $0.25\mu\text{m}$ technology.

Table I shows the computational time of clock grids (wire width = $0.1\mu\text{m}$) ranging from 4×4 to 128×128 and the difference rate between Hspice simulation and the proposed method. The first column shows the measured clock grids, and

the second column shows the error rate of the proposed method comparing to Hspice simulation. The third and fifth column represent the CPU simulation time for each simulation. Finally, the fourth and sixth column are the measured skew time for each method. The accuracy of the proposed method is within 10% difference comparing to Hspice results. In addition, the simulation time of the proposed method is much faster than that of Hspice.

Figure 5 shows a comparison of the clock signal at cell 1 in Fig. 2 between Hspice and proposed method. The time simulation results show that the accuracy of the proposed method is comparable to Hspice results.

Table I. Experimental Results for Clock Grids

Clock Grid (NxN)	error (%)	Hspice		Proposed Method	
		CPU Time (sec)	Skew (psec)	CPU time (sec)	Skew (psec)
4x4	5.8%	6.88	19.02	0.51	20.13
8x8	8.0%	18.69	8.23	0.62	8.89
16x16	9.6%	56.89	5.49	1.86	6.02
32x32	2.3%	319.30	4.43	5.29	4.33
64x64	6.6%	2132.43	3.81	19.45	4.06
128x128	7.4%	172853.54	3.80	74.98	4.08

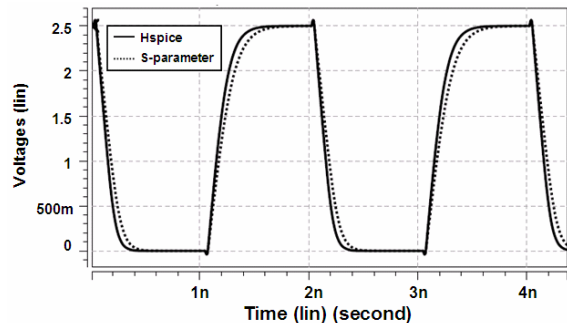


Fig. 5. Clock Signal at the Cell 1 in Fig. 2.

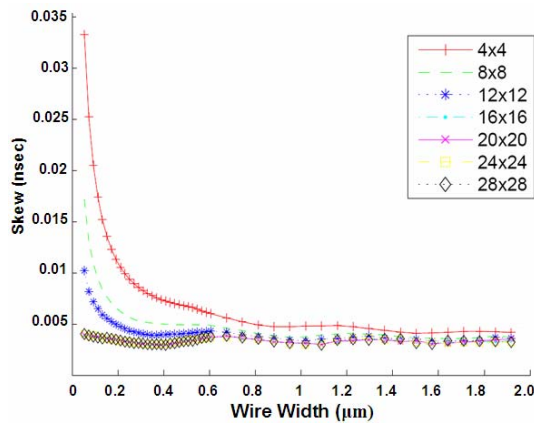
Figure 6 presents the worst-case skew of a clock grid with regard to the variation of wire width and grid size. In the simulation, gate loads is randomly distributed at 20% of the cells, and the source clock signals drive the edge nodes of all the four sides of the grid as shown in Fig. 2.

Figure 6 (a) and (b) show the simulation results of the proposed method and Hspice simulation, respectively. As shown in the figures, the results have the same tendency and the difference rates of the clock skews are very small.

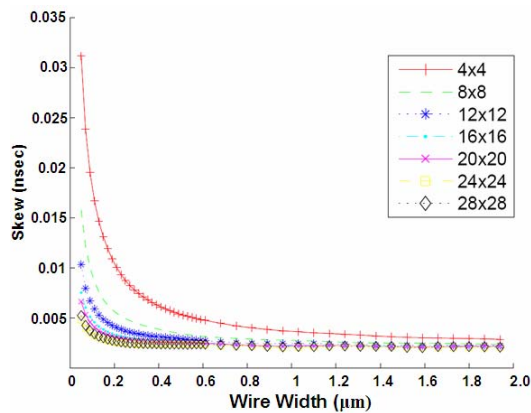
In case of grid size less than 16×16 , the worst-case skew decreases monotonically with the increase of the grid size for a fixed wire width. As the grid size increases further, the skew converges to a certain value regardless of the increased grid size. As for the wire width, the worst-case skew decreased monotonically with the increase of the wire width when the grid size is sufficiently small. However, the slope of this

decreasing quickly flattens with the increase of the wire width. Further, when the grid size exceeds a certain value, the skew is not affected by the change of the wire width. In summary, the clock skew is limited to a certain value by either increasing the grid size and the wire width. The increase in the grid size has more effect on the decrease of the skew than the increase in the wire size.

Therefore, in order to get the optimal value of grid size and wire width, a grid size is firstly determined to meet a clock skew budget where further increasing of the grid size doesn't influence on the skew reducing. Once the grid size is chosen, a wire size can be determined comfortably. To reduce the clock skew more, other design methodologies like buffer insertion needs to be investigated.



(a) Proposed Method (S-parameter Simulation)



(b) Hspice Simulation

Fig. 6. Comparison of the Hspice and the Proposed Method for Clock Skew

V. CONCLUSION

This paper presents a new algorithm for transient simulations of frequency-dependent clock grids characterized and modeled by scattering parameter. Using the modeling for S-parameter, the signal flow graph is generated in Matlab and

the clock skew is calculated in Hspice. This method results in less than 10% errors compared to Hspice and leads to a significant reduction in the simulation time comparing to that of Hspice. It also gives a more accurate and efficient simulation result than those of other reduction algorithm.

In addition, this paper shows an efficient solution of the grid size and wire width for the clock grid.

The proposed methodology can be used effectively in the high speed clock distribution design and also be applied to interconnection analysis including crosstalk and reflection in VLSI system.

VI. REFERENCES

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