

# Reliability Modeling and Assurance of Clockless Wave Pipeline <sup>\*†</sup>

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## Abstract

*This paper presents theoretical yet practical methodologies to model, assure and optimize the Reliability of Clockless Wave Pipeline. Clockless wave pipeline is a cutting-edge and innovative technology as an alternative to traditional pipeline, and a promising computing model towards ultra-high throughput and speed. The basic computational components of such clockless wave pipeline are data waves in association with request signals and switches. The key to the success of clockless wave pipeline is how to coordinate and ensure the processing of datawaves throughout the pipeline in association with the request signals without relying on any intermediate access points under clocked-control. Due to the complication of clockless operations, an efficient and effective method to model and analyze the confidence level (referred to as reliability or yield) of clockless operations of wave pipeline is exigently demanded, but has not yet been adequately addressed, in an integrated level such as datawaves in association with request signals, leaving this as a challenge. In this regard, out-of-orchestration between datawaves and request signals, referred to as datawave fault, is the major concern in assuring and optimizing the reliability of the system. This paper specifically addresses and resolves: extensive and practical clockless-induced datawave-fault modeling; assurance and optimization; clockless-oriented fault tolerant design methods. The proposed methods will establish a sound and adequate theoretical foundation for development of innovative yet practical test/diagnosis/fault-tolerant design methods in early design stage of clockless wave pipeline.*

## 1 Introduction

Clockless wave pipeline is a cutting-edge and innovative technology as an alternative to traditional pipeline, and a promising computing model towards ultra-high throughput and speed. The

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basic computational components of such clockless wave pipeline are data waves in association with request signals and switches. The key to the success of clockless wave pipeline is how to coordinate and ensure the processing of datawaves throughout the pipeline in association with the request signals without relying on any intermediate access points under clocked-control. Due to the complication of clockless operations, an efficient and effective method to model and analyze the confidence level (referred to as *reliability* or *yield*) of clockless operations of wave pipeline is exigently demanded, but has not yet been adequately addressed, in an integrated level such as datawaves in association with request signals, leaving this as a challenge. The confidence level is primarily determined by the reliability of the clockless orchestration of datawaves and their associated request signals under switch arrangements for datawave alignment. In this regard, out-of-orchestration between datawaves and request signals, referred to as delay fault, is the major concern in assuring and optimizing the reliability of the system. New faults, referred to as *Intra-Wave Fault*, *Inter-Wave Fault* and further *Request Signal Faults*, are proposed in our previous paper[17]. The proposed fault models help reveal fundamental yet essential characteristics of the reliability of the clockless wave pipeline, and enables efficient and effective reliability assurance and optimization. The intra/inter-wave faults are used as the primary drivers to maneuver the evaluation method of the fault-impacts on the reliability with respect to extensive delay-sensitive design parameters such as delay distribution, delay variation, crosstalk noise, intra/inter-wave of datawaves, request signal and other elements. The proposed research will establish a sound and adequate theoretical foundation for development of innovative yet practical test/diagnosis/fault-tolerance method in early design stage of clockless wave pipeline.

The specific objectives of the paper are: clockless wave pipeline-specific fault models will be established as the primary drivers for yield and reliability modeling, assurance and optimization; the paper will provide a thorough *characterization* and *parameterization* of the representative clockless wave pipeline-specific faults such as intra-wave fault, inter-wave fault, and request signal fault; theoretical and parametric *yield optimization* will be conducted with respect to the characteristics and parameters identified in the proposed fault models; fault tolerant design methods with respect to datawave faults will be developed, and a novel yet solid yield models for the proposed fault tolerance will be established for efficient and effective manipulation of extensive fault tolerance; circuit simulation-based model validation will be conducted to verify the efficiency and effectiveness of the proposed models and methods.

This paper is organized as follows. Section II introduces the theoretical and technical background of wave pipeline. The proposed fault models on clockless wave pipeline are described in Section III. In Section IV, the proposed design for reliability techniques are described for datawave faults. Then, the conclusions and discussions are drawn in the final section.

## 2 Preliminaries and Review

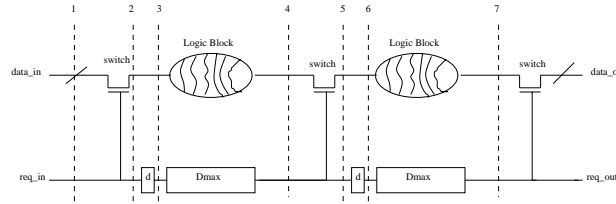
Wave pipeline is a pipeline processing technique that can increase the throughput without increasing internal storage spaces and power consumption [1, 6, 11, 12, 13]. Multiple datawaves can propagate through the wave pipeline from the PI (Primary Input) to the PO (Primary Output) simultaneously without internal latching. It can ideally achieve the theoretical maximum performance, and draws lots of attentions in the industry nowadays.

Wave pipeline can be built either in a synchronous or an asynchronous manner. Synchronous wave pipeline uses clock signal to synchronize the movement of datawave bits. It has been successfully deployed in several commercial processors such as floating point unit in IBM 360/91 [2] and

external caches in HP PA8000 [3]. Asynchronous wave pipeline uses request and acknowledgement signals, or only request signal instead of a global clock to serve as a reference signal (note that the asynchronous wave pipeline with request signal only is referred to as *clockless wave pipeline* in this paper). Asynchronous wave pipeline is relatively more difficult to deploy than synchronous wave pipeline due to its explorativeness and a few technological hurdles as mentioned before. Clockless wave pipeline circuit has only been experimented in non-commercial sectors such as the two-phase clockless wave pipeline which uses only a single request signal line [4, 5]. The specific architectural model investigated in this paper is the two-phase clockless wave pipeline [5] since it is ideally supposed to yield [15, 16] the theoretical maximum performance.

In conventional pipeline, there are registers or latches between any two stages, and there is only one datawave active in any stage at any time. The clock cycle time is determined by the maximum stage path delay, i.e.,  $T_{ck} \geq D_{max}$ . Wave pipeline remove all of the internal registers or latches, and let multiple datawaves propagate through the circuit at the same time, thus the throughput is enhanced greatly. The clock cycle time of wave pipeline with clock is determined not by the maximum path delay but the difference between the maximum path delay and minimum path delay, and its clock cycle [7, 8, 9, 14] is  $\frac{T_{max}}{N} < T_{ck} < \frac{T_{min}}{N-1}$ , where  $N$  is the number of waves in the circuit (degree of the wave pipeline).

Clockless wave pipeline is an asynchronous circuit. A *two-phase asynchronous wave pipeline* was proposed by Hauck and Huss in [5] as shown in Figure (1), which has the two-phase operation by alternating positive and negative level-sensitive switches, and it employs request signal only.



**Figure 1. Two-phase asynchronous wave pipeline [5]**

As shown in Figure (1)[5], two types of switches, namely positive and negative switches, logically and physically partition the circuit into several pipelined stages for datawave progress alignment purpose, and request signal controls the switches. A pair of a datawave and a request signal level (either at the high or low pulse) enters the clockless wave pipeline at the same time in full-association, and they must stay so throughout during the propagation of the datawave. The switch can be *opaque* or *transparent* to the datawaves. If opaque the switch latches the datawave, and if transparent the datawave passes the switch without latching. Specifically,  $N$  type switches (negative switches) are made to be opaque to the datawaves associated with a high request signal, and transparent to those associated with a low request signal. Symmetrically,  $P$  type switches (positive switches) are made to be transparent to the datawave associated with a high request signal, and opaque to those associated with a low request signal. The propagation of the datawave within pipelined circuit is intermittent. Once the datawave enters the circuit, it is assigned a request signal alternately, high or low level. Then, by the design rule as defined, the datawave associated with a high request signal propagates through  $N$  switches without stopping for alignment, but has to be latched at  $P$  switches. Symmetrically, the datawave associated with a low request signal propagates through  $P$  switch without stopping, but has to stop and be latched at  $N$  switches.

Two representative delay-fault models of *synchronous wave pipeline* are proposed as follows.

- Wave Delay Fault [10]: The timing constraint in synchronous wave pipeline is two-sided such that each datawave must obey the *setup* and *hold* time constraints at each end of its current clock cycle, for correct synchronization. Violation of the two-sided clock-timing constraint, such as setup or hold time error, is referred to as wave delay fault.
- Wave Fault [10]: In order for successive datawaves propagate and stay in correct operation back to back, it is required that each datawave must stay within the time-range of the clock cycle period in association. Thus, wave delay fault may further create wave faults. Wave fault is very likely to cause signal invalidation such as spikes or no-signals.

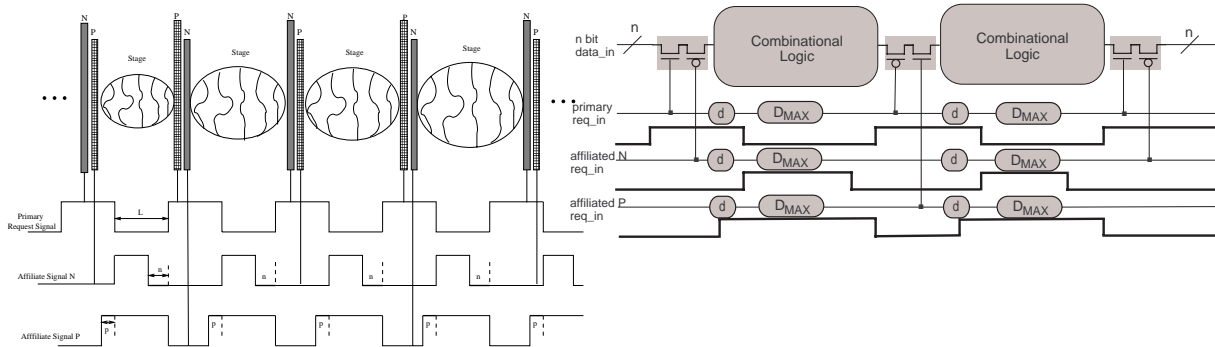
In order to efficiently and effectively depart from the delay fault models of conventional synchronous wave pipeline, we propose two new fault models. The *Intra-Wave Fault Model* is based on the *Pulse Fault Model* as proposed in our previous work [18]. Based on the intra-wave fault model, we introduce the *Inter-Wave Fault Model* to provide a comprehensive yet essential understanding of the fault mechanism of clockless wave pipeline. The fault models are used as the theoretical basis for the proposed yield modeling, assurance and optimization method. Also, we will take into account a synergistic fault model in which specifically the co-relation of intra/inter-wave faults with the request signal faults, because correct association between datawaves and request signal primarily determines the delay-oriented yield and reliability.

### 3 Proposed Design for Reliability

We propose a basic yet novel framework to establish incisive models and methods to facilitate the reliability optimization process. The proposed design-for-reliability method will reduce or possibly completely tolerate the proposed intra-wave and inter-wave faults. As the intra-wave fault is the necessary but insufficient condition for an inter-wave fault to occur, we focus our modeling and fault tolerance on the improvement of intra-wave fault-related yield. Inter-wave fault-related yield improvement can also be realized by relating the inter-wave fault model to the intra-wave fault model. The main concern of the proposed method is to control the shape of the datawaves to maintain their width (i.e.  $d_{max} - d_{min}$ ) within  $L$  (i.e. the length of the request signal pulse in association).

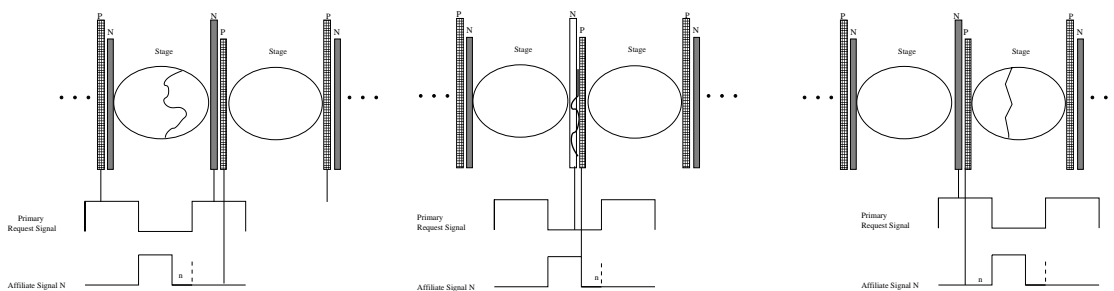
The proposed basic framework for reliability optimization employs a novel idea of *Duplex Switches* in association with *Affiliate Request Signals*.

The proposed duplex switch, as shown in Figures (2) and (3), consists of two switches connected in series and each of which is in opposite polarity. There are two types of duplex switches such as *PN-switch* (i.e. series connection of P and N type switches) and *NP-switch* (i.e. series connection of N and P type switches). The duplex switches can be deployed such that each type of duplex switch is alternately placed through the circuit. The alternate placement of duplex switches enables the proposed *Double Alignment Method*, i.e. datawaves are given another chance for alignment. Hence, there are two possible such arrangements we can consider to demonstrate the double alignment methods as PN-NP-PN and NP-PN-NP. As the two arrangements are symmetric, we will demonstrate only the first arrangement of PN-NP-PN as shown in Figures (4), (5) and (6). In Figure (4), it is shown that a datawave is propagating through the stage in between the first PN and NP; the datawave, which was initially supposed to be completely aligned (i.e. the first alignment) at the P-switch in the first PN-switch, is then getting out-of-alignment during the propagation due to variation of each path-delay; the datawave is associated with its primary request signal with low-level; the affiliate request signal with low-level in length  $n$  is provided to control the double alignment. Figure (5) demonstrates the double alignment method: at the NP-switch the datawave



**Figure 2. Architecture of the reliability enhanced 2-phase clockless wave pipelined pipeline**

just passes through the N-switch because the datawave is associated with low-level primary request signal and the N-switch is transparent to low-level request signal; passing through the N-switch, the datawave then gets aligned at the P-switch (i.e. the second-chance alignment) in association with the low-level affiliate request signal for the  $n$  period of time because P-switch is opaque to low-level request signal; the second-chance alignment period  $n$  can be determined by the expected extent of the out-of-alignment (note that in the symmetric case of NP-PN-NP, the high-level affiliate request signal spans for the  $p$  period of time). In Figure (6), it is shown that the datawave has got aligned back through the double alignment; *the proposed double-alignment-method will definitely reduce the chance for an intra-wave fault to occur, thereby consequently reducing the chance for an inter-wave fault as well.*



**Figure 4. Before passing the middle N switch**  
**Figure 5. Passing the middle N switch and P affiliated switch**  
**Figure 6. After passing the middle N switch and P affiliated switch**

To demonstrate the validity of the proposed fault tolerant method for the datawave faults, we use a modeling and assurance method as follows.

Assume a random variable  $x$  with a normal distribution to represent the path-delay of a bit in a datawave without the duplex switches; and  $y$  with the duplex switches. The p.d.f. of  $x$  can be expressed as follows:  $f_x(t) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(t-\mu)^2}{2\sigma^2}}$ . In order to manipulate the extra-delay induced by the double-alignment, we introduce a parameter  $\gamma$  such that the value of the effective extra-delay is

**Table 1. Parameter Values Simulated**

-	# path	path 1	path 2	path 3	path 4
$S_0 - S_2$	2	22	26	-	-
$S_1 - S_3$	3	64	62	56	-
$S_2 - S_4$	4	34	32	30	28

$n \times \gamma$  (or symmetrically  $p \times \gamma$ ).  $y$  is the random variable of our concern since that represents the new delay variable with the duplex switches employed, and is to be formalized in terms of the path-delay variable without the duplex switches (i.e.  $x$ ). In the analysis, there is a specific path-delay value  $z$  of  $x$  at which the duplex switch makes effect to increase  $y$  from  $x$  (i.e.  $z$ ) to  $x + n\gamma$  (i.e.  $z + n\gamma$ ).

The overall  $f_y(y)$  is as follows and verifies the correctness of the proposed model.

$$\begin{aligned}
 f_y(y) &= \int_{-\infty}^{z-n\gamma} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y-\mu)^2}{2\sigma^2})} dy + \int_{z-n\gamma}^{z+n\gamma} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y-\mu)^2}{2\sigma^2})} dy + \int_{z+n\gamma}^{\infty} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y-\mu)^2}{2\sigma^2})} dy \\
 &= \int_{-\infty}^{+\infty} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y-\mu)^2}{2\sigma^2})} dy \\
 &= 1
 \end{aligned} \tag{1}$$

Without loss of generality, we assume a functional independency between PN-duplex-switches and NP-duplex switches, and the intra-wave fault rate for each type of duplex switch (i.e.  $i^{th}$  *n*type for a PN-duplex switches and  $j^{th}$  *p*type for an NP-duplex switch) can be expressed as follows, respectively.

$$P_{i'th-n_{i}type} = \int_{-\infty}^{d_{min_i} - (L - \alpha_i - \Delta_i)} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y - n \times \gamma - \mu)^2}{2\sigma^2})} dy + \int_{d_{max_i} + \alpha_i}^{+\infty} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y-\mu)^2}{2\sigma^2})} dy \tag{2}$$

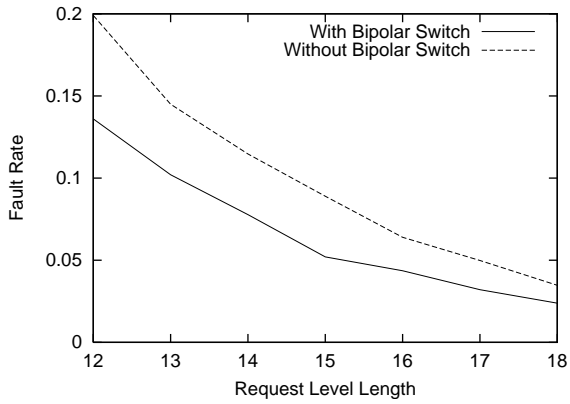
$$P_{j'th-p_{j}type} = \int_{-\infty}^{d_{min_j} - (L - \alpha_j - \Delta_j)} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y - p \times \gamma - \mu)^2}{2\sigma^2})} dy + \int_{d_{max_j} + \alpha_j}^{+\infty} \frac{1}{\sqrt{2\pi\sigma}} e^{(-\frac{(y-\mu)^2}{2\sigma^2})} dy \tag{3}$$

Thus, assuming there are  $n$  number of *n*type duplex switches and  $p$  number of *p*type duplex switches in-placed, the overall intra-wave fault rate ( $P_{overall}$ ) can be expressed as  $P_{overall} = 1 - \prod_{i=1}^n (1 - P_i) \times \prod_{j=1}^p (1 - P_j)$ . Therefore, the overall yield,  $Y$ , is  $Y = 1 - P_{overall}$ .

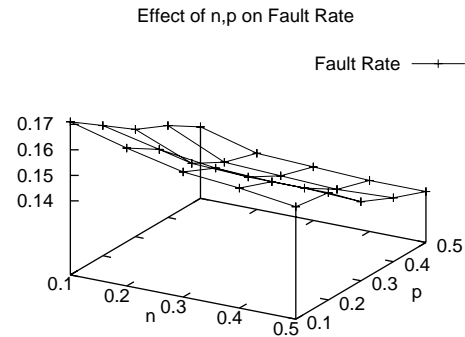
For a simulation purpose, suppose there is a clockless wave pipelined circuit with 5 switches (e.g., S0 - S4 as given in Table 1). Also, suppose that the number of paths within any partial circuit (i.e. the number of paths in each row as given in Table 1), and the delay on each path is known.

The simulation based on this architecture is carried out with focus on the following three analysis: to analyze the effectiveness of request signal length on fault rate with  $n, p = 0.4$  and  $\gamma = 0.6$ ; to analyze the effectiveness of  $n, p$  on fault rate and yield with  $L = 12$  and  $\gamma = 0.6$ ; to analyze the effectiveness of  $\gamma$  on fault rate with of  $L = 12$  and  $n, p = 0.4$ . They are illustrated in Figure (7), (8),(9),(10).

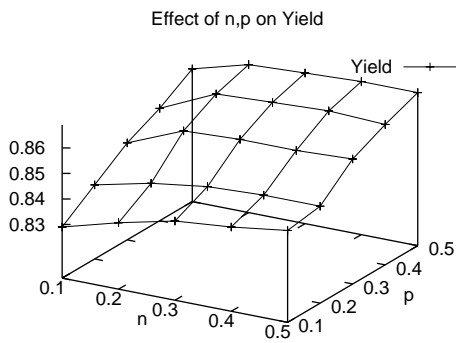
The simulation results demonstrate that the proposed fault tolerant technique using the duplex switches has a great impact on the intra-wave fault rate. Note that the simulations is conducted only



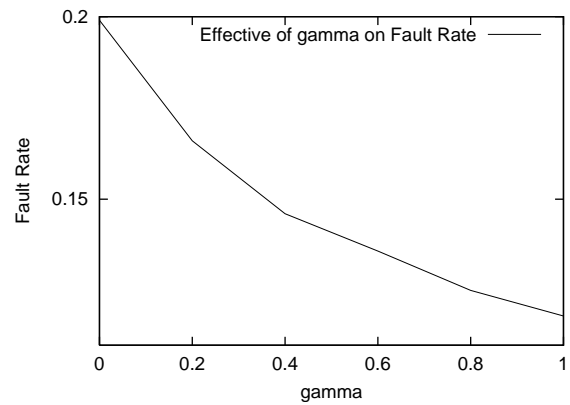
**Figure 7. Fault Rate with/without Duplex**



**Figure 8. Effectiveness of n, p w.r.t. Fault Rate**



**Figure 9. Effectiveness of n, p w.r.t. Yield**



**Figure 10. Effectiveness of  $\gamma$  w.r.t. Fault Rate**

with respect to intra-wave fault because inter-wave fault functionally depends on intra-wave fault as proved in this paper. Figure (7) shows that the fault rate with duplex switches of the clockless wave pipelined circuit is significantly lower than the equivalent circuit without duplex switches. As the request level length grows, both of the fault rates are reduced, and still the one with duplex switches is lower. Figure (8), (9) show the effectiveness of the  $n$  and  $p$  with respect to the overall fault rate and yield, respectively. When  $n$  and  $p$  become larger, the effectiveness of reducing the fault rate and enhancing the yield become greater. Figure (10) shows the effectiveness of  $\gamma$  with respect to the fault rate. It is demonstrated that  $\gamma$  is another design-factor to consider to improve the fault rate and yield as well.

## 4 Conclusions and Discussion

This paper has presented theoretical yet practical methodologies to model, assure and optimize the *Reliability of Clockless Wave Pipeline*. The fault tolerance datawave approach has been proposed under the fault models in order to realize a reliable clockless wave pipeline,

It was demonstrated that the proposed duplex switches 2-phase clockless wave pipeline with redundant affiliate request signals cause the reduction on the data skew along the datapaths. As the intra-wave fault is caused by the data skew on different data paths, the duplex switches in association with the affiliated request signals can effectively slow down the propagation speed of the faster data bits without affecting the propagation of the slower data bits. Therefore, the data skew rate has been reduced and consequently the intra-wave fault rate has been wffectively reduced as well. Numerical experiment and simulations have demonstrated and verified the efficiency and effectiveness of the proposed reliability modeling and assurance methods and fault tolerant design for reliability.

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