



# Design metal-dot based QCA circuits using SPICE model

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## Abstract

This paper proposes a SPICE model development methodology for quantum-dot cellular automata (QCA) cells and presents a SPICE model for QCA cells. The model is validated by simulating the basic logic gates such as inverter and majority voter. The proposed model makes it possible to design and simulate QCA combinational circuits and hybrid circuits of QCA and other NANO devices using SPICE. In the second half part of the paper, SET and QCA co-design methodology is proposed and SET is used as a readout interface of the QCA cell array. The SET and QCA hybrid circuit is a promising nano-scale solution.

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## 1. Introduction

With continuously scaling of CMOS technology below 100 nm, problems such as ultrathin gate leakage and doping fluctuations arise and result in increasing of failure density and power density level. These issues will finally block the future down-scaling of CMOS process. Novel materials and technologies have been extensively researched or developed at nano-scale to replace conventional lithography based VLSI technology in recent years. These emerging technologies include SET (single electron device), RTD (resonant tunneling devices), nano-tube, nano-wire and QCA (quantum-dot cellular automata). Among them, QCA plays an important role not only because it provides a solution to build circuits at nano-scale, but also offers a new methodology of computation and information transformation. The feature size of the basic QCA cell can be as small as few nanometers by molecular implementation at a room temperature [1]. In an abstract way, a basic QCA cell can be considered consisting of four quantum dots located at the four corners of a square array and coupled by tunnel barriers. Electrons can travel

between the adjacent corners by tunneling through the barriers in a cell, and high inter-cell barriers suppress the electrons to tunnel out of a cell. If there are two extra electrons bounded in a cell, they must be forced to locate on the opposite corners of the cell due to Coulomb repulsion in ground states. Consequently, these two ground states can be used to represent the logic '0' and '1' as shown in Fig. 1. Based on basic QCA cells, [2–5] have demonstrated and designed QCA wires, QCA majority voter, inverter, and more complicated circuits such as full-adder, H-memory structure, and 12-bit microprocessor. In recent years, digital circuits design usually needs millions of logic gates. Therefore, for the actual application and further research, CAD tools for QCA circuits design are essential. QCADesigner is a QCA layout and simulation tool developed by ATIPS laboratory [6]. This simulator uses the nonlinear approximation for determining the polarization of cells [7]. This software can be used to draw QCA layout with basic cells and do logic simulation, however it uses a bottom-up design methodology which is not efficient for large circuits design. Furthermore, it is not compatible with traditional CMOS design softwares and therefore it is unsuitable for QCA and CMOS or other NANO technology co-design. HSPICE is a popular and accurate simulator for traditional CMOS circuits design. This paper is organized as follows: QCA SPICE behavioral model is deduced in Section 2 based on metal-dot based physical implementation. Section 3 illustrates the basic QCA gates simulation using

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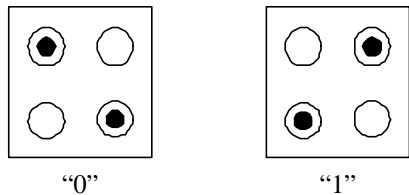


Fig. 1. Two ground-state polarizations of basic four-dot QCA cell.

HSPICE. Section 4 introduces QCA and SET co-design methodology and Section 5 concludes the paper.

## 2. QCA cell SPICE model

Researchers have fulfilled many experiments to demonstrate the behavior of QCA cells [4,8,9,14]. In these experiments, the ‘push–pull’ signal (the sign of the voltage on one input dot opposite to the one on another input dot) [14] is used to polarize the input dots and the polarization direction of the output dots is detected by measuring the output voltages using voltage meters. Our SPICE model is based on those experimental verifications on the behavior of QCA cells. As shown in Fig. 2, a possible realization of a basic QCA cell consists of two series-connected metal dots separated by tunneling barriers and capacitively coupled to the second pair of identical double dots based on existing technology [14]. Since the left half and the right half of a QCA cell are exactly symmetrical, the model for the half-QCA cell is built first, and then two of them can be combined together to develop the whole QCA cell model. The schematic diagram of the simplified half-QCA cell is shown in Fig. 2(b). The two black dots represent two quantum dots and T1 is a tunneling junction. Electrons are able to tunnel between the islands through the tunneling junction T1 but cannot leave these two islands [11]. The electrostatic energy to move an electron from one island  $i$  to another island  $j$  is given by [15]

$$\Delta E = -e(v_j - v_i) + (C_{ii}^{-1} - 2C_{ij}^{-1} + C_{jj}^{-1})e^2/2, \quad (1)$$

where  $C_{ii}$ ,  $C_{jj}$  and  $C_{ij}$  are capacitances of nodes  $i$  and  $j$  with respect to ground, and the capacitance between them.  $v_i$  and  $v_j$  are the voltages on island  $i$  and  $j$  before the electron has

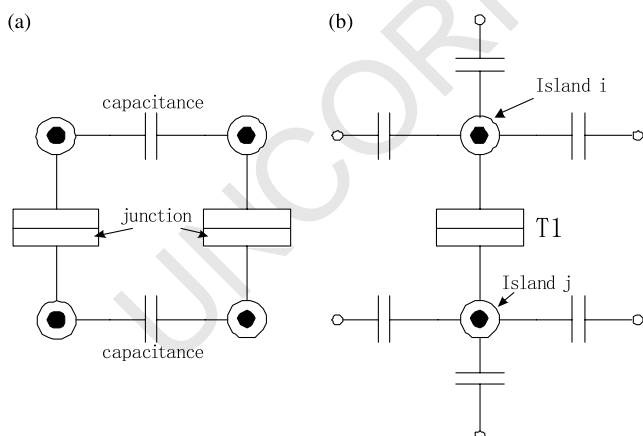


Fig. 2. (a) Two-junction realization of a quantum cellular automata. (b) A schematic diagram of a half-QCA cell.

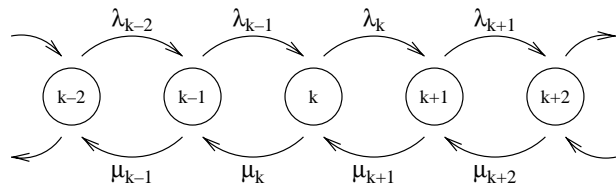


Fig. 3. The state transition diagram of the birth-and-death process.

tunneled from node  $i$  to node  $j$ . If a state  $k$  is defined in terms of  $k$  extra electrons on the quantum island, the state transition process of single electron tunneling is modeled by the birth-and-death Markov chain as shown in Fig. 3. According to steady-state probabilities and global balance equations

$$p_k = p_{k-1} \frac{\lambda_{k-1}}{\mu_k}, \quad (2)$$

where  $p_k$  is the probability that one island holding  $k$  electrons and  $\lambda_k$  is the transition rate from state  $k$  to state  $k+1$  and  $\mu_k$  is the transition rate from state  $k$  to state  $k-1$ . In a simple case, there is only one extra electron in one pair of quantum dots. Therefore, only two states exist. One state is the extra electron trapped in island  $i$  and the other state is island  $j$  holding the extra electron. Hence, the following expression is obtained

$$P_{i=1,j=0} \Gamma_{i \rightarrow j} = P_{i=0,j=1} \Gamma_{j \rightarrow i}, \quad (3)$$

where  $\Gamma_{j \rightarrow i}$  is the tunnel rate for an electron tunneling from island  $j$  to island  $i$ .  $P_{i=a,j=b}$  represents the probability that node  $i$  holding  $a$  electrons while node  $j$  has  $b$  electrons ( $a, b$  can be either 0 or 1). The tunnel rate is formulated based on the orthodox theory [12] and given by [15]

$$\Gamma(\Delta E) = \frac{\Delta E}{e^2 R_T (e^{\Delta E/k_B T} - 1)}, \quad (4)$$

where  $R_T$  is the tunnel resistance,  $k_B$  is Boltzmann’s constant,  $T$  is temperature, and  $\Delta E$  is the energy difference calculated from Eq. (1). There can be one to three voltage sources connected to each island depending on the placement of other QCA cells around this QCA cell, and  $C_{im}$  ( $m$  from 1 to 3) is the corresponding input capacitance for each input with voltage source  $V_{im}$  of island  $i$ . According to the model shown in Fig. 2, the following equations can be obtained using the simple electrostatics

$$V_{i=1} = \frac{\sum_m V_{im} C_{im} + V_{j=0} C_{T1} - e}{C_S}, \quad (5)$$

$$V_{i=0} = \frac{\sum_m V_{im} C_{im} + V_{j=1} C_{T1}}{C_S}, \quad (6)$$

$$V_{j=1} = \frac{\sum_m V_{jm} C_{jm} + V_{i=0} C_{T1} - e}{C_S}, \quad (7)$$

$$V_{j=0} = \frac{\sum_m V_{jm} C_{jm} + V_{i=1} C_{T1}}{C_S}, \quad (8)$$

where  $V_{i=1}$  is the voltage of node  $i$  with the extra electron and  $V_{i=0}$  is the voltage of node  $i$  with no extra electron.  $C_S$  is the total capacitance of node  $i$  and  $j$ . We assume that the total capacitances

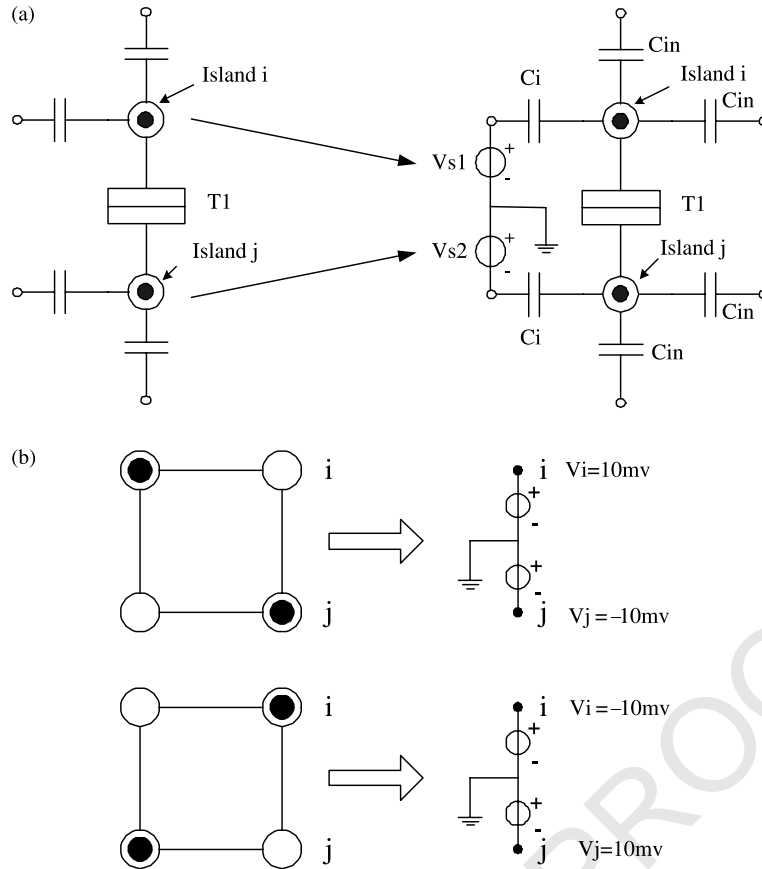


Fig. 4. (a) The model of QCA cell in SPICE. (b) The equivalent voltage sources correspond to the polarizations of QCA cells.

of island  $i$  and  $j$  are the same.  $C_{T1}$  is the capacitance of tunneling junction  $T1$ . Solving the above four equations, the voltages of island  $i$  and  $j$  can be expressed as follows:

$$V_{i=1} = \frac{(\sum V_{im} C_{im} - e)C_S + (\sum V_{jm} C_{jm})C_{T1}}{C_S^2 - C_{T1}^2}, \quad (9)$$

$$V_{j=0} = \frac{(\sum V_{im} C_{im} - e)C_{T1} + (\sum V_{jm} C_{jm})C_S}{C_S^2 - C_{T1}^2}, \quad (10)$$

$$V_{i=0} = \frac{(\sum V_{im} C_{im})C_S + (\sum V_{jm} C_{jm} - e)C_{T1}}{C_S^2 - C_{T1}^2}, \quad (11)$$

$$V_{j=1} = \frac{(\sum V_{im} C_{im})C_{T1} + (\sum V_{jm} C_{jm} - e)C_S}{C_S^2 - C_{T1}^2}. \quad (12)$$

From Eq. (1), the changes in energy when an electron tunnels from node  $i$  to  $j$  and from node  $j$  to  $i$  are:

$$\Delta E_{i \rightarrow j} = -e(V_{j=0} - V_{i=1}) + (C_S^{-1} + 2C_{T1}^{-1} + C_S^{-1})e^2/2, \quad (13)$$

$$\Delta E_{j \rightarrow i} = -e(V_{i=0} - V_{j=1}) + (C_S^{-1} + 2C_{T1}^{-1} + C_S^{-1})e^2/2. \quad (14)$$

Accordingly, the tunnel rate  $\Gamma_{j \rightarrow i}$  and  $\Gamma_{i \rightarrow j}$  can be deduced based on Eq. (1). Because  $P_{i=1,j=0} + P_{i=0,j=1} = 1$ , from Eq. (3),

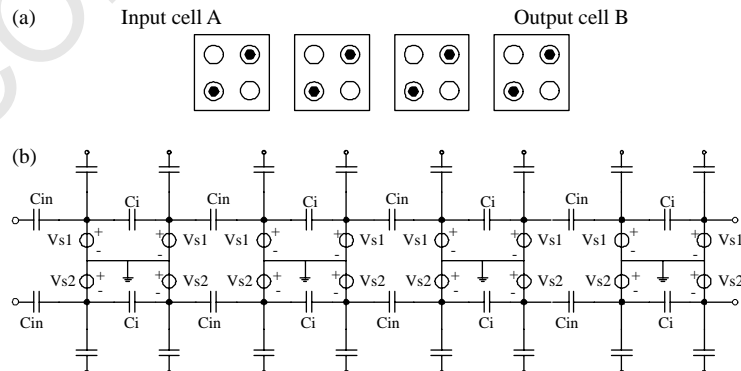


Fig. 5. QCA wire: (a) QCA wire composed of a chain of QCA cell. (b) The SPICE model of a QCA wire.

$P_{i=1,j=0}$  and  $P_{i=0,j=1}$  can be expressed as:

$$P_{i=1,j=0} = \frac{\Gamma_{j \rightarrow i}}{\Gamma_{j \rightarrow i} + \Gamma_{i \rightarrow j}}, \quad (15)$$

$$P_{i=0,j=1} = \frac{\Gamma_{i \rightarrow j}}{\Gamma_{j \rightarrow i} + \Gamma_{i \rightarrow j}}. \quad (16)$$

And the average voltages of island  $i$  and  $j$  are given by:

$$V_i = P_{i=1,j=0}V_{i=1} + P_{i=0,j=1}V_{i=0}, \quad (17)$$

$$V_j = P_{i=0,j=1}V_{j=1} + P_{i=1,j=0}V_{j=0}. \quad (18)$$

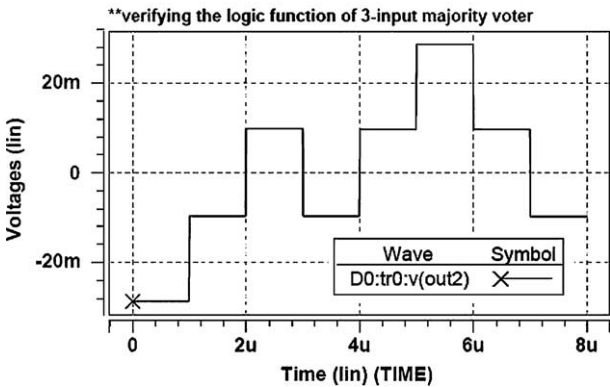
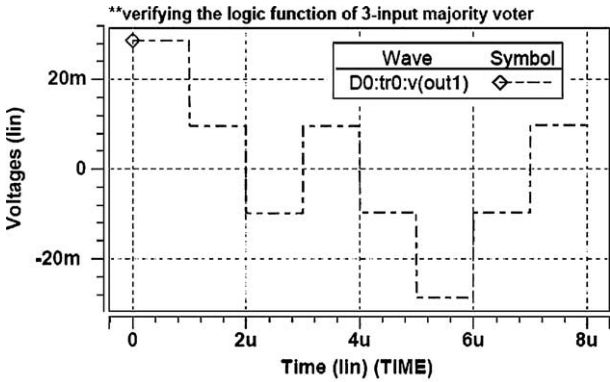
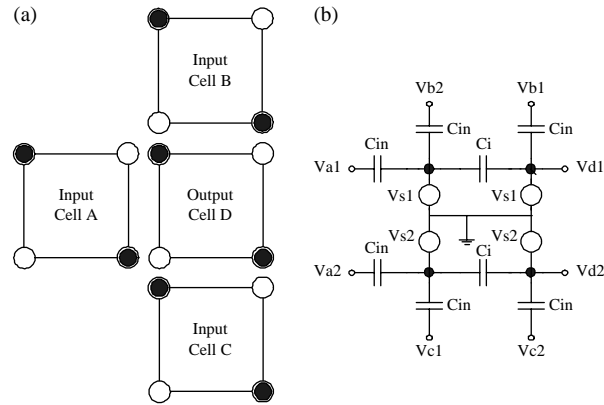


Fig. 6. The majority voting gate: (a) The majority voting gate composed of three input cells and one output cell. (b) The corresponding SPICE model of the output cell (Cell D). (c) SPICE simulation results of this majority voter, the X-axis is the time, the Y-axis of the upper figure is the node voltage of the output cell  $v(out1)$  and the Y-axis of the lower figure is the node voltage of the output cell  $v(out2)$ .

Therefore, to the next half cell, the two islands of the current half cell can be considered as two voltage controlled voltage sources  $V_{S1} = V_{S2} = (V_i - V_j)/2$  as shown in Fig. 4(a). In the figure,  $C_{in}$  is the capacitance between the QCA cells and  $C_i$  is the capacitance between two pairs of QCA dots. The node connecting two voltage sources  $V_{S1}$  and  $V_{S2}$  is grounded. Therefore, the voltage of node  $i$  equals to  $V_{S1}$  and the voltage of node  $j$  equals to  $-V_{S2}$ . As shown in Fig. 4(b), the polarizations of QCA cells correspond to the different voltages of node  $i$  and  $j$  of the right-half QCA cell. When the polarization state is '0',  $V_i$  is positive and  $V_j$  is negative; while the state is '1',  $V_i$  is negative and  $V_j$  is positive. The signs of voltage  $V_i$  and  $V_j$  are always opposite to each other. The voltages of node  $i$  and node  $j$  change from negative to positive or positive to negative depending on the polarization of QCA cells as shown in Fig. 4(b).

### 3. Basic QCA gates

On the basis of the SPICE QCA model built in Section 2, basic QCA gates or components such as QCA wire, majority voter and inverter can be built. QCA wire is composed of a chain of QCA cells as shown in Fig. 5(a). The simulation results show that the polarization of the output QCA cell changes from '1' to '0' following the polarization transition of the input QCA cell. Here, we assume the coupling process between the QCA cells has no delay. If there is any delay of the coupling process between the QCA cells,  $II$  or  $TRC$  model can be placed between the QCA cells to model the delay. Majority voter is a basic logic gate in QCA circuits as shown in Fig. 6(a). The polarization states of the cells on the top (cell B), left (cell A) and bottom (cell C) are fixed while the center cell (cell D) is free to react to the fixed charges [3]. In the actual circuits implementation, the polarization states of cell D's three neighbors are not fixed; they would be driven by other QCA cells. The values of capacitors and resistors used in SPICE simulation are obtained from [4]. The output voltage level depends on these parameters. The truth table of the majority voter is shown in Table 1. The polarization of the center QCA cell depends on the value of voltage  $V(D1)$  and  $V(D2)$  ( $V(D1) = -V(D2)$ ). If  $V(D1) > 0$ , the polarization state of this QCA cell is '0', otherwise the state of this QCA cell is '1'. So with inputs sequences shown in Table 1, the output waveform illustrated in Fig. 6(c) has the logic sequence of 00101110. The function of the majority voting logic can be expressed in terms

Table 1  
The truth table of a majority voter

A (input 1 of majority voter)	0	0	1	1	1	1	0	0
B (input 2 of majority voter)	0	0	0	0	1	1	1	1
C (input 3 of majority voter)	0	1	1	0	0	1	1	0
D (the output of majority voter)	0	0	1	0	1	1	1	0

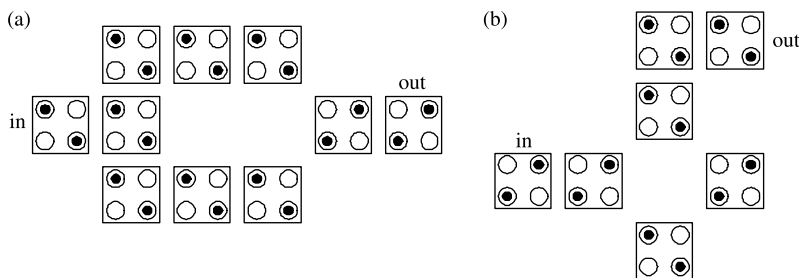


Fig. 7. The QCA inverter implementation: (a) The standard inverter implemented by QCA cells. (b) An alternative structure of QCA inverter.

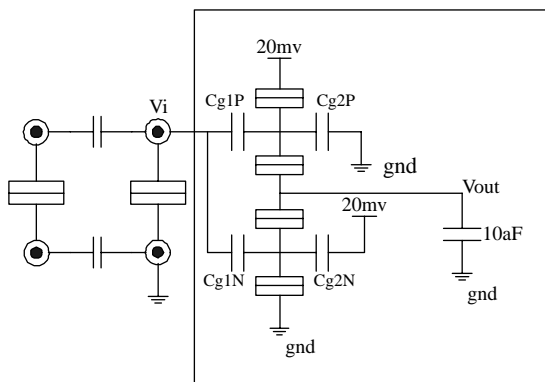


Fig. 8. The typical QCA-SET connection to measure the QCA output cell.

of fundamental Boolean operators as:

$$M(A,B,C) = AB + BC + AC. \tag{19}$$

When any one of the three inputs is fixed to one, it performs OR operation; while any one of the three inputs is fixed to zero, it performs AND operation. Using the standard QCA inverter as shown in Fig. 7(a), OR gate and AND gate, any combinational circuits can be built. There is an alternative structure of QCA inverter as shown in Fig. 7(b). This inverter structure uses fewer cells comparing with the inverter structure

shown in Fig. 7(a). These two inverter structures are useful to do the alternative layout.

#### 4. QCA and SET co-design

QCA circuits are extremely area efficient for digital circuits design. As the area of one QCA cell is  $100 \text{ nm}^2$  with  $10 \text{ nm}$  cell dimension, the total area of a QCA full-adder is around  $0.04 \text{ } \mu\text{m}^2$ . The clock period of QCA circuits is very short comparing to CMOS implementation. In the experimental

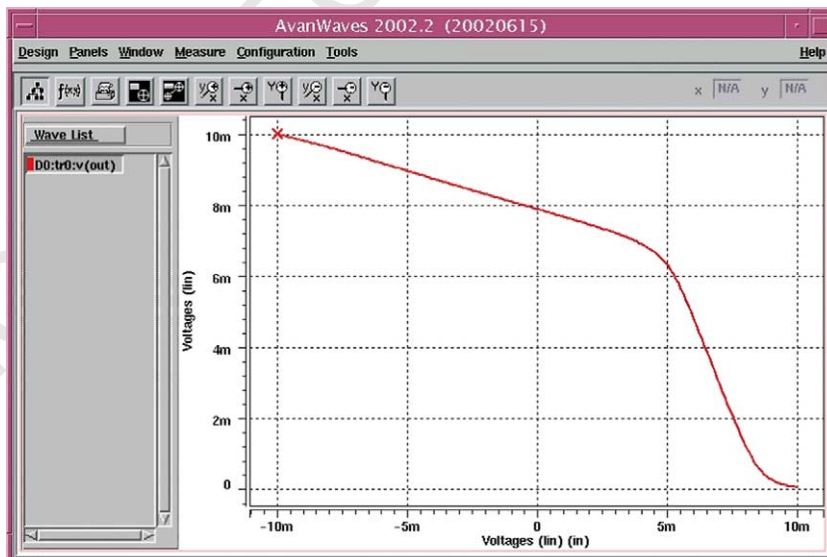


Fig. 9. The simulation result of one QCA cell driving a SET inverter: the X-axis is the node voltage of QCA cell  $V_i$ , the Y-axis is the output node voltage of the SET inverter  $V_{out}$ .

Table 2  
The parameters chosen for the SET inverter in the QCA and SET co-design simulation

$C_j$ (junction capacitance)	1 aF
$R_j$ (junction resistance)	1 M $\Omega$
$C_{g1N}$ (capacitance of gate 1 in SET N)	2 aF
$C_{g2N}$ (capacitance of gate 2 in SET N)	9.5 aF
$C_{g1P}$ (capacitance of gate 1 in SET P)	2 aF
$C_{g2P}$ (capacitance of gate 2 in SET P)	1.18 aF
$T$ (temperature)	4.2

demonstration of a QCA cell switching behavior [9], SET based electrometer is used to detect or measure the results of QCA computation-array. SET is another nano-scale technology solution. It can be realized using the same physical material as the y-dot implementation of QCA cells and it can drive capacitor loads. Therefore, using SET to measure or detect the polarization of QCA output cell is a sound idea. SPICE model of SET and the interface circuits between SET and CMOS circuits have been developed in [10,13,17]. Fig. 8 shows a typical connection method to measure the voltages of QCA output cell [16]. HSPICE is used to verify our concept of QCA-SET co-design. Both SET SPICE model and QCA SPICE model are used in this basic co-design simulation. The output QCA cell drives a SET inverter as shown in the squared area of Fig. 8 and the SET inverter is biased with 20 mV source

voltage. The SPICE simulation result as shown in Fig. 9 illustrates the fact that  $V_{out}$  follows the transition of  $V_i$ . Since the voltage of  $V_i$  indicates the polarization of the output QCA cell (the logic value of it), 9 mV can be set as the high threshold voltage for  $V_{out}$  with logic value '1' and 1 mV can be set as the low threshold voltage for  $V_{out}$  with the logic value '0'. The parameters chosen for the SET inverter are listed in Table 2.

The idea of QCA and SET co-design is amazing since QCA cell array has strong abilities to do the logic computation really fast while SET works in a similar way as the traditional CMOS circuits. Similar to QCA circuits design flow [18], a design flow of QCA-SET co-design is shown in Fig. 10, dividing the blocks into the appropriate implementations is an essential step in the flow. Generally, the digital computation blocks and memories are preferred to be implemented using QCA cells while the buses, I/O, mixed-signal parts are implemented using SETs.

## 5. Conclusions

In this paper, SPICE model for QCA cell is proposed, which is the first effort to develop SPICE macro modeling of QCA cells. This model is based on experimental demonstrations of QCA cells and the knowledge of single electron tunneling. The functions of some basic gates are verified in SPICE using the proposed model. With this model, combinational QCA circuits and hybrid circuits of SET and QCA can be built and simulated in HSPICE. The idea of QCA and SET co-design is promising since they have the same physical basis and different features. The QCA and SET co-design flow is proposed and basic SET-based readout circuits for QCA computation array is verified in HSPICE.

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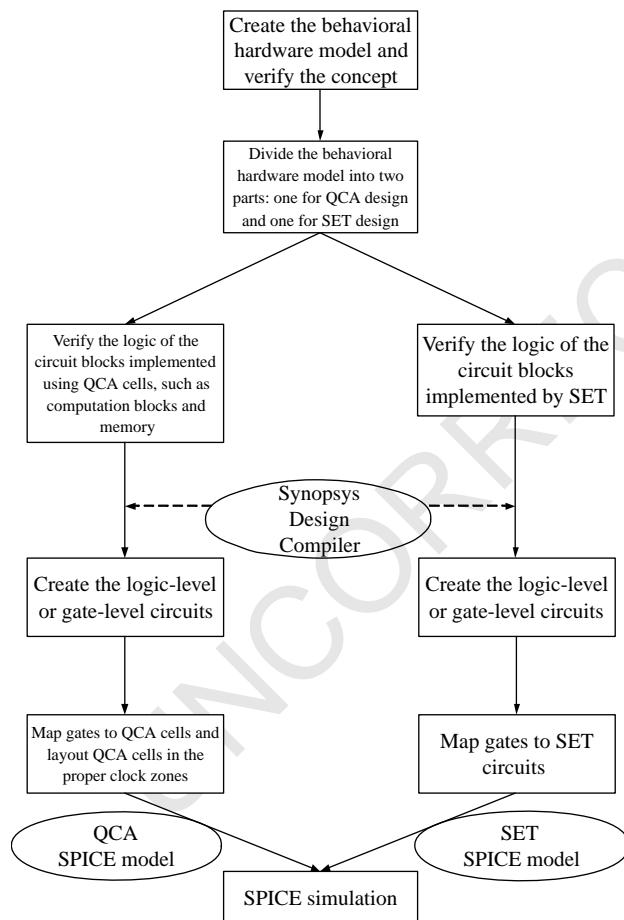
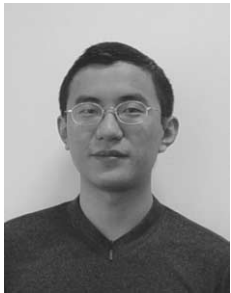


Fig. 10. QCA and SET hybrid circuits design flow.

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