Quantum-Dot Cellular Automata SPICE Macro Model

Rui Tang
Northeastern University
360 Huntington Ave
Boston, MA
rtang@ece.neu.edu

Fengming Zhang
Northeastern University
360 Huntington Ave
Boston, MA
fzhang@ece.neu.edu

Yong-Bin Kim
Northeastern University
360 Huntington Ave
Boston, MA
ybk@ece.neu.edu

ABSTRACT

This paper describes a SPICE model development methodology for Quantum-Dot Cellular Automata (QCA) cells and presents a SPICE model for QCA cells. The model is validated by simulating the basic logic gates such as inverter and majority voter. A full-adder is designed with QCA cells using the SPICE model as a test vehicle and the function is verified successfully. The proposed model makes it possible to design and simulate QCA combinational circuits and hybrid circuits of QCA and other NANO devices using SPICE.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles; I.6.5 [**Simulation and Modeling**]: Model Development

General Terms

Design

Keywords

QCA Macro Modeling

1. INTRODUCTION

Since CMOS technology is approaching its physical limitation below 65nm, it is extremely difficult to maintain the current trend of feature size scaling down. Novel materials and technologies have been extensively researched or developed at nano-scale to replace conventional VLSI technology. Among them, QCA plays an important role. The feature size of the basic QCA cell can achieve few nanometers by molecular implementation at room temperature[2]. In an abstract way, a basic QCA cell can be considered consisting of four quantum dots located at the four corners of a square array and coupled by tunnel barriers. Electrons can travel between the adjacent corners by tunnelling through the barriers in a cell, but can't leave it. If there are two extra electrons bounded in a cell, they must be forced to locate on the opposite corners of the cell due to Coulomb repulsion in ground states. Consequently, these two ground states can be used to represent logic "0" and "1" as shown in Fig 1(a).

Based on basic QCA cells, [3] [5] [7] have demonstrated and designed QCA majority voter, inverter, and more complicated circuits such as 12-bit microprocessor. CAD tools for QCA circuits design are essential for real application and further research. QCADesigner is a QCA layout and simulation tool developed by ATIPS laboratory [1]. This software can be used to draw QCA layout with basic cells and do logic simulation, however, it uses a bottom-up design methodology which is not efficient for large circuits design. Furthermore, it is not compatible with the traditional CMOS design software, therefore it is unsuitable for QCA and CMOS or other NANO technology co-design. In this paper, a method to develop SPICE model of QCA cells is presented. This model facilitates circuit designers to achieve very accurate simulations on QCA circuits.

2. SPICE MODEL OF QCA CELL

Our SPICE model is based on the experimental verification on the behavior of QCA cells[4][5]. As shown in Fig 1(b), a possible realization of basic QCA cell consists of two series-connected metal dots separated by tunnelling barriers and capacitively coupled to the second pair of identical double dots based on existing technology[4]. Since the left half part and the right half part of a QCA cell are exactly symmetrical, the model for the half-QCA cell is built first, and then two of them can be combined together to develop the whole QCA cell model. The schematic diagram of the simplified half-QCA cell is shown in Fig 1(c). The two black dots represent two quantum dots and T1 is a tunnel junction. Electrons are able to tunnel between the islands through the tunnel junction T1 but can't leave these two islands.

The electrostatic energy to move an electron from one island i to another island j is given by [8]:

$$\Delta E = -e(v_j - v_i) + (C_{ii}^{-1} - 2C_{ij}^{-1} + C_{jj}^{-1})e^2/2, \quad (1)$$

where C_{jj} is the total capacitance of island j, C_{ii} is the total capacitance of island i, C_{ij} is the negative capacitance between the island i and j, v_i and v_j are the voltages on island i and j before the electron has tunnelled from node i to node j. If one island contains k extra electrons, the state transition process is a birth-and-death Markov chain. The

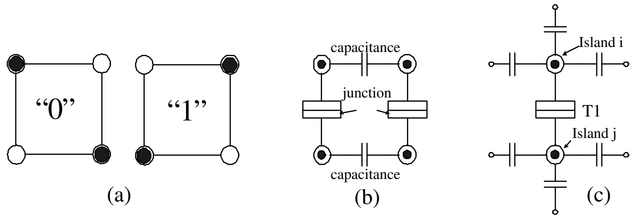

Figure 1: (a)Two ground-state polarizations of basic four-dot QCA cell (b)Two-junction realization of the quantum cellular automata (c)A schematic diagram of the half-QCA cell

probability that one island holds k electrons, p_k, is given by $p_k = p_{k-1}\frac{\lambda_{k-1}}{\mu_k}$, where λ_k and μ_k are transistion rates from one state to another state. In a simple case, there is only one extra electron in one pair of quantum dots. Therefore, only two states of the transition exist, one state is the extra electron trapped in island i and the other state is island j holding the extra electron. Therefore, the following expression is obtained:

$$P_{i=1,j=0}\Gamma_{i\to j} = P_{i=0,j=1}\Gamma_{j\to i}, \tag{2}$$

where $\Gamma_{j\to i}$ is the tunnel rate for an electron tunnelling from island j to island i. $P_{i=a,j=b}$ represents the probability that node i holds a electrons while node j has b electrons(a, b can be either 0 or 1). The tunnel rate is formulated based on the orthodox theory and given by [8]:

$$\Gamma(\Delta E) = \frac{\Delta E}{e^2 R_T(\mathrm{e}^{\Delta E/k_B T} - 1)}, \tag{3}$$

where R_T is the tunnel resistance, k_B is Boltzmann's constant, T is temperature, and ΔE is the energy difference calculated from Equation 1. There can be one to three voltage sources connected to each island depending on the placement of other QCA cells around this QCA cell, and C_{im}(m from 1 to 3) is the corresponding input capacitance for each input with voltage source V_{im} of island i. For the particular model shown in Fig 1, the following equations are obtained using the simple electrostatics:

$$V_{i=1} = \frac{\Sigma_m V_{im}C_{im} + V_{j=0}C_{T1} - e}{C_S} \tag{4}$$

$$V_{i=0} = \frac{\Sigma_m V_{im}C_{im} + V_{j=1}C_{T1}}{C_S} \tag{5}$$

$$V_{j=1} = \frac{\Sigma_m V_{jm}C_{jm} + V_{i=0}C_{T1} - e}{C_S} \tag{6}$$

$$V_{j=0} = \frac{\Sigma_m V_{jm}C_{jm} + V_{i=1}C_{T1}}{C_S}. \tag{7}$$

Solving the above four equations, the following equations are obtained:

$$V_{i=1} = \frac{(\Sigma V_{im}C_{im} - e)C_S + (\Sigma V_{jm}C_{jm})C_{T1}}{C_S^2 - C_{T1}^2} \tag{8}$$

$$V_{j=0} = \frac{(\Sigma V_{im}C_{im} - e)C_{T1} + (\Sigma V_{jm}C_{jm})C_S}{C_S^2 - C_{T1}^2} \tag{9}$$

$$V_{i=0} = \frac{(\Sigma V_{im}C_{im})C_S + (\Sigma V_{jm}C_{jm} - e)C_{T1}}{C_S^2 - C_{T1}^2} \tag{10}$$

$$V_{j=1} = \frac{(\Sigma V_{im}C_{im})C_{T1} + (\Sigma V_{jm}C_{jm} - e)C_S}{C_S^2 - C_{T1}^2}, \tag{11}$$

where $V_{i=1}$ is the voltage of node i with the extra electron and $V_{i=0}$ is the voltage of node i with no extra electron. C_S is the total capacitance of node i and j. It is assumed that the total capacitances of island i and j are the same. C_{T1} is the capacitance of tunnel junction $T1$. According to Equation 1, the change in energy when an electron tunnels from node i to j is given by

$$\Delta E_{i\to j} = -e(V_{j=0} - V_{i=1}) + (C_S^{-1} + 2C_{T1}^{-1} + C_S^{-1})e^2/2. \tag{12}$$

Similarly, the change in energy when an electron tunnels from node j to i is

$$\Delta E_{j\to i} = -e(V_{i=0} - V_{j=1}) + (C_S^{-1} + 2C_{T1}^{-1} + C_S^{-1})e^2/2. \tag{13}$$

Now, the tunnel rate $\Gamma_{j\to i}$ and $\Gamma_{i\to j}$ can be calculated. Because $P_{i=1,j=0} + P_{i=0,j=1} = 1$, the value of $P_{i=1,j=0}$ and $P_{i=0,j=1}$ are obtained as following:

$$P_{i=1,j=0} = \frac{\Gamma_{j\to i}}{\Gamma_{j\to i} + \Gamma_{i\to j}} \tag{14}$$

$$P_{i=0,j=1} = \frac{\Gamma_{i\to j}}{\Gamma_{j\to i} + \Gamma_{i\to j}}, \tag{15}$$

and the average voltages of island i and j are given by

$$V_i = P_{i=1,j=0}V_{i=1} + P_{i=0,j=1}V_{i=0} \tag{16}$$

$$V_j = P_{i=0,j=1}V_{j=1} + P_{i=1,j=0}V_{j=0}. \tag{17}$$

Therefore, two voltage sources $V_{S1} = V_{S2} = (V_i - V_j)/2$ are used with the internal resistance R_{T1} to replace the tunnel junction in SPICE macro model as shown in Fig 2(a). In

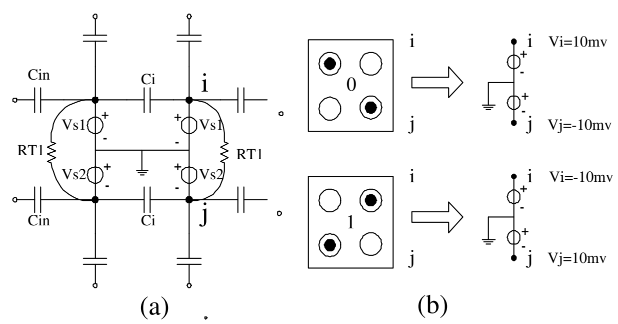

Figure 2: (a)The SPICE model of QCA cell (b)The voltage sources corresponding to the polarizations of input QCA cells

the figure, C_{in} is the capacitance between the QCA cells and C_i is the capacitance between two pairs of QCA dots. The node connecting two voltage sources V_{S1} and V_{S2} is grounded. Therefore, the voltage of node i equals to V_{S1} and the voltage of node j equals to $-V_{S2}$. As shown in Fig 2(b), the polarizations of QCA cells correspond to the different voltages of node i and j. When the polarization state is "0", V_i is positive and V_j is negative; while the state is "1", V_i is negative and V_j is positive. The signs of voltage V_i and V_j are always opposite to each other. The voltages of node i and node j change from negative to positive or positive to negative depending on the polarization of QCA cells as shown in Fig 2(b).

3. BASIC QCA GATES

Basic QCA gates or components such as QCA wire, majority voter and inverter can be built based on the SPICE

QCA model built in the previous section. QCA wire is com-

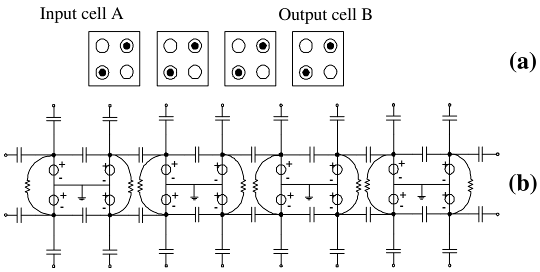

Figure 3: QCA wire:(a)QCA wire composed of a chain of QCA cell (b)The SPICE model of a QCA wire

posed of a chain of QCA cells as shown in Fig 3(a). The polarization of the output QCA cell changes from "1" to "0" following the polarization transition of the input QCA cell. That is, the signal can transmit through a QCA wire. Majority voter is a basic logic gate in QCA circuits as shown in Fig 4(a). The polarization states of the cells on the top (cell B), left (cell A) and bottom (cell C) are fixed while the center cell (cell D) is free to react to the fixed charges[7]. In the actual circuits implementation, the polarization states of cell D's three neighbors would not be fixed; they would be driven by other QCA cells. The output waveform is shown in Fig 4(c) with the logic sequence of 00101110. The polarization of the center QCA cell depends on the value of voltage $V(D1)$ and $V(D2)$ ($V(D1) = -V(D2)$). If $V(D1) > 0$, the polarization state of this QCA cell is "0", otherwise the state of this QCA cell is "1". The function of the majority voting logic can be expressed in terms of fundamental Boolean operators as:

$$M(A, B, C) = AB + BC + AC. \tag{18}$$

When any one of the three inputs is fixed to one, it performs OR operation; while any one of the three inputs is fixed to zero, it performs AND operation. Using the standard QCA inverter as shown in Fig 5(a), OR gate and AND gate, any combinational circuits can be built. There is an alternative structure of QCA inverter as shown in Fig 5(b). This inverter structure uses less cells comparing with the inverter structure shown in Fig 5(a). However this structure will complicate the layout of QCA circuits.

4. QCA CIRCUITS DESIGN

Using the basic QCA cells verified in last section, any combinational QCA circuits can be designed. However, even for a small circuit like full adder, we have to set four-clock zones to make it work correctly. There are four clock phases of the QCA cells [3]: *switch phase*, *hold phase*, *release phase*, *relax phase*. During the *switch phase*, the inter-dot potential barriers are raised from low to high and the QCA cells become polarized according to the state of their driver. During the *hold phase*, the barriers are held high enough to suppress any electron tunneling, and the states of QCA cells are fixed. In the *release phase*, barriers switch from high to low and cells relax to an unpolarized state. During the *relax phase*, cell barriers remain low and QCA cells keep in the unpolarized state[6]. Therefore, the circuit can be divided into several clocking zones and all of the cells within a clocking zone are

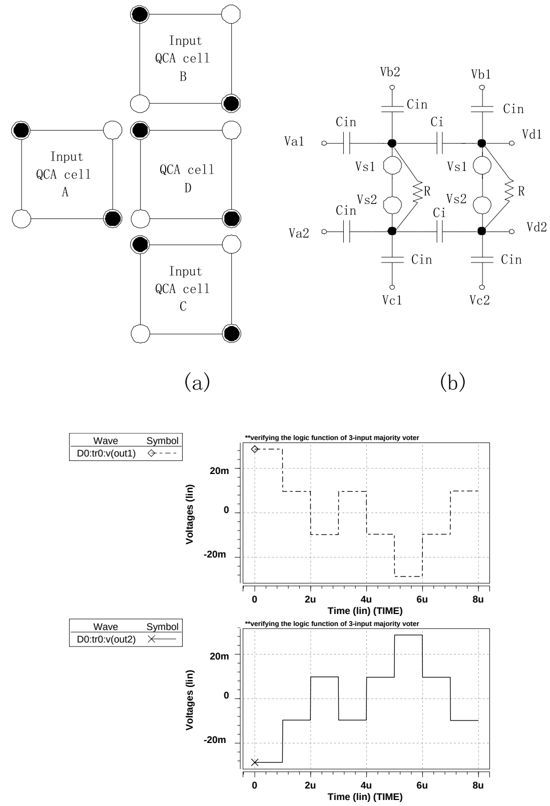

Figure 4: The majority voting gate: (a) The majority voting logic cell, (b) Corresponding SPICE model and the figure below (a) and (b) shows SPICE simulation results (the X-axis is time and the Y-axis is voltage of the output cell v(out))

in the same phase at the same time. "Signal" can be passed from one clock zone to an adjacent clock zone with a phase shift of 45 degrees. Consequently, the clock frequency determines the delay of the whole circuit and pipelining can be easily implemented. A QCA full-adder is designed to test and verify our SPICE model. Using the majority function, the QCA addition algorithm is obtained as following [9]:

$$\begin{aligned} C_{out} &= MV(a, b, c_{in}) \\ \overline{C_{out}} &= \overline{MV(a, b, c_{in})} \\ S &= MV(\overline{c_{out}}, c_{in}, MV(a, b, \overline{c_{in}})), \end{aligned}$$

where $MV(a, b, c)$ stands for majority voting of signal a, b, c. Based on this algorithm, one-bit QCA full-adder can be implemented using three majority gates and two inverters as illustrated in Fig 6. The alternative inverter structure as shown in Fig 5(a) is used to design the full-adder.

Fig 7 shows the QCA adder layout Both QCADesigner and HSPICE are used to verify the function. Fig 8 illustrates the simulated waveforms. The results from QCADesigner and HSPICE are similar, however the waveforms from QCADesigner shows the polarization of the output QCA cells while the outputs of HSPICE show the actual voltages of the output QCA cells. In HSPICE simulation results, $V > 0$ means that the polarization of the output cell is "0" while $V < 0$ means the state of the QCA cell is "1". Therefore, as shown in Fig 8, the results of *sum* are in the logic

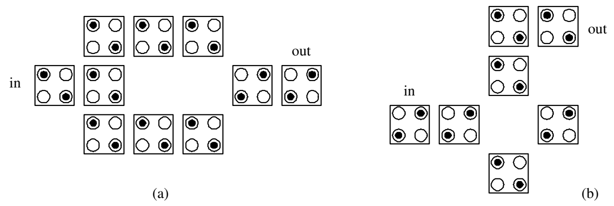

Figure 5: The Inverter: (a) The standard inverter implementation made by QCA cells (b) An alternative structure of QCA inverter

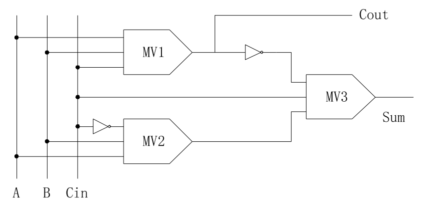

Figure 6: One-bit QCA full-adder

sequence of 01101001 and the results of C_{out} are in the logic sequence of 00010111.

5. CONCLUSIONS

In this paper, SPICE model for QCA cell is proposed, which is the first effort to develop macro SPICE modelling of QCA cells. This model is based on experimental demonstrations of QCA cells and the knowledge of single electron tunnelling. The functions of full-adder and majority voter are verified in SPICE using the proposed model. This model makes it possible to build combinational QCA circuits using HSPICE and to verify their functions, which enables designers to develop top-down design process of QCA digital circuits similar to the traditional CMOS design flow.

6. REFERENCES

[1] http://www.atips.ca/projects/qcadesigner.

[2] C. S. Lent and B. Isaksen. Clocked molecular quantumn-dot cellular automata. *IEEE Transaction On Electron Devices*, 50(9):1890 – 1896, September 2003.

[3] M. T. Niemier and P. M. Kogge. Logic in wire: Using quantum dots to implement a microprocessor. In *Proc. of the International Conference of Electronics, Circuits, and Systems*. Cyprus, September 1999.

[4] A. O. Orlov, I. Amlani, and G. H. Bernstein. Realization of a functional cell for quantum-dot cellular automata. *Science*, 277(9), August 1997.

[5] A. O. Orlov, I. Amlani, and G. Toth. Experimental demonstration of a binary wire for quantum-dot cellular automata. *Applied Physics Letters*, 74(19), May 1999.

[6] C. S.Lent and P. Tougaw. A device architecture for computing with quantum dots. In *Proceedings of IEEE*, volume 85, pages 541–557, April 1997.

[7] P. D. Tougaw and C. S. Lent. Logical devices implemented using quantum cellular automata. *Journal of Applied Physics*, 75(3), February 1994.

[8] C. Wasshuber. *Computational Single-Electronics*. SpringerWienNewYork, Springer-Verlag Wien New York, 2001.

[9] K. W. Wei Wang and G. Jullien. Quantum-dot cellular automata addesr. *Nanotechnology*, 1(12-14):461–464, August 2003.

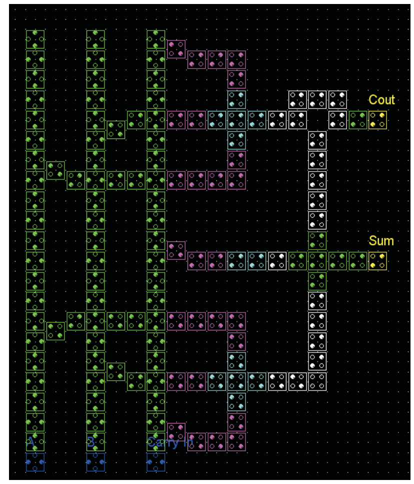

Figure 7: Layout of the one-bit QCA adder

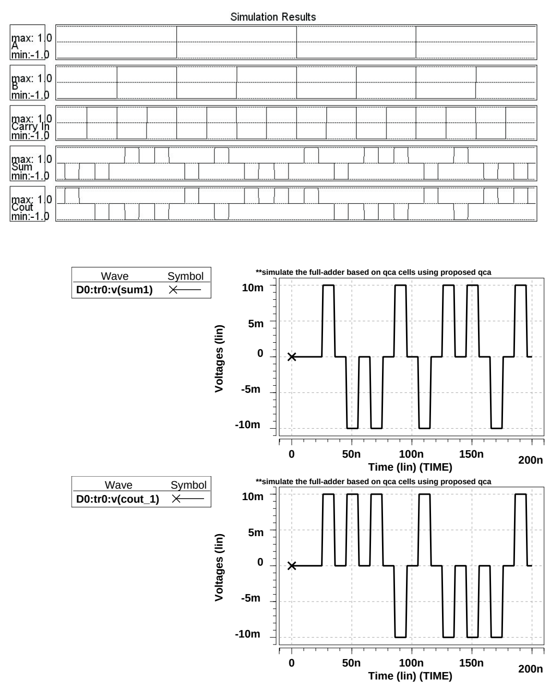

Figure 8: The Simulation Results: the top waveforms are from QCADesigner, the bottom figures are from HSPICE