

An Accurate Timing Model for Nano CMOS Circuit Considering Statistical Process Variation

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Abstract— Process variation has more significant impact on circuit performance as technology develops to nano scale. It is therefore necessary to evaluate chip performance using statistical timing analysis rather than deterministic static timing analysis. This paper first evaluates the impact of single extrinsic fluctuation on circuit performance based on the rigorously derived propagation delay model. The parameter fluctuations are characterized and a novel statistical approach is developed to evaluate the effect of simultaneous variations in multiple process parameters. The probability distribution of propagation delay is calculated and timing yield is estimated.

I. INTRODUCTION

As technology continues to scale, process variation has more significant impact on circuit performance. Small dimension devices operating at low supply voltages show an increased sensitivity to parameter variations. It is therefore desirable to characterize and control the parameter fluctuations to improve the performance and yield of integrated circuits.

Parameter fluctuations could be classified to be two categories, intra-die parameter variations and global parameter variations [1]. Some researchers also define the fluctuations as systematic variations and random variations. Intra-die or systematic variations are caused by process gradients over the wafer during manufacturing. These variations are independent of device size, and cause same deviation on each device on same chip. Global or random parameter variations could be divided into two types, extrinsic variations and intrinsic variations. Fluctuations of effective channel length, doping concentrations and oxide thickness caused by extrinsic equipment are considered to be extrinsic variations. The intrinsic variations are due to random fluctuations in channel dopant number, oxide charge, interface charge, etc.

The traditional ‘corner-based’ deterministic static timing analysis will lead to pessimistic results because it assumes worst case for all the devices on a die and consider them to have same variation features. The International Technology Roadmap for Semiconductors has identified a clear demand for statistical timing analysis, which models process

variations by probabilistic distributions and reduces the excessive conservatism.

A number of methods on statistical timing analysis have been presented. Intrinsic fluctuations in threshold voltage, subthreshold swing, saturation drain current and subthreshold leakage due to random placement of dopant atoms in channel are examined in [2]. However, the variations’ impact on delay was not estimated. [1] and [3] assume the propagation delay of each gate to be Gaussian distributed function and the density function of the critical path is calculated. But the random parameter variations are excluded in analytical analysis. The effects are simulated and modeled using look-up table in [4].

In this paper, we will first evaluate the parameter variations’ impact on propagation delay based on a rigorously derived propagation delay model. Parameter standard deviation ranging from 5% to 10% is estimated for the delay model. Then parameter variations are characterized for general delay model, probability density function of propagation delay is calculated by integrating the joint pdf considering all the parameters to change simultaneously. Timing yield is derived by integrating the pdf of propagation delay in a continuous integration range. Our work provides a novel analytical statistical estimation on path delay accounting the simultaneously changed extrinsic and intrinsic parameter variations.

This paper is organized as follows: in Section II we describe the rigorously derived propagation delay model. Section III presents the simulated results for parameter fluctuations on the model described in Section II. Section IV derives the analytical expression of probability density for general propagation delay considering all the parameter variations to change simultaneously. Timing yield is also calculated. Section V concludes the work.

II. PROPAGATION DELAY MODEL

An accurate propagation delay model for CMOS inverters is presented in [5]. This model is derived by solving the non-homogeneous linear differential equation of the inverter. Output transient response expressions are derived for each operation region of inverter during input transition. Propagation delay is calculated by taking the time

difference of the 50% transition points of the input and output waveforms. The delay expression is given as follows:

$$tpHL = \frac{tr}{Kz} \cdot \log\left(\frac{C34}{\frac{1}{\lambda_n} - \frac{V_{DD}}{2}}\right) - \frac{tr}{2} \quad (1)$$

Where $C34 = [cr \cdot V_{DD} \cdot (1 + \frac{K_y \cdot (1 - v_{thn})^{\alpha n + 2}}{\alpha_n + 2}) + \frac{1}{\lambda_n} - cr \cdot V_{DD} \cdot v_{thn}] \cdot \exp[K_z - K_y \cdot (1 - v_{thn})^{\alpha n + 1}]$,

$$K_y = \frac{\beta_{sn} \cdot tr \cdot \lambda_n}{(C_L + C_M) \cdot (\alpha_n + 1)}, K_z = \frac{\beta_{sn} \cdot tr \cdot \lambda_n}{C_L + C_M} \cdot (1 - v_{thn})^{\alpha n}$$

tr is the rise time of the input signal, λ_n is the channel length modulation factor, V_{DD} is the power supply voltage, v_{thn} is the normalized threshold voltage, αn represents the velocity saturation index, and C_L represents the load capacitance. C_M is the gate to drain coupling capacitance, which is proportional to the area of the inverter and reverse proportional to the oxide thickness T_{OX} . $\beta_{sn} = I_{D0} / (1 - v_{thn})^{\alpha n}$, where I_{D0} is the process related factor, which is proportional to the width over length ratio of a MOSFET.

Table I shows the values of the NMOS parameters used in model for different technologies.

III. IMPACT OF SINLE PARAMETER FLUCTUATION

The extrinsic fluctuations of channel length (L), channel width (W), and threshold voltage after accounting intrinsic fluctuations [2] are assumed to follow uncorrelated Gaussian (Normal) distributions for the NMOS and PMOS in each gate. Their probability density function (pdf) could be expressed as:

$$f_x(x) = \frac{e^{-(x-m)^2 / 2\sigma^2}}{\sqrt{2\pi}\sigma} \quad (2)$$

Where m is the mean and σ is the standard deviation of X. Gaussian pdf is a “bell-shaped” curve centered and symmetric about m and whose “width” increases with σ . The propagation delay model described in section II is simulated in both 65nm and 90nm technology, with $Wn/Ln=3$ and 50fF load capacitance. Input transition time is set to be 450ps, the width of PMOS is kept being equal to $2Wn$.

Figure 1 shows the simulated delay variation with respect

to the variation of gate width. The width of the gate is assumed to follow Gaussian distribution with mean value equal to $2 \cdot Ln$, and $\sigma_w / W = 5\%$. Both the simulated and fitted curves are shown. The mean of the propagation delay in 65nm process is measured to be 247.56ps, and the standard deviation is measured to be 8.716ps, which is 3.52% of the mean value. The mean of the propagation delay in 90nm process is measured to be 230.209ps, and the standard deviation is measured to be 7.769ps, which is 3.37% of the mean value.

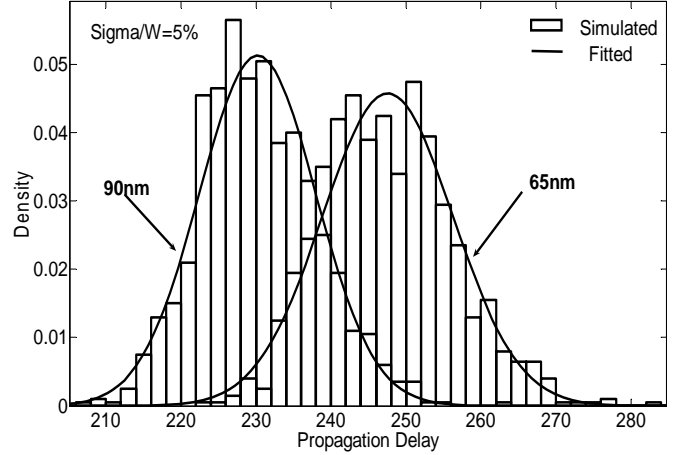


Fig. 1 Delay Distribution vs. Gate Width Variation

Figure 2 illustrates the simulated delay variation with respect to the variation of threshold voltage. The threshold voltage of MOSFET is assumed to follow Gaussian distribution with mean value equal to the value given in Table I, and $\sigma_{v_{th}} / V_{th} = 5\%$. The mean of the propagation delay in 65nm process is measured to be 247.354ps, and the standard deviation is measured to be 1.814ps, which is 0.7% of the mean value. The mean of the propagation delay in 90nm process is measured to be 229.74ps, and the standard deviation is measured to be 2.087ps, which is 0.9% of the mean value.

We could conclude that for the delay model described in section II, propagation delay distribution could be approximated to be Gaussian distributed functions when one of the process parameters follows the Gaussian distribution. We also observe that geometric parameter fluctuations have more significant impact on the propagation delay compared to the threshold voltage fluctuations. The standard deviations of both width and threshold voltage were set to be 5% of their normal value in simulation, the deviation of delay is above 3% in Figure 1 while within 1% in Figure 2. Also short channel devices are more sensitive to geometric parameter fluctuations compared to the ones with relatively

Process	W(um)	Id0(uA)	α	Vth(V)	Vdd(V)	λ (1/V)	Tox(nm)
0.13um	0.26	149.07	1.3366	0.332	1.3	0.0713	1.6
90nm	0.18	133.58	1.2479	0.2607	1.2	0.12	1.4
65nm	0.13	113.89	1.4622	0.22	1.1	0.167	1.2

Table I: NMOS Parameters in Propagation Delay Model

longer channel length.

Similar simulation could be run for other process parameters such as channel length, gate oxide thickness, doping profiles etc. Look-up table could be built according to the simulated results for future delay distribution estimation.

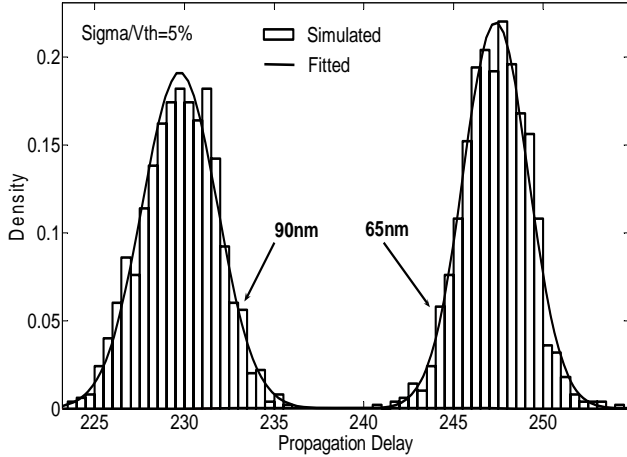


Fig. 2 Delay Distribution vs. Threshold Voltage Variation

IV. IMPACT OF SIMULTANEOUS FLUCTUATIONS

The impact of process variations for propagation delay model in [5] have been presented in section II. In this section, we will discuss how to estimate the impact of parameter fluctuations on general delay model. Both single parameter fluctuation and simultaneous parameter fluctuations cases will be presented.

The following equation is widely used in delay approximation for static CMOS gates:

$$delay \propto \frac{C_{load} V_{DD}}{\mu C_{ox} (W/L) (V_{DD} - V_{th})^\alpha}, \text{ where } \mu \text{ is the mobility,}$$

V_{th} is the threshold voltage, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the gate capacitance

per unit area, W and L are the transistor dimensions, and α is the velocity saturation index. We could rewrite the delay

$$\text{expression as } delay \propto \frac{C_{load} \cdot V_{DD} \cdot L \cdot T_{ox}}{\mu \epsilon_{ox} W (V_{DD} - V_{th})^\alpha} \text{ for the}$$

convenience of future statistical analysis. Each individual process parameter in the expression is assumed to follow independent Gaussian distribution with mean m and standard deviation σ .

If only one of the parameters in the numerator fluctuates, for example, only channel length L fluctuates following Gaussian distribution with mean value m_L and standard deviation σ_L , the propagation delay will also follow Gaussian distribution with mean value equal

to $\frac{C_{load} \cdot V_{DD} \cdot T_{ox}}{\mu \epsilon_{ox} W (V_{DD} - V_{th})^\alpha} \cdot m_L$ and standard deviation equal

$$\text{to } \frac{C_{load} \cdot V_{DD} \cdot T_{ox}}{\mu \epsilon_{ox} W (V_{DD} - V_{th})^\alpha} \cdot \sigma_L.$$

If only one of the parameters in the denominator fluctuates, the distribution function of propagation delay could be calculated to be the addition of scaled Gamma distribution, Reyleigh distribution and Gaussian distribution. The shape of the delay distribution depends on the deviation of transistor width W . However, for today's manufacturing process, the deviation of W is usually controlled to be within 5% to 10%, which will lead the probability density function of propagation delay to be dominated by Gaussian distribution. The mean of delay is

$$\text{approximately } \frac{C_{load} \cdot V_{DD} \cdot T_{ox}}{\mu \epsilon_{ox} W (V_{DD} - V_{th})^\alpha} \cdot \frac{1}{m_W}, \text{ the standard}$$

deviation of delay σ_{delay} equals $m_{delay} \cdot \frac{\sigma_W}{m_W}$. Figure 3 shows

the simulated delay variation with respect to the variation of gate width. σ_W / m_W is set to be 10%, and the simulated $\sigma_{delay} / m_{delay}$ is 10% for both 65nm and 90nm process, which validates the above conclusion.

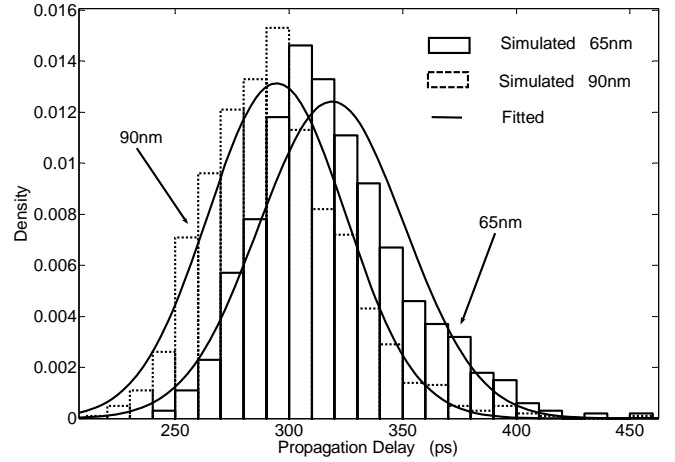


Fig. 3 Delay Distribution for General Delay Model

When all the process parameters are changing simultaneously, assume all these parameters are following independent Gaussian distribution, the joint probability density function of W, L, T_{ox}, V_{th} could be expressed as:

$$f_{W,L,T_{ox},V_{th}} = f_W \cdot f_L \cdot f_{T_{ox}} \cdot f_{V_{th}}, \text{ which is joint Gaussian.}$$

Let $z1 = delay = K \cdot \frac{L \cdot T_{ox}}{W \cdot V^\alpha}$, where $K = \frac{C_{load} V_{DD}}{\mu \epsilon_{ox}}$ is a constant,

and V is a Gaussian random variable with $m_V = V_{DD} - m_{V_{th}}$,

$$\sigma_V = \sigma_{V_{th}}. \text{ Also define } h1 = \frac{z1}{K} \cdot \frac{W \cdot V^\alpha}{T_{ox}}, \text{ } h3 = z3 = W,$$

$h4 = z4 = V$, the Jacobian of the reverse transformation is given by

$$J(z1, z2, z3, z4) = \det \begin{bmatrix} \frac{\partial h1}{\partial z1} & \frac{\partial h1}{\partial z2} & \frac{\partial h1}{\partial z3} & \frac{\partial h1}{\partial z4} \\ \frac{\partial h2}{\partial z1} & \frac{\partial h2}{\partial z2} & \frac{\partial h2}{\partial z3} & \frac{\partial h2}{\partial z4} \\ \frac{\partial h3}{\partial z1} & \frac{\partial h3}{\partial z2} & \frac{\partial h3}{\partial z3} & \frac{\partial h3}{\partial z4} \\ \frac{\partial h4}{\partial z1} & \frac{\partial h4}{\partial z2} & \frac{\partial h4}{\partial z3} & \frac{\partial h4}{\partial z4} \end{bmatrix} \quad (3)$$

$$= \det \begin{bmatrix} WV^\alpha & z1 \cdot W \cdot V^\alpha & z1 \cdot V^\alpha & \alpha z1 \cdot V^{\alpha-1} \\ KT_{ox} & K \cdot T_{ox}^2 & K \cdot T_{ox} & KT_{ox} \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

The joint pdf of $z1, z2, z3, z4$ could be expressed as the joint pdf of W, L, T_{ox}, V_{th} times the Jacobian of the reverse transformation:

$$f_{z1, z2, z3, z4} = f_{W, L, T_{ox}, V_{th}}(h1, h2, h3, h4) \cdot |J(z1, z2, z3, z4)| \quad (4)$$

The probability density function of propagation delay of a single gate could be calculated by integrating the joint pdf

$$f_{z1, z2, z3, z4}: f_{delay} = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} f_{z1, z2, z3, z4} dz2 dz3 dz4 \quad (5)$$

When the single gate delay model is expanded to a critical path consisting n gates, if the single gate delay is calculated to follow Gaussian distribution, the propagation delay of the critical path will also follow Gaussian distribution with mean value equal to the sum of the mean delay of each gate, which is $m_{path} = m_{gate1} + m_{gate2} + \dots + m_{gaten}$. The standard deviation of the critical path is given by $\sigma_{path} = \sqrt{\sigma_{gate1}^2 + \sigma_{gate2}^2 + \dots + \sigma_{gaten}^2}$, where σ_{gaten} stands for the standard deviation of each gate on the critical path.

The probability density function of critical path could be

$$\text{expressed as: } f_{path}(x) = \frac{e^{-(x-m_{path})^2 / 2\sigma_{path}^2}}{\sqrt{2\pi}\sigma_{path}} \quad (6)$$

The yield of the chip could be given by integrating the pdf of the path over a certain delay range, which is usually the period of the clock in synchronous circuit design.

$$\text{Yield} = \int_{-\infty}^{T_{CLK}} f_{path}(x) dx \quad (7)$$

An obvious method to improve the yield is to increase the period of the clock. However, this option lowers the clock frequency of the chip, which is not desired in today's high speed circuit design. Another option to improve the yield is to lower the mean value of the propagation delay

distribution. This way will shift the pdf of the propagation delay towards the origin, which increases the cumulative distribution function value given a certain integral up limit. The reduction of the mean delay could be achieved by increasing the power supply voltage or the sizes of gates, which is sacrificing the power dissipation and area of the chip. The yield could be further improved by decreasing the standard deviation of the delay distribution, which will result in a taller and narrower bell curve. The yield could be understood as the area under the delay probability density function up to clock period in integration; this method will also increase the "area" of the integration given a certain clock frequency. From the analysis above, the standard deviation of the propagation delay is usually related to the standard deviation of the manufacturing parameters, such as the dimension and threshold voltage of the transistors. So it's important to have accurate control over the parameter fluctuations in manufacturing in order to improve the yield.

V. CONCLUSION

Process variations have become a critical issue in today's high performance circuit design as technology keeps scaling down. In this work, we have presented the impact of process variations on path delays. The impact of parameter fluctuations is evaluated for both a rigorously derived delay model and general propagation delay model. Simulation results are shown for both 65nm and 90nm technology.

A novel statistical approach is developed to evaluate the effect of simultaneous variations in multiple process parameters by computing the delay probability density function from finding the Jacobian determinant of the combined parameter matrix. Several options to improve the chip yield are analyzed based on this new statistical approach. Our work allows circuit-designers to predict the worst case circuit delay under the influence of process variations before chip fabrication.

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