

# A Power Optimization Method to Design Butterworth Filter on SiGe Process

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**Abstract**—A novel approach to design operational amplifier with large unit gain bandwidth (UGBW) and high phase margin (PM) is proposed that focuses on minimizing power dissipation. After poles and zeros are determined according to the specifications of UGBW and PM, the design formulations can be significantly simplified for power optimization. The design of an operational amplifier on  $0.18\mu\text{m}$  SiGe BiCMOS process is presented as an example. An dual mode low pass filter for wide-band and GSM is implemented based on this op-amp.

## I. INTRODUCTION

The dual mode transmit path is one of the most important blocks in today's wide-band wireless chips. It usually consists of two channels for both I (in-phase) and Q (quadrature) data modulation. In each channel, a parallel digital input stream is converted into a differential analog signal, filtered, and amplified. Therefore, the standard transmit path includes a digital to analog converter (DAC), a filter, and a programmable gain amplifier. Silicon Germanium (SiGe) BiCMOS technology is being developed very fast recently[3]. It has been widely used in high-performance and low-power wireless communication products as well as high-speed/high-capacity network applications. Combining the cost benefits of standard CMOS process with the speed of more profound and expensive technologies, such as Gallium Arsenide (GaAs), SiGe is ideal for communications and wireless networking designs[1]. In this paper, the design of Low Pass Filter (LPF) used in wireless transmit path on  $0.18\mu\text{m}$  SiGe process is presented. This LPF supports both wide-band and narrow-band application.

## II. FILTER STRUCTURE

The proposed LPF has two operating modes for both WCDMA and GSM specs. In WCDMA mode, it is used as a 5th order Butterworth LPF with 3.5MHz cut-off frequency, and in GSM mode, it switches to the 3rd order Butterworth LPF with 405KHz cut-off frequency. It consists of three stages as shown in Fig 1: the first stage is a first order filter to provide the highest input impedance, the second stage is a low Q bi-quad filter and the third stage is a high Q bi-quad filter. In the WCDMA mode, all three stages are turned on while only the first and the third stages are used and the second stage is power down in the GSM mode. The switches select resistors to provide desired cut-off

frequency for different modes. Due to the tight range of cut-off frequency, a calibration is needed to narrow down the variation of cut-off frequency. As highlighted in Fig1, the programmable capacitor array is used to change cut-off frequency according to trim codes. During the calibration, the 4-bit tunable capacitor starts from its largest capacitor value (code 1111) and counts down toward its smallest value (code 0000).

## III. OPERATIONAL AMPLIFIER DESIGN

### A. Design Equations

Operational amplifier (op-amp) is a critical block in this LPF structure which considerably affects the filter performances. The schematic of the op-amp used in this filter design is

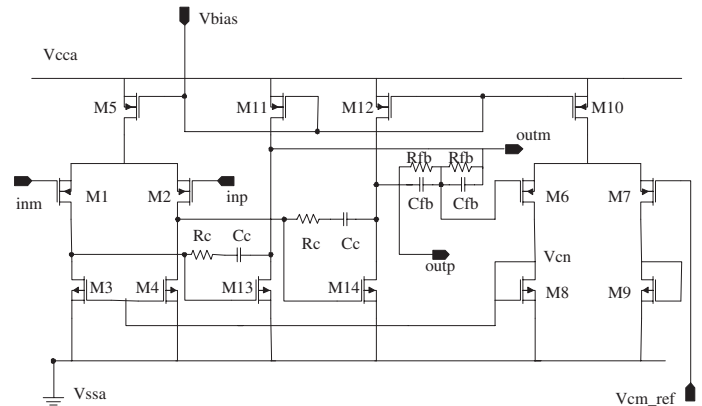


Fig. 2. The two-stage op-amp with CMFB.

shown in Fig 2. It's a two-stage fully differential op-amp with common-mode feedback circuit (CMFB) and compensation resistor  $R_c$  and capacitor  $C_c$ . The current mirror which carries the on-chip  $10\mu\text{A}$  bias current to the current loads is not shown in this graph. In order to use the op amp for the Butterworth filter with 3.5MHz cut-off frequency, the design specifications required for this op-amp are 78dB DC gain, 70MHz unit gain bandwidth (UGBW) with 70 degree phase margin(PM) when driving  $2\text{pF}$  capacitance. The common mode input  $V_{cm}$  is 1.4V and the input swing is  $V_{cm} \pm 0.3$  since the inputs of

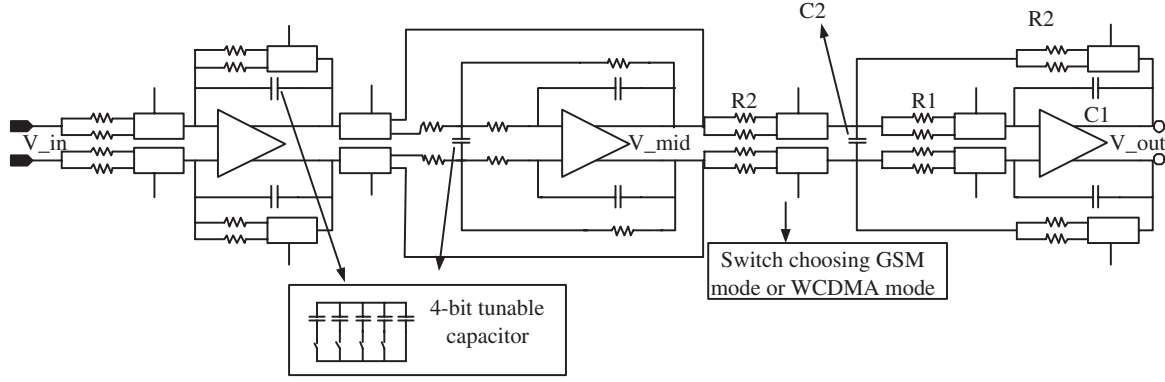


Fig. 1. The structure of the proposed dual-mode low pass filter.

the filter directly connected to the outputs of the DAC which has 1.1V to 1.7V output range.

Fig 3 shows the small-signal mode of this two-stage op-amp. In the small signal mode, we have:

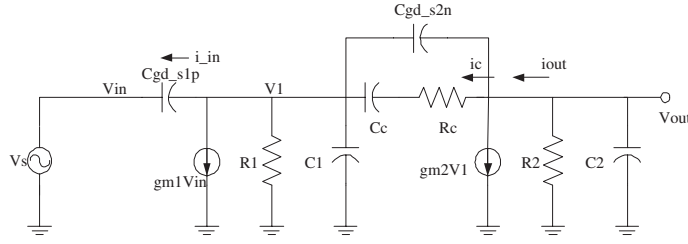


Fig. 3. The small-signal mode of the two-stage op-amp.

$$R_1 = \frac{1}{g_{ds\_s1p} + g_{ds\_s1n}} \quad (1)$$

$$C_1 = C_{db\_s1p} + C_{db\_s1n} + C_{gs\_s2n} \quad (2)$$

$$R_2 = \frac{1}{g_{ds\_s2p} + g_{ds\_s2n} + g_{fb}} \quad (3)$$

$$C_2 = C_{db\_s2p} + C_{db\_s2n} + C_{fb} + C_L, \quad (4)$$

where  $g_{fb}$  and  $C_{fb}$  are the impedance value and the capacitance value of CMFB as shown in Fig 2 while  $C_L$  is the load capacitance.  $g_{ds\_s1n}$  represents  $g_{ds}$  value of nmos in stage1 (M3, M4 in Fig 2) and  $C_{db\_s2p}$  stands for  $C_{db}$  of pmos in stage2 (M11, M12 in Fig 2). In the small signal mode, we have the following KCL and KVL equations:

$$V_{out} = -i_{out}Z_2 \quad (5)$$

$$i_c = i_{out} - g_{m2}V_1 \quad (6)$$

$$i_{in} = (V_1 - V_{in})/Z_{gd1} \quad (7)$$

$$V_1 = (i_c - g_{m1}V_{in} - i_{in})Z_1, \quad (8)$$

where

$$Z_1 = \frac{R_1}{R_1C_1S + 1} \quad (9)$$

$$Z_2 = \frac{R_2}{R_2C_2S + 1} \quad (10)$$

$$Z_c = \frac{R_cC_cS + 1}{R_cC_cC_{gd\_s2n}S^2 + S(C_{gd\_s2n} + C_c)} \quad (11)$$

$$Z_{gd1} = \frac{1}{SC_{gd\_s1p}}. \quad (12)$$

Therefore, the transfer function is obtained:

$$h = \frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}Z_1Z_2\left(\frac{1}{g_{m1}Z_{gd1}} - 1\right)\left(\frac{1}{g_{m2}} - Z_c\right)}{Z_1 + Z_2 + Z_c + g_{m2}Z_1Z_2 + \frac{(Z_2 + Z_c)Z_1}{Z_{gd1}}}. \quad (13)$$

In this design,  $DC\_gain$ ,  $UGBW$  and  $PM$  are three most important specifications. Therefore, before any parameter for transistors are set, poles and zeros are determined to make sure  $UGBW$  and  $PM$  reach the target values. It is reasonable to assume that the first zero/pole and the second and third zero/pole are widely separated. After some deductions and approximations, the following zeros and poles are obtained:

$$\omega_{Z1} = \frac{1}{(R_c - 1/g_{m2})C_c} \quad (14)$$

$$\omega_{Z2} = -\frac{g_{m2}R_c - 1}{C_{gd\_s2n}R_c} \quad (15)$$

$$\omega_{Z3} = -\frac{g_{m1}}{C_{gd\_s1p}}, \quad (16)$$

$$\omega_{P1} = \frac{1}{R_1(C_1 + C_c(1 + g_{m2}R_2)) + R_2(C_2 + C_c)} \quad (17)$$

$$\omega_{P2,3} = \left(\frac{1}{2Q} \pm \frac{1}{2}\sqrt{\frac{1}{Q^2} - 4}\right)\omega_{P0} \quad (18)$$

$$\omega_{P0} = \frac{1}{\sqrt{a}}, \quad (19)$$

where  $Q = \frac{\sqrt{a}}{b}$ ,  $a = C_1C_2C_cR_1R_2R_c\omega_{P1}$  and  $b = (R_1R_2C_c(C_2 + C_1) + R_cC_c(R_1C_1 + R_2C_2) + R_1R_2C_1C_2)\omega_{P1}$ . Three poles are all in the left half plane and the dominant zero  $\omega_{Z1}$  is in the left half plane while two other zeros,  $\omega_{Z2}$  and  $\omega_{Z3}$ , are in the right half plane. Therefore, the transfer function can be expressed in the following way:

$$h(S) = \frac{V_{out}}{V_{in}} = \frac{dc\_gain\left(\frac{S}{\omega_{Z1}} + 1\right)\left(\frac{S}{\omega_{Z2}} + 1\right)\left(\frac{S}{\omega_{Z3}} + 1\right)}{\left(\frac{S}{\omega_{P1}} + 1\right)\left(\frac{S^2}{\omega_{P0}^2} + \frac{S}{\omega_{P0}Q} + 1\right)}. \quad (20)$$

Since  $g_{m2}R_2 \gg 1$

$$\omega_{P1} = \frac{1}{g_{m2}R_1R_2C_c} \quad (21)$$

$$\omega_{P0} = \sqrt{\frac{g_{m2}}{C_1C_2R_c}}. \quad (22)$$

Because DC gain of this op-amp is given by  $g_{m1}R_1g_{m2}R_2$ ,

$$\omega_{P1} = \frac{g_{m1}}{dc\_gain C_c}. \quad (23)$$

### B. Formulations for Power Minimization

Aiming at the minimum static power usage, the op-amp is designed and optimized in the following way. The static power dissipation is given by

$$P_{static} = V_{cc}(2I_{D5} + 2I_{D12}), \quad (24)$$

where  $I_{Di}$  is the static current of transistor  $Mi$ . From [2][4],

$$g_{m1} = \sqrt{\mu_p C_{ox} \frac{W_1}{L_1} I_{D5}} \quad (25)$$

$$C_{gd\_s1p} = C_{gd\_1} = C_{ox} W_1 L_{ov} \quad (26)$$

$$g_{m2} = \sqrt{2\mu_n C_{ox} \frac{W_{14}}{L_{14}} I_{D12}} \quad (27)$$

$$C_{gs\_s2n} = C_{gs\_14} = \frac{2}{3} W_{14} L_{14} C_{ox}. \quad (28)$$

From equation (16), (23), (25) and (26),

$$\sqrt{W_1} = \frac{a_1}{\omega_{Z3}} \sqrt{I_{D5}} \quad (29)$$

$$g_{m1} = a_2 I_{D5} \quad (30)$$

$$I_{D5} = k_1 C_c, \quad (31)$$

where  $a_1 = \sqrt{\frac{\mu_p}{C_{ox} L_1} \frac{1}{L_{ov}}}$ ,  $a_2 = -\frac{a_1 \sqrt{\mu_p C_{ox}}}{\omega_{Z3} \sqrt{L_1}}$  and  $k_1 = -\frac{\omega_{P1} dc\_gain}{a_2} = -\frac{\omega_{Z3} \omega_{P1} L_1 L_{ov} dc\_gain}{\mu_p}$ . Since the lengths of the transistors are usually selected as a constant value,  $a_1$ ,  $a_2$  and  $k_1$  are constants. Therefore,  $I_{D5}$  can be expressed in term of  $C_c$  and a constant. Because  $C_{db}$  is usually much smaller than  $C_{gs}$  or op-amp load capacitance  $C_L$ ,  $C_2 \approx C_L + C_{fb}$  and  $C_1 \approx C_{gs\_s2n}$ . From equation (14), (22), (27) and (28),

$$W_{14}^{1/2} = b_2 \frac{I_{D12}^{1/2}}{R_c} \quad (32)$$

$$g_{m2} = b_3 \frac{I_{D12}}{R_c} \quad (33)$$

$$I_{D12} = \frac{k_3}{1 - \frac{k_2}{R_c C_c}}, \quad (34)$$

where  $b_1 = \frac{3}{2L_{14}^{3/2}} \sqrt{2\frac{\mu_n}{C_{ox}}}$ ,  $b_2 = \frac{b_1}{C_2 \omega_{P0}}$ ,  $b_3 = \sqrt{\frac{2\mu_n C_{ox}}{L_{14}}} b_2$ ,  $k_2 = \frac{1}{\omega_{Z1}}$  and  $k_3 = \frac{1}{b_3}$ .  $b_1$ ,  $b_2$ ,  $b_3$ ,  $k_2$  and  $k_3$  are constants. Since  $C_2 > C_c \gg C_1$  and  $R_1 \gg R_2 \gg R_c$

$$Q = \frac{\sqrt{a}}{b} \approx \sqrt{\frac{C_1 R_c g_{m2}}{C_2}} \quad (35)$$

the second and third pole will be quite close if  $Q \approx 0.5$ . From (27), (28), (32) and (35),

$$I_{D12} = k_0 R_c, \quad (36)$$

where  $k_0 = \sqrt{\frac{Q^2 C_2}{b_4 b_3^2}}$  and  $b_4 = \frac{2\sqrt{2}\mu_n^{1/2} C_{ox}^{3/2} L_{14}^{1/2}}{3}$ .

Therefore,

$$I_{D12} = k_3 + \frac{k_2 k_0}{C_c} \quad (37)$$

$$P(C_c) = (2(k_3 + \frac{k_2 k_0}{C_c}) + 2k_1 C_c) V_{cc}. \quad (38)$$

$P(C_c)$  has the minimum value when  $C_c = \sqrt{\frac{k_2 k_0}{k_1}}$ . Therefore, though some approximations and estimations are made, it is amazing to see that the static power dissipation of this two-stage op-amp is only determined by one variable  $C_c$ .

### C. Design Procedure

The design flow for the proposed power optimized butterworth filter is summarized as follows:

- 1) Determine  $\omega_{Z1}$ ,  $\omega_{Z2}$ ,  $\omega_{Z3}$ ,  $\omega_{P1}$ ,  $\omega_{P2}$ ,  $\omega_{P3}$  from the design specifications such as DC\_gain, UGBW and PM using the Equation (14) to Equation (19).
- 2) Compute  $k_0$ ,  $k_1$ ,  $k_2$  and  $k_3$  from the poles and zeros.
- 3) Choose  $C_c$  that gives the minimum value of the static power and compute  $I_{D5}$  and  $I_{D12}$ .
- 4) Using the following relationships between the design parameters  $\frac{W_5}{L_5} = \frac{W_{10}}{L_{10}} = \frac{I_{D5}}{I_{ref}} = \frac{I_{D10}}{I_{ref}}$  and  $\frac{W_{11}}{L_{11}} = \frac{W_{12}}{L_{12}} = \frac{I_{D12}}{I_{ref}} = \frac{I_{D11}}{I_{ref}}$ , get the widths and lengths of these transistors.
- 5) Obtain  $R_c$  from Equation(36), and obtain  $W_1 = W_2 = W_6 = W_7$  and  $W_{13} = W_{14}$  from Equation (29) and (32).
- 6) Compute  $g_{m1}$ ,  $g_{m2}$  and  $R_{fb}$ .
- 7) Implement the structure and check all the specifications, modify as necessary.

#### Numerical example:

This design procedure is implemented for an op-amp design on  $0.18\mu m$  SiGe process. To satisfy the design specifications for UGBW and PM,  $\omega_{P1} = 2\pi \times 10k$ ,  $-\omega_{Z3} = 2\pi \times 1G$  (which causes 4–5 degree phase margin decrease),  $\omega_{Z1} = 2\pi \times 60M$  (which is close to UGBW) and  $\omega_{P0} = 2\pi \times 140M$  (which is bigger than two times of  $\omega_{Z1}$ ) are set.  $\omega_{Z2}$  will be far away in the right half plane.  $Q \approx 0.5$  and  $dc\_gain = 8000$ . Once these parameters are determined, the power dissipation is minimized by splitting the power between the first and the second stage of the amplifier.

- 1) Compute  $k_0 = 3.4079 \times 10^{-8}$ ,  $k_1 = 1.2566 \times 10^8$ ,  $k_2 = 2.6526 \times 10^{-9}$  and  $k_3 = 2.3167 \times 10^{-5}$ .
- 2) Select  $C_c = 848fF$  and compute  $I_{D5} = 106\mu A$  and  $I_{D12} = 129\mu A$ .
- 3) Compute  $R_c = 3.8k\Omega$ , choose  $L_5 = L_{10} = L_{11} = L_{12} = 2\mu m$ ,  $W_{11} = W_{12} = 13 \times 10\mu m$  and  $W_5 = W_{10} = 10 \times 10\mu m$ .
- 4) Choose  $W_1 = W_2 = W_6 = W_7 = 4 \times 10\mu m$  and  $W_{13} = W_{14} = 9 \times 5\mu m$  while all lengths equal to  $1\mu m$ .
- 5) Compute  $R_{fb} = 30k\Omega$ .
- 6) Implement the structure and check all the specifications, modify the compensation  $R_c$ ,  $C_c$  if necessary.

$R_{fb}$	$C_{fb}$	$R_c$	$C_c$	$C_L$
30.4k $\Omega$	140fF	3.92k $\Omega$	810.4fF	2pf
$(\frac{W}{L})_{5,10}$	$(\frac{W}{L})_{1,2,6,7}$	$(\frac{W}{L})_{3,4,8,9}$	$(\frac{W}{L})_{13,14}$	$(\frac{W}{L})_{11,12}$
100/2	40/1	6/1	45/1	130/2

TABLE I

THE ACTUAL DESIGN PARAMETERS FOR THE PROPOSED OP-AMP ON 0.18 $\mu$ m SiGe PROCESS

	Typical corner	FAST corner	SLOW corner
DC_gain(db)	78.13	78.36	76.35
UGBW	84.23MHz	184MHz	39.8MHz
PM	75.57	59.85	67.98
$I_{D5,10}$	101.2 $\mu$ A	184.2 $\mu$ A	49.8 $\mu$ A
$I_{D11,12}$	132.6 $\mu$ A	241.5 $\mu$ A	65.3 $\mu$ A
$F_{p1}$	8.6kHz	12.2kHz	6.67kHz
$F_{p2}$	133MHz	150MHz	57MHz
$F_{p3}$	163MHz	150MHz	238MHz
$F_{z1}$	67MHz	62MHz	78.7MHz
$F_{z2}$	-1.05GHz	-1.42GHz	-729MHz
$F_{z3}$	-2.99GHz	-4.72GHz	-1.6GHz
Static Power	1.53mW	2.8mW	0.76mW

TABLE II

THE CIRCUITS PERFORMANCE FOR THE PROPOSED OP-AMP ON 0.18 $\mu$ m SiGe PROCESS

Table I shows the actual design parameters we finally set and Table II summarizes the performances of this op-amp works in the normal case, fast corner and slow corner. Fig 4 shows AC response of the proposed op-amp.

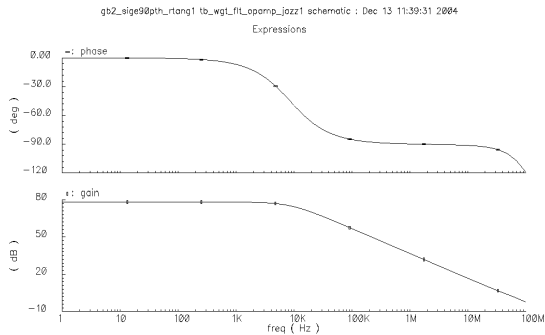


Fig. 4. AC response of the proposed op-amp from Spectre simulator

#### IV. FILTER PERFORMANCE

Based on the proposed op-amp, the three stage LPF shown in Fig 1 is implemented. In WCDMA case,  $\omega_0 = 2\pi f_{wcdma} = 21.99M$  and the ideal transfer function of these three stages are:

$$h1(S) = \frac{1}{\frac{S}{\omega_0} + 1} \quad (39)$$

$$h2(S) = \frac{1}{\frac{S^2}{\omega_0^2} + \frac{S}{0.618\omega_0} + 1} \quad (40)$$

$$h3(S) = \frac{1}{\frac{S^2}{\omega_0^2} + \frac{S}{1.618\omega_0} + 1}, \quad (41)$$

	Filter Specification	Target Value	Simulation Result
WCDMA	Cut-off frequency	3.15MHz to 3.85MHz	3.512MHz
	Pass Band	DC to 1.92MHz $0 \pm 0.3dB$	DC to 1.92MHz $0 \pm 0.12dB$
	A@F $\geq$ 5.4MHz	10dB min	15.77dB
	A@F $\geq$ 7.2MHz	22dB min	27.71dB
	A@F $\geq$ 10 MHz	36dB min	42.06dB
	A@F $\geq$ 13.5MHz	49dB min	55.18dB
A@F $\geq$ 20MHz	66dB min	73.01dB	
GSM	Cut-off frequency	345kHz to 465kHz	406.3kHz
	Pass Band	DC to 140kHz $0 \pm 0.2dB$	DC to 140kHz $0 \pm 0.1dB$
	A@F $\geq$ 680kHz	10dB min	12.9dB
	A@F $\geq$ 1.1MHz	22dB min	25.12dB
	A@F $\geq$ 1.8MHz	35dB min	36.7dB
	A@F $\geq$ 3.2MHz	50dB min	50.57dB

TABLE III

GSM AND WCDMA SPECIFICATIONS AND THE SIMULATION RESULTS FROM CADENCE SPECTRE (NOTE: A=ATTENUATION AND F=FREQUENCY)

where h2 is a low Q biquad and h3 is a high Q biquad. In GSM case,  $\omega_0 = 2\pi f_{gsm} = 2.54M$  and the transfer function is:

$$h(S) = \frac{1}{\frac{S}{\omega_0} + 1} \times \frac{1}{\frac{S^2}{\omega_0^2} + \frac{S}{\omega_0} + 1}. \quad (42)$$

In the biquad filter, we have

$$h = \frac{V_{out}}{V_{in}} = \frac{1}{C_1 C_2 R_1 R_2 S^2 + (2C_1 R_1 + C_1 R_2)S + 1}. \quad (43)$$

Therefore,  $\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}$  and  $Q = \frac{C_1(2R_2 + R_1)}{\sqrt{C_1 C_2 R_1 R_2}}$ . For the first stage,  $\omega_0 = \frac{1}{RC}$ . After theoretical computation and some adjustments, all the filter design specifications are satisfied. The resistors are implemented using P+ poly resistors while the capacitances are implemented using MIM capacitor over nwell. The filter performances for both GSM and WCDMA modes are shown in Table III.

#### V. CONCLUSION

In this paper, a innovative and effective design method for high PM and large UGBW op-amp is presented focusing on power minimization. Since high frequency performance is essential, Miller capacitance  $C_{gd}$  which determine the value of the second and the third zeros is considered. Alternative formulations for DC current of the transistors are obtained to minimize the static power consumption. A op-amp on 0.18 $\mu$ m SiGe process is designed use this approach and a dual-mode LPF is implemented with this op-amp.

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