

Optimal Spare Utilization in Repairable and Reliable Memory Cores

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Abstract

Advances in System-on-Chip (SoC) technology rely on manufacturing and assembling high-performance system cores for many critical applications. Among these cores, memory occupies the largest portion of the SoC area; this trend much likely will continue in the future as it is widely anticipated that it will approach the 94% level by the year 2014. As memory cells are more prone to defects and faults than logic cells, redundancy has been extensively used for enhancing defect and fault tolerance through repair by spare (row and column) replacement. Unlike legacy PCB (printed circuit board) or MCM (multichip module) based systems, embedded cores cannot be physically replaced once they are fabricated onto a SoC. To realize both enhanced manufacturing yield and field reliability, ATE (automated test equipment) and BISR (built-in-self-repair) are utilized to allocate redundancy for the embedded memory cores. As ATEs (for the repair of manufacturing defects) and BISR (for repairing field faults) rely on the provided redundancy (rows and columns), spare partition and utilization techniques are proposed in this paper to achieve an optimal combination of yield and reliability for embedded memory cores. Parametric simulation results for the single dimensional (i.e., spare columns) and two-dimensional (i.e., both spare columns and rows) cases are provided.

Keywords: Embedded Memory Repair and Reliability, System-on-chip, Fault-Tolerant Memory Core, Built-In-Self-Repair, Yield.

1 Introduction

Advances in Ultra-Large-Scale-Integration (ULSI) have made possible the seamless embedding of numerous cores on a single chip (i.e., commonly referred to as *System-On-Chip* technology); the dependability of SoC has become a stringent requirement for different applications (such as

high-performance and critical systems) because a small performance degradation or defect in core components can result in unacceptably low manufacturing yield and field reliability of the SoC. According to the Semiconductor Industry Association and ITRS2000, embedded memory will continue to dominate the SoC content in the next several years, approaching 94% of the die area by 2014, as shown in Figure 1 [6]. For SoC integration, one of the most common and important cores is the repairable embedded memory because memory cells are usually more prone to defects and faults compared with components in other cores such as logic cells [3, 4, 5, 8, 9, 10, 11, 12]. Yield enhancement and field reliability are usually combined under the measure of *dependability*. The issues surrounding the dependability of high-density multi-megabit embedded memory must be efficiently solved to meet this trend and to produce cost effective SoC-based products. As the SoC fabrication process utilizes deep-sub-micron technology (such as today's line width of $0.13\mu m$), the need for a high yield and ultra reliable embedded memory core becomes obvious. Reconfiguration (repair) of memory arrays using spare lines (rows and columns) is the most common technique for yield enhancement of these chips [3, 4, 5, 8, 9, 10, 11, 12]. Numerous algorithms have been proposed by which rows and columns with faulty cells are logically deleted from the functioning chip and replaced by fault-free spares. Unfortunately, once fabricated embedded memory cores cannot be physically replaced in the field. Thus, built-in test, diagnosis and repair circuits for field utilization are also provided along with ATE-based repair facilities to assure improved manufacturing yield and field reliability of these cores [4, 3, 5, 8]. [4] has proposed a SRAM embedded memory with low cost in which redundancy is controlled through switches by FLASH EEPROMs. In [5], a simple built-in-self-analysis-repair scheme (generally known as CREASTA) for embedded DRAM has been proposed. A row-column self-repair scheme for the embedded SRAM module of the Alpha 21264 has been analyzed in [8]. A shared built-in self-

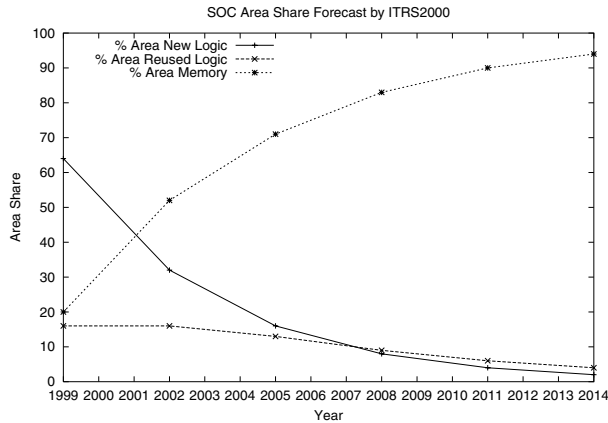


Figure 1. SoC area forecast of embedded memory cores, ITRS2000

repair analysis scheme (Shared-BISA) for multiple embedded memory cores in SoC applications has been proposed in [3]; this approach offers an area penalty realization which is independent of the number of embedded memory cores. Although it is clear that a combination of ATE and BISR is able to achieve significant improvements in manufacturing yield (i.e., the probability for a memory to be manufactured and repaired as functional) and field reliability (i.e., the function of time which is defined by the conditional probability that the system performs correctly throughout the interval of time $[t_0, t]$ given the system was performing flawlessly at the initial time t_0), an existing problem that this remains unaddressed for embedded memory cores is the so-called *balanced redundancy partition and utilization*, i.e. the utilization of spare resources commonly associated with redundant spare rows and columns for the dual purpose to achieve high yield (by circumventing defects at manufacturing) and high reliability (to take care of field faults). As ATEs (for repairing manufacturing defects) and BISR (for repairing field faults) utilize the same spare resources, a technique for a balanced redundancy partition and utilization is very important, thus allowing to achieve the ultimate combination of acceptable yield and reliability of the embedded memory cores. Thus, dependability evaluation techniques for single (one-dimensional) and two-dimensional redundancy architectures will be initially investigated for redundancy balancing. Then, balanced partition and utilization techniques for both single and two-dimensional redundancy architectures will be evaluated. Extensive parametric simulation results will be presented. The organization of the paper is as follows. In the following section (Section 2), a conceptual architectural model of the embedded memory core with both ATE-based and BISR capabilities will be shown. The significance of redundancy partition

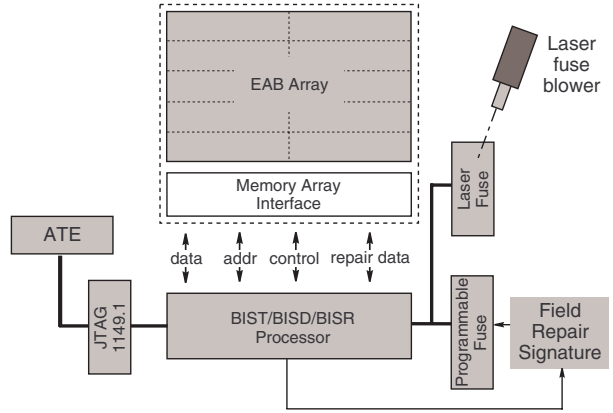


Figure 2. Model embedded memory system core architecture

and utilization for yield and reliability will be discussed. In Section 3 and 4, a detailed yield and reliability analysis for the single and two-dimensional redundancy cases will be pursued respectively. Balanced redundancy partition and utilization will be proposed for both cases. Parametric simulation is used to further verify the effectiveness of the proposed redundancy techniques in Section 5. Finally, discussion and conclusions are given in Section 6.

2 Preliminaries

Figure 2 shows the model of the embedded memory system core under investigation; both ATE-based repair for manufacturing and BISR for field operation are performed for manufacturing yield and field reliability enhancement. Within this analysis the embedded memory system core consists of the following components.

- IEEE JTAG (Joint Test Action Group) 1149.1 : Boundary-scan interface for test and repair [1, 2].
- Laser Fuse : A set of laser reconfigurable fuses to permanently program the given redundancy resources in factory [7].
- BIST/BISD/BISR Processor : This system component governs self-test, self-diagnosis, and self-repair procedures.
- Programmable Fuse : A set of programmable fuses to store additional reconfiguration signature generated by the BIST/BISD/BISR processor in field.
- Memory Array Interface : This component connects the EAB (embedded array block) array and the

BIST/BISD/BISR Processor together. Data, address, control and repair data flow via this component.

The embedded memory system core is tested and repaired according to the following processes.

- *Factory Repair*: To circumvent defects due to imperfect manufacturing processes, the ATE communicates with the embedded memory system core via its external test equipment interface (as provided by pin electronics in the head architecture). Then, the laser fuse is permanently programmed to allocate redundancy and to repair manufacturing defects in the EABs.
- *Field Repair*: Whenever the SoC is reset or powered, the BISR circuitry tests, diagnoses and repairs the EABs. The programmable units (such as switches) are programmed to store the information for redundancy allocation.

Although it is obvious that a combination of ATE and BISR is much likely able to achieve significant enhancements of manufacturing yield and field reliability for SoC with embedded memory system cores, a problem still remains unsolved: *the provided redundancy in terms of spare rows and columns must be partitioned into two groups (i.e., one for ATE repair and one for BISR) such that both the manufacturing yield and field reliability can be adjusted for increased dependability.* As an ATE (for the repair of manufacturing defects) and BISR (for repairing field faults) share the provided redundancy, a balanced partition and utilization of the spare lines is very important to achieve the desired combination of yield and reliability of the embedded memory system core. Balanced redundancy partition and utilization of the embedded memory system core with one-dimensional redundancy (spare rows or columns) will be investigated in the next section followed by the two-dimensional case (both spare rows and columns) in Section 4.

3 One-Dimensional Redundancy

The following notation will be used throughout this manuscript

- n_c : Number of columns of the memory (i.e., number of bits per word).
- n_r : Number of rows of the memory (i.e., number of words).
- s_c : Number of spare columns.
- s_{cm} : Number of spare columns used for manufacturing yield improvement (i.e., $s_c - s_{cf}$).

- s_{cf} : Number of spare columns used for field reliability improvement (i.e., $s_c - s_{cm}$).
- λ_m : Expected number of manufacturing defects per memory cell.
- λ_f : Field failure (arrival) rate of a memory cell per unit time interval.
- Y : Manufacturing yield.
- $R(t)$: Field reliability at time t .
- $D(t)$: Overall dependability.

The yield of a single cell is usually characterized by the exponential failure law as

$$Y_{cell} = e^{-\lambda_m} \quad (1)$$

Therefore, the probability of having n_r non-defective cells in a column (i.e., the yield of a column) can be written as

$$Y_{column} = (Y_{cell})^{n_r} \quad (2)$$

The memory consists of n_c memory columns and s_{cm} spare memory columns. The quorum size of the memory is that n_c of the total of $n_c + s_{cm}$ columns are required to be functional as part of the EAB. Thus, the memory yield with column-redundancy can be formulated using the binomial distribution as

$$Y = \sum_{i=0}^{s_{cm}} \binom{n_c + s_{cm}}{i} (Y_{column})^{n_c + s_{cm} - i} \cdot (\bar{Y}_{column})^i \quad (3)$$

As is well known, the binomial distribution can be approximated by the Poisson distribution. This approximation technique avoid a great deal of algebra associated with the equation shown above. If $\bar{Y}_{column} \leq 0.05$ and $n_c \geq 20$, the following approximation holds.

$$Y = \sum_{k=s_{cm}}^{n_c} \frac{(n_c \bar{Y}_{column})^k e^{-n_c \bar{Y}_{column}}}{k!} \quad (4)$$

Reliability can be assessed in a similar fashion as follows

$$R_{cell}(t) = e^{-\lambda_f \cdot t} \quad (5)$$

$$R_{column}(t) = (R_{cell}(t))^{n_r} \quad (6)$$

$$R(t) = \sum_{i=0}^{s_{cf}} \binom{n_c + s_{cf}}{i} (R_{column}(t))^{n_c + s_{cf} - i} \times (1.0 - R_{column}(t))^i$$

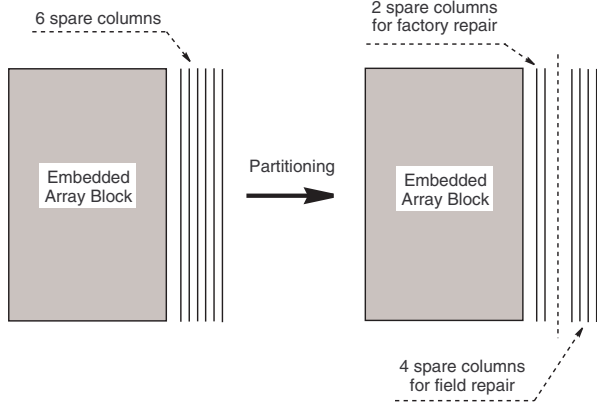


Figure 3. Example of redundancy partition for one dimensional redundancy

$$\begin{aligned}
 &= \sum_{i=0}^{s_c - s_{cm}} \binom{n_c + s_c - s_{cm}}{i} \\
 &\times (R_{column}(t))^{n_c + s_c - s_{cm} - i} \\
 &\times (1.0 - R_{column}(t))^i \quad (7)
 \end{aligned}$$

Also, the following approximation holds in case of $\bar{R}_{column}(t) \leq 0.05$ and $n_c \geq 20$.

$$R(t) = \sum_{k=s_{cf}}^{n_c} \frac{(n_c \bar{R}_{column}(t))^k e^{-n_c \bar{R}_{column}(t)}}{k!} \quad (8)$$

The conditional probability of having a memory manufactured-as-good (i.e., Y) and not-failing-in-field during the time interval $[t_0, t]$ (i.e., $R(t)$) is referred to as *dependability* and is denoted by $D(t)$. Since Y and $R(t)$ are serial probabilities, the product of equations 3 and 7 can be used to formulate $D(t)$ as

$$\begin{aligned}
 D(t) &= Y \cdot R(t) \quad (9) \\
 &= \sum_{i=0}^{s_{cm}} \binom{n_c + s_{cm}}{i} (Y_{column})^{n_c + s_{cm} - i} \\
 &\times (1.0 - Y_{column})^i \\
 &\times \sum_{i=0}^{s_c - s_{cm}} \binom{n_c + s_c - s_{cm}}{i} \\
 &\times (R_{column}(t))^{n_c + s_c - s_{cm} - i} \\
 &\times (1.0 - R_{column}(t))^i \quad (10)
 \end{aligned}$$

If $\bar{Y}_{column} \leq 0.05$, $\bar{R}_{column}(t) \leq 0.05$ and $n_c \geq 20$, the following approximation holds.

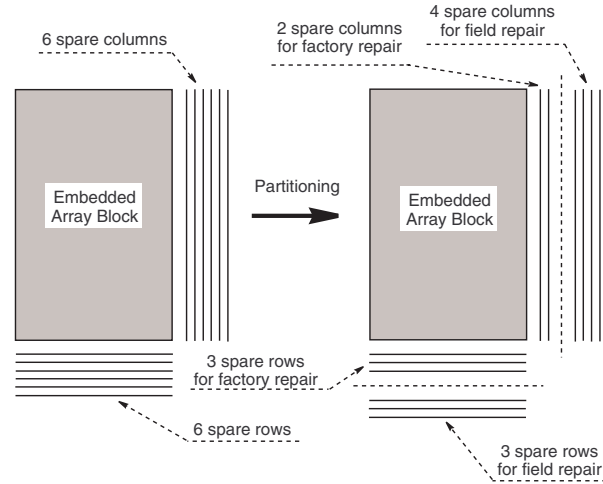


Figure 4. Example of redundancy partition for two-dimensional redundancy

$$\begin{aligned}
 D(t) &= \sum_{j=s_{cm}}^{n_c} \frac{(n_c \bar{Y}_{column})^j e^{-n_c \bar{Y}_{column}}}{j!} \\
 &\times \sum_{k=s_{cf}}^{n_c} \frac{(n_c \bar{R}_{column}(t))^k e^{-n_c \bar{R}_{column}(t)}}{k!} \quad (11)
 \end{aligned}$$

To find the spare allocation corresponding to a balanced s_{cm} , $D(t)$ must be differentiated and solved with respect to s_{cm} , i.e. .

$$\frac{dD(t)}{ds_{cm}} = 0 \quad (12)$$

Note that s_{cf} follows because $s_{cf} = s_c - s_{cm}$. s_{cm} must be an integer, so, both $\lceil s_{cm} \rceil$ and $\lfloor s_{cm} \rfloor$ must be evaluated to determine the optimal partition of the spare resources. Figure 3 shows an example of a EAB with six spare columns. In a latter section, this set will be partitioned into two groups: two spare columns for ATE repair and four spare columns for BISR.

4 Two-Dimensional Redundancy

The following notation will be used in addition to the one presented in the previous section.

- s_r : Number of spare rows.
- s_{rm} : Number of spare rows used for enhancing the manufacturing yield (i.e., $s_r - s_{rf}$).

- s_{rf} : Number of spare rows used for enhancing the field reliability (i.e., $s_c - s_{rm}$).
- λ_{cm} : Expected number of manufacturing defects per column in the memory.
- λ_{rm} : Expected number of manufacturing defects per row in the memory.
- λ_{cf} : Field failure (arrival) rate of column per unit time interval.
- λ_{rf} : Field failure (arrival) rate of row per unit time interval.

Repair by row/column deletion is an NP-complete problem. An exact closed formulation of Y and $R(t)$ is intractable. So, in this paper, a line-based fault evaluation is pursued for the two-dimensional case (in place of a cell-based evaluation as used previously for the one-dimensional case). The yield of a row and a column in the memory can be approximated as $Y_{row} = e^{-\lambda_{rm}}$ and $Y_{column} = e^{-\lambda_{cm}}$ respectively. Then, the yield of all rows in the memory (subject to the quorum for a repaired memory) is given by

$$Y_{rows} = \sum_{i=0}^{s_{rm}} \binom{n_r + s_{rm}}{i} (Y_{row})^{n_r + s_{rm} - i} \times (1.0 - Y_{row})^i \quad (13)$$

Equivalently, the yield of all columns in the memory (subject to the quorum for a repaired memory) is

$$Y_{columns} = \sum_{i=0}^{s_{cm}} \binom{n_c + s_{cm}}{i} (Y_{column})^{n_c + s_{cm} - i} \times (1.0 - Y_{column})^i \quad (14)$$

Thus, the overall yield of the memory is given by an approximation which considers the yields of both rows and columns, i.e.

$$Y = Y_{rows} \times Y_{columns} \quad (15)$$

It is also possible to use the following Poisson approximation for reduced algebraic complexity, if Y_{row} & $Y_{column} \leq 0.05$ and s_{rm} & $s_{cm} \geq 20$.

$$Y = \sum_{j=s_{rm}}^{n_r} \frac{(n_r \bar{Y}_{row})^j e^{-n_r \bar{Y}_{row}}}{j!} \times \sum_{k=s_{cm}}^{n_c} \frac{(n_c \bar{Y}_{column})^k e^{-n_c \bar{Y}_{column}}}{k!} \quad (16)$$

The same approximation can be also derived for reliability under field repair; likewise,

$$R_{row}(t) = e^{-\lambda_{rm} t} \quad (17)$$

$$R_{column}(t) = e^{-\lambda_{cm} t} \quad (18)$$

$$R_{rows}(t) = \sum_{i=0}^{s_{rf}} \binom{n_r + s_{rf}}{i} (R_{row}(t))^{n_r + s_{rf} - i} \times (1.0 - R_{row}(t))^i \quad (19)$$

$$= \sum_{i=0}^{s_r - s_{rm}} \binom{n_r + s_r - s_{rm}}{i} \times (R_{row}(t))^{n_r + s_r - s_{rm} - i} \times (1.0 - R_{row}(t))^i \quad (20)$$

$$\times (1.0 - R_{row}(t))^i \quad (21)$$

$$R_{columns}(t) = \sum_{i=0}^{s_{cf}} \binom{n_c + s_{cf}}{i} \times (R_{column}(t))^{n_c + s_{cf} - i} \times (1.0 - R_{column}(t))^i = \sum_{i=0}^{s_c - s_{cm}} \binom{n_c + s_c - s_{cm}}{i} \times (R_{column}(t))^{n_c + s_c - s_{cm} - i} \times (1.0 - R_{column}(t))^i \quad (22)$$

$$R(t) = R_{rows}(t) \times R_{columns}(t) \quad (23)$$

Also, the following approximation holds in case of $\bar{R}_{row}(t)$ & $\bar{R}_{column}(t) \leq 0.05$ and n_r & $n_c \geq 20$.

$$R(t) = \sum_{j=s_{rf}}^{n_r} \frac{(n_r \bar{R}_{row}(t))^j e^{-n_r \bar{R}_{row}(t)}}{j!} \times \sum_{k=s_{cf}}^{n_c} \frac{(n_c \bar{R}_{column}(t))^k e^{-n_c \bar{R}_{column}(t)}}{k!} \quad (24)$$

The overall dependability is the conditional probability of both field reliability and yield, i.e.

$$D(t) = Y \times R(t) \quad (25)$$

To find the allocation corresponding to a balanced s_{cm} and s_{rm} , $D(t)$ can be differentiated and solved with respect to s_{cm} and s_{rm} as follows.

$$\frac{d^2 D(t)}{ds_{cm} ds_{rm}} = 0 \quad (26)$$

Note that also in this case s_{cf} and s_{rf} follow because $s_{cf} = s_c - s_{cm}$ and $s_{rf} = s_r - s_{rm}$, s_{cm} and s_{rm} must be integer; so, both $\lceil s_{cm} \rceil$ and $\lfloor s_{cm} \rfloor$ and $\lceil s_{rm} \rceil$ and $\lfloor s_{rm} \rfloor$ must be evaluated to determine the final partition and the division of the spare lines. Figure 4 shows an example of a EAB with six spare columns and six spare rows. Later, the spare columns are partitioned into two groups: two spare columns for ATE repair and four spare columns for BISR and spare rows are also partitioned into two groups: three spare columns for ATE repair and three spare columns for BISR.

5 Parametric Simulation and Results

The effect of redundancy balancing for the one and two dimensional cases will be studied through numerical experiments. The parameters used in the simulation are summarized in Table 1 (one-dimensional case) and Table 2 (two-dimensional case).

Table 1. Simulation parameters for the one-dimensional case

Parameters	n_c & n_r	s_c	λ_m	λ_f	t
Values	128	8	10^{-4}	10^{-5}	10

The simulation results for the single dimensional redundancy case are shown in Figure 5 and 6, the following observations are made.

- *Symmetric Case* : In Figure 5 and 6, the dependability and its derivative are plotted with respect to s_{cm} using points with blank box symbol. In this case, parameters are selected in order to show symmetric behavior in both Y and $R(t)$. Thus, the partition is [4,4]: 4 spare columns for factory repair and 4 spare columns for field repair, i.e. spares are evenly partitioned and utilized.
- *Reliability-Intensive Case* : In Figure 5 and 6, the dependability and its derivative are plotted with respect to s_{cm} using points with cross symbol. In this case, parameters are selected to take into account the presence of more field faults than manufacturing defects (i.e., $t = 10 \rightarrow 20$). Thus, the partition is now [3,5]: 3 spare columns for factory repair and 5 spare columns for field repair, i.e. in this case spares are partitioned and utilized to achieve an enhancement in field reliability.

- *Yield-Intensive Case* : In Figure 5 and 6, the dependability and its derivative are plotted with respect to s_{cm} using points with blank diamond symbol. In this case, parameters are selected such that more manufacturing defects than field faults are induced (i.e., $\lambda_m = 10^{-4} \rightarrow 2 \times 10^{-4}$). Thus, the partition is [5,3]: 5 spare columns for factory repair and 3 spare columns for field repair. Spares are partitioned and utilized to increase the manufacturing yield.

For the two-dimensional redundancy case (as shown in Figure 7 - 12), similar observations can be made.

6 Discussion and Conclusions

Among cores for SoC integration, the embedded memory core occupies the largest area and its performance in terms of manufacturing yield and field reliability is very important because memory cells are usually more prone to defects and faults than other components such as logic cells. Since cores cannot be physically replaced once they are fabricated onto a SoC, a combination of ATE and BISR is common practice. Proper partition and utilization of the spare redundancy is significantly desirable to achieve a balance of manufacturing yield and field reliability of the embedded memory system. Thus, yield and reliability assurance techniques have been proposed for the one dimensional redundancy case (only spare columns), then extended to two-dimensional redundancy case (both spare rows and columns are present). As a figure of merit between yield and reliability, dependability (i.e., $Y \times R(t)$) is proposed. Maximum dependability is possible only if the provided redundancy is partitioned properly into two groups to repair both manufacturing defects (i.e., ATE-based repair) and field faults (i.e., BISR). To accomplish a balanced redundancy partition and utilization, the equations for the dependability are differentiated and solved with respect to the number of spares used to enhance the manufacturing yield. Parametric simulation results have verified that the proposed redundancy partition and utilization techniques for embedded memory system cores achieves the theoretically optimal value. The proposed techniques can be incorporated with existing CAD compilers for embedded memory system cores, thereby providing a cost-effective partition and utilization of the shared redundant spares.

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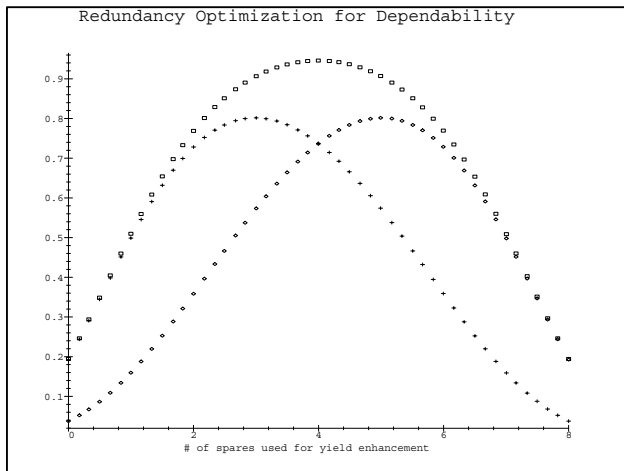


Figure 5. Dependability graph for 1D redundancy

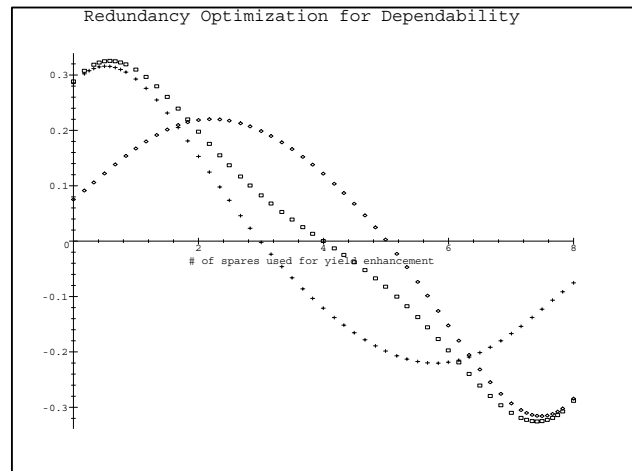


Figure 6. Balanced partition results: [3,5], [4,4] and [5,3]

Table 2. Simulation parameters for the two-dimensional case

Parameters	n_c & n_r	s_c & s_r	$\lambda_c m$ & $\lambda_r m$	$\lambda_c f$ & $\lambda_r f$	t
Values	128	8	10^{-2}	10^{-3}	10

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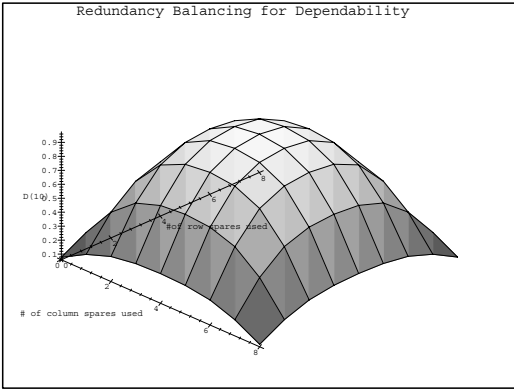


Figure 7. Symmetric dependability for 2D redundancy

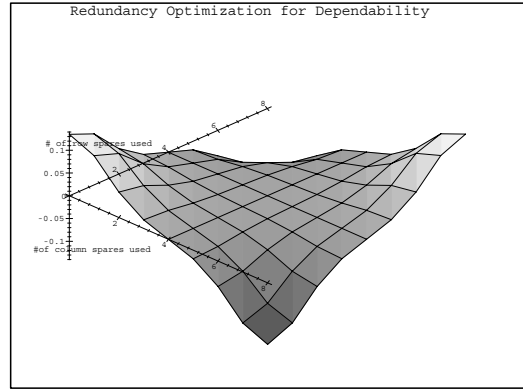


Figure 8. Balanced partition for {[4,4],[4,4]}

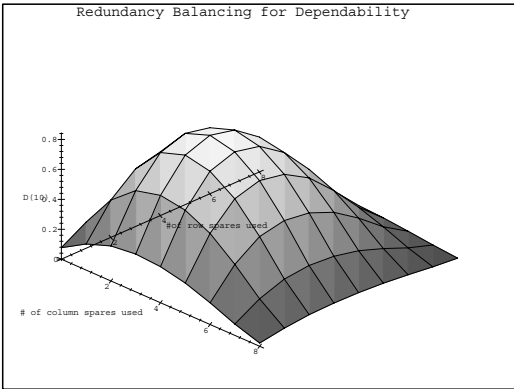


Figure 9. Reliability-intensive dependability for 2D redundancy

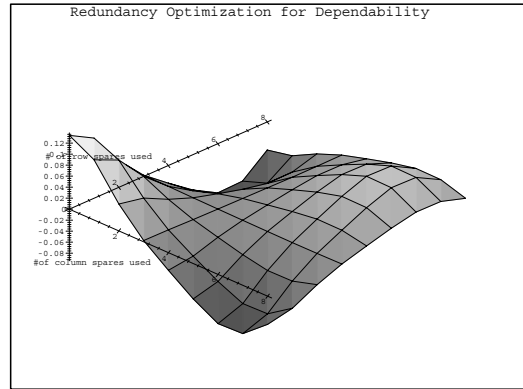


Figure 10. Balanced partition for {[3,5],[3,5]}

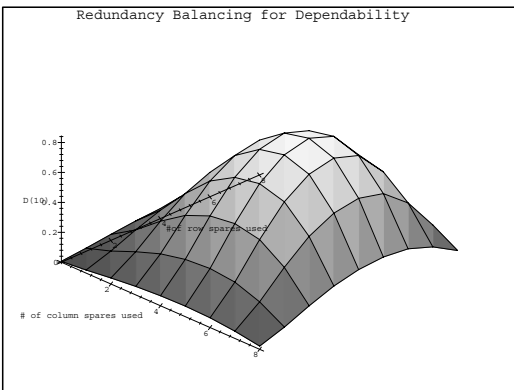


Figure 11. Yield-intensive dependability for 2D redundancy

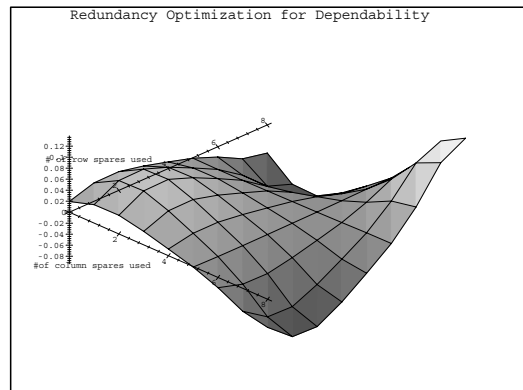


Figure 12. Balanced partition for {[5,3],[5,3]}