

# 0.8 $\mu$ m CMOS Optical Clock Receiver Design

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## Abstract

This paper describes a CMOS optical signal receiver circuit design, analysis, and implementation, which has been developed for on-chip optical clock distribution. The optical receiver block consists of a photo detector, a transimpedance pre-amplifier, and a post-amplifier, and a wave shaping stage. The input current dynamic range is between 30 $\mu$ A and 100 $\mu$ A. In order to achieve the high switching speeds the front-end part of the optical receiver circuit has been in pure analog way to get the full 5V swing at the output with Automatic Gain Control (AGC). The optical receiver circuit has been implemented using CMOS 0.8 $\mu$ m technology. High speed operation up to 450-Mb/s has been verified with power consumption of 9.3mW. It uses 5V single power supply and the die size is 0.3 X 0.25 mm<sup>2</sup> including bonding pads.

## 1 Introduction

As the clock frequency of VLSI systems and die area continue to increase, the problem associated with clock skew becomes one of the major problems in VLSI systems design. Timing constraints for the state of the art VLSI in silicon are rapidly approaching communication limits available with layered two-dimensional metal and polysilicon wiring approaches. Transmission line effects and electromagnetic interferences are two of the many challenges encountered in high frequency clock distribution [1].

As a solution to minimize the clock skew on Ultra Large Scale Integrated Circuit (ULSI) such as the systems design using memory/logic merged technology, the optical clock distribution using SiO<sub>2</sub>/Si or SiO<sub>3</sub>/SiO<sub>2</sub> on chip wave guide is proposed. [2, 3]

Clock receivers are placed periodically along an optical wave guide. In each receiver, the optical signal emerging from the wave guide is converted to an electrical current by a photodiode, which is then amplified by a low noise transimpedance amplifier.

This paper describes an CMOS integrated circuit designed for the optical clock receiver. The design consideration is discussed in Section 2. Section 3 discusses the circuit design issues followed by input noise consideration in Section 4. Simulation and fabrications are discussed in Section 5. Performance and conclusion are discussed in Section 6 and 7, respectively.

## 2 Design Consideration

The principal system trade-offs involve the physics of photo detection and wavelength of the optical signal. The designer of a photodetector generally has

the option of applying a large enough reverse bias to adjust the depletion layer width to match the photon absorption length for the wavelength of light that is detected. This is where a principle conflict between design elements of the goals for the optical clock distribution system is observed. The optical receiver in this paper uses a PIN photodiode among several other choices, because the bandwidth is much higher than that of avalanche photodiodes. This involves a non-standard fabrication process. However, this process conflict can be avoided by mounting the PIN diode on the surface of a silicon die.

An optical receiver for a low-cost, high speed optical link must convert a  $\mu$ A range input current into a digital voltage signal. The optical clock is distributed over silicon using silicon-base wave guide, furthermore, the wave guide has to be bent to a certain extent on the chip surface to distribute the optical signals to all over the places on almost wafer surface. Therefore, the optical signal attenuation has to be considered. Based on actual silicon-base wave guide simulation the typical requirement for photo diode current ranges between 30 $\mu$ A and 100 $\mu$ A.

There are four main circuit design issues in designing an optical transimpedance amplifier.

1. To minimize input noise
2. To maximize bandwidth for desired data rate
3. To produce rail-to-rail output voltage
4. To stabilize for different process corners and temperatures

The first three requirements are dependent each other because bandwidth can often be increased at the expense of noise, and gain bandwidth product is constant.

## 3 Circuit Design

A circuit diagram of an optical clock receiver (transimpedance amplifier) is shown in Fig. 1. In order to accomplish the high speed amplifier, a local shunt feedback inverting pre-amplifier is used. The resistively biased NMOS transistor is used as a feedback element. The receiver circuit is composed of analog preamplifier followed by post amplifier section which are analog buffer stages to amplify the detected input photocurrent to voltage signal levels enough to drive CMOS logic circuits.

The receiver has been designed to provide a dynamic input current range between 30 $\mu$ A and 100 $\mu$ A using

Automatic Gain Control(AGC). Larger input causes circuit saturation and smaller input current is limited by noise. An AGC is required to follow the wide input dynamic range. Without this AGC loop the input dynamic range would have been between  $30\mu\text{A}$  and  $60\mu\text{A}$  instead of between  $30\mu\text{A}$  and  $100\mu\text{A}$ . The optical receiver was designed using a shunt feedback resistor. A resistive feedback element is required for the photocurrent to modulate the gate signal of the N-type device of the first amplifying stage. The modulated output signal of the first stage is modulated and amplified through the next three analog amplifying stages.

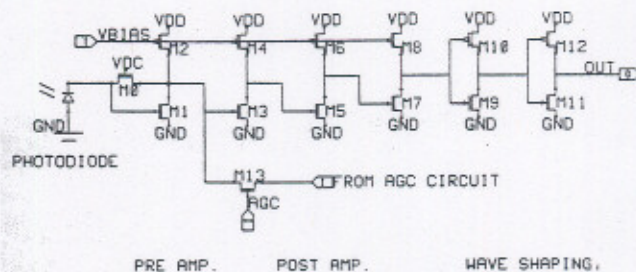


Fig.1 Circuit diagram of transimpedance amplifier

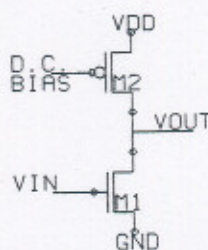


Fig.2 Analog inverting amplifier

Fig.2 shows the analog inverting amplifier. If body effect and channel length modulation are neglected, the small-signal voltage gain is simply given by

$$\begin{aligned}
 A_v &= -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \\
 &= -\frac{2I_D}{V_{gs1} - V_{t1}} \\
 &= -\frac{2I_D}{V_{gs2} - V_{t2}} \\
 &= -\left(\frac{V_{gs2} - V_{t2}}{V_{gs1} - V_{t1}}\right) \quad (1)
 \end{aligned}$$

where  $g_{m1}$ ,  $g_{m2}$  are transconductances of N and P transistor, respectively, and  $I_D$  is drain current.  $V_{gs1}$  and  $V_{gs2}$  are gate source voltages of N and P transistor, respectively,  $V_{t1}$  and  $V_{t2}$  are threshold voltages.

The relationship among slew rate, unity-gain bandwidth is given by

$$SR = (V_{gs} - V_t)\omega_1 \quad (2)$$

where SR is slew rate,  $V_{gs}$  and  $v_t$  are gate and threshold voltages of pull down transistor and  $\omega_1$  is the unity gain frequency of the amplifier.[4]

From equation (1) and (2) it becomes clear that there is a trade-off relationship between gain and slew rate. If the amplifier is designed for high gain, the slew rate becomes poorer. In this paper high speed requirements is more critical than other issues. Therefore, transistor sizes have been determined for high slew rate at the expense of gain of the amplifier stages. To insure minimum gain required multiple gain stages are used to get enough overall gain of the amplifier. These amplifiers are connected directly to each other without coupling capacitors to ensure good response at low and high frequencies. The other issue is involved in transistor sizing, which is the noise issue and it will be addressed in Section 4. Finally, a couple of digital inverter string has been added to obtain a rail-to-rail digital signal at the output.

#### 4 Noise Consideration

The simplified equivalent circuit of the input preamplifier stage of the transimpedance amplifier in Fig.1 is shown in Fig.3. Since the noise due to the analog buffer stages after preamplifier is negligible we focus on the noise of the first input stage.

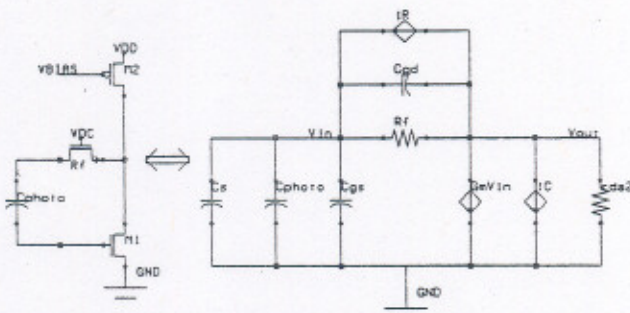


Fig.3 Small signal equivalent circuit of the preamplifier stage

In Fig.3  $C_{photo}$ ,  $C_{gs}$ ,  $C_s$ ,  $C_{gd}$  represent the photodiode capacitance, gate-to-source capacitance, stray capacitance, and gate-to-drain capacitance of the input transistor M1, respectively.  $R_f$  represents feedback resistance while  $i$ , and  $i_c$  represent the mean square noise current at the feedback resistor and the channel.

Since modern devices demonstrate very low leakage current, the noise in the photodiode can be ignored. Under this assumption, there are two main noise sources of the amplifier, which are thermal noise  $i_c$  in the channel of the input pull-down transistor and the thermal noise  $i_r$  in the feedback resistor.[5] The thermal noise in the channel is drain-source shot noise and calculated as

$$\overline{i_r^2} = 4kTB(2/3)g_m \quad (3)$$

where  $k$  is Boltzmann's constant,  $T$  is the temperature in Kelvin,  $B$  is the noise bandwidth of the receiver(constant). For the noise analysis, the effects of each source on the output voltage of the first stage are determined. The nodal equation of Fig.3 gives

$$V_{out} = (1/g_m) \times \frac{1 + j\omega(C_z + C_{gd}) \times R_f}{1 + j\omega \frac{(C_z + g_m r_{ds2} C_{gd}) R_f}{g_m r_{ds2}}} \times i_c + (R_f) \times \frac{1}{1 + j\omega \frac{(C_z + g_m r_{ds2} C_{gd}) R_f}{g_m r_{ds2}}} \times i_r \quad (4)$$

where  $C_z = C_{gs} + C_s + C_{photo}$ . The noise current  $i_c$  and  $i_r$  can be represented as equivalent input noise current  $i_{eq}$  at the input instead of splitting at the actual location as shown in Fig.3. After nodal analysis with the equivalent input noise current source at  $V_{in}$  node in Fig.3,  $V_{out}$  can be obtained as follows.

$$V_{out} = i_{eq} R_f \times \frac{1}{1 + j\omega \frac{(C_z + g_m r_{ds2} C_{gd}) R_f}{g_m r_{ds2}}} \quad (5)$$

From Equations (4) and (5)

$$i_{eq} = \frac{1}{g_m R_f} \times (1 + j\omega(C_z + C_{gd})R_f) i_c + i_r \quad (6)$$

Therefore, the mean square value of the input noise is given by

$$\overline{i_{eq}^2} = \omega^2 \times \frac{[C_{gs} + C_{gd} + C_s + C_{photo}]^2}{g_m^2} \times \overline{i_n^2} + \overline{i_r^2} \cong \omega^2 \times \frac{[C_{gs} + C_{gd} + C_s + C_{photo}]^2}{g_m^2} \times \overline{i_n^2} \quad (7)$$

for high  $\omega$ .

From Equations (3) and (7)

$$\overline{i_{eq}^2} = \omega^2 \times \frac{[C_{gs} + C_{gd} + C_{IN}]^2}{g_m^2} \times 4kTB(2/3)g_m \quad (8)$$

The parameters that can be controlled by designer in

Equation (8) are  $C_{gs}$  and  $C_{gd}$ .  $\overline{i_{eq}^2}$  becomes minimum when  $C_{gs} + C_{gd} = C_{IN}$ . Therefore it is clear that input transistor size is determined by the photodiode and stray capacitance to minimize the input noise which may appears as a large noise signal at the output.

## 5 Simulation and Fabrication Result

Because the circuit should be stable over temperature, power supply, and process variations, an extensive simulation has been performed before fabrication for entire process corners with back annotation data. The optical receiver has been implemented using a standard  $0.8\mu\text{m}$  CMOS standard process technology. The microphotograph of the receiver is shown in Fig.4

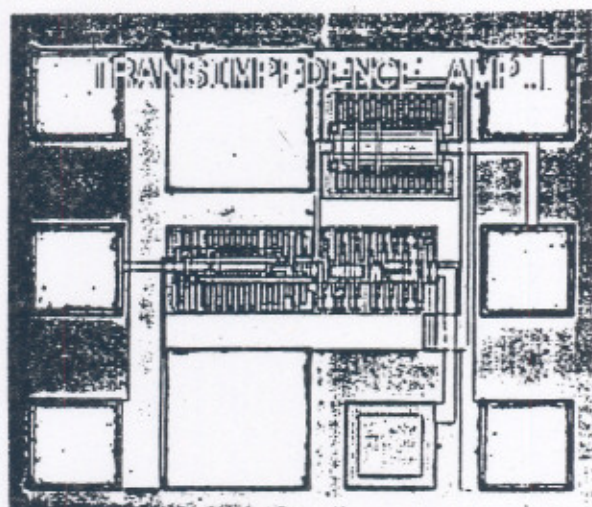


Fig.4 Microphotograph of the optical receiver

The chip size is  $0.3 \times 0.25 \text{mm}^2$ , and it dissipates  $9.3 \text{mW}$  power with  $5 \text{V}$  single power supply. The chip characteristics are shown in Table 1.

Power supply	5V
Power dissipation	9.3mW
Process	$0.8\mu\text{m}$ CMOS
Die size	$0.3 \text{mm} \times 0.25 \text{mm}$
Maximum bit-rate	450-Mb/sec
Input dynamic range	$30\mu\text{A}$ $100\mu\text{A}$

Table 1. Chip characteristics

Type	LT022PD0
Output power	3.0mW
Threshold current	44.4mA
Efficiency	0.31mW/mA
Operating current	52.4mA

Table 2. Laser diode characteristic

In order to measure the performance of the receiver with optical signal, a laser diode was connected to the input of the circuit as a photodetector. Table 2 shows the characteristic of laser diode used as a photodiode. The power of the laser source was less than 1mW. The optical receiver responded to the wide input dynamic range, which is between  $30\mu\text{A}$  and  $100\mu\text{A}$ . The optical receiver has to be carefully tested due to the stability problem at high frequency, which is caused by parasitic capacitance and inductances at bonding wire and pad area. Fig.5 shows the transimpedance vs. frequency characteristic of the CMOS optical receiver. The maximum transimpedance of the receiver is  $50\text{K}\Omega$ . Fig.6 shows output response with  $30\mu\text{A}$  input photocurrent at 450MHz.

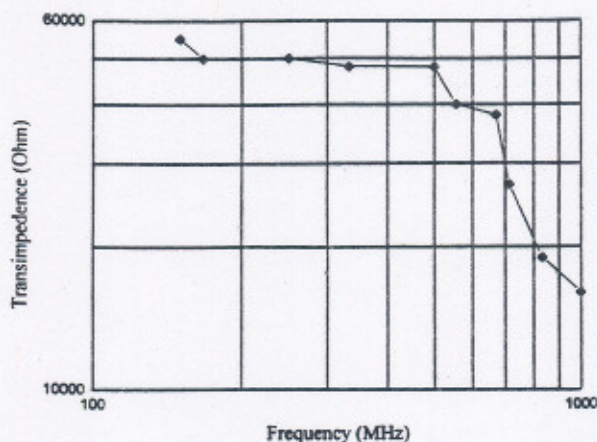


Fig.5 Transimpedance vs. frequency

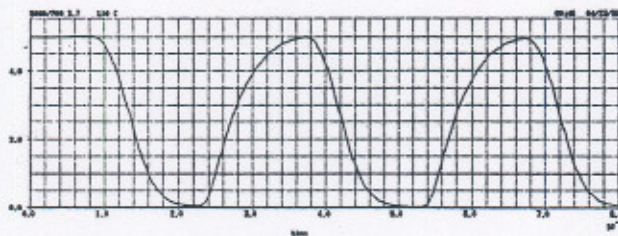


Fig.6 Output response with  $30\mu\text{A}$  input current at 450MHz

## 6 Conclusion

A fully CMOS compatible optical receiver has been developed using  $0.8\mu\text{m}$  CMOS process technology. Wide input dynamic range has been obtained using Automatic Gain Control. This paper demonstrates the potential of optical signal distribution such as clock

distribution in ULSI or memory/logic merged technology applied systems. The speed of the optical receiver can go even higher if the stability of the input stage is improved. More careful layout and stability consideration are required to improve the maximum bit-rate and effective test.

## References

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