A Novel Hardened Design of a Memory Cell in Nanoscale CMOS

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Abstract— **The aggressive scaling of CMOS into the deep submicron/nano ranges has resulted in an increased sensitivity to externally induced phenomena such as soft errors. Tolerance to soft errors, however, must be met while retaining high static stability, low delay, and a low power supply in circuit operation. This paper proposes a new design for hardening CMOS memory cell at the nano feature size of 32nm. By separating the circuitry for the write and read operations, the static stability of the proposed cell configuration increase more than 4.4 times and 5 times at typical and slow process corners, respectively compared to the previous designs. Simulation shows that by appropriately sizing the pull-down transistors, the proposed cell results in a 40% higher critical charge and 13% less delay than the conventional design. Moreover, the proposed hardened cell is less susceptible to process and random variations. Simulation results are provided using the predictive technology file for 32nm feature size in CMOS to show that the proposed hardened memory cell is best suited when designing memories for both high performance and soft error tolerance.**

Index Terms—**Radiation hardening, Memory design, Storage cell, Nanotechnology**

I. Introduction

ADvances in nanotechnology have made it possible to achieve an extremely high density in integrated circuit integration. The design of nanoscale circuits has, however, been affected by the deterioration of many performance metrics such as power and delay. Compared to the submicron technology, manufacturing and operation of these electronic circuits have been characterized by higher leakage current, lower gain, and a higher sensitivity to process variations. Today 45nm technology is already used and 32 nm will be reached in the next few years. However, the aggressive scaling of CMOS technology must also consider reliable operation with respect to externally induced phenomena such as cosmic ray neutrons and α-particles [1]. Due to the lower supply voltage and the smaller capacitance, the amount of charge stored on a circuit node is increasingly smaller, thus energy particles travelling through the silicon bulk can create minority carriers. These carriers may be collected by the source/drain diffusion and alter the voltage value of the nodes [2]. When affected by particle strikes, storage cells such as memories and latches lose data often resulting in a system failure. Therefore, this type of event may result in transient faults (TFs). If a TF is latched by a sampling element (latch), then a so-called soft error (SE) is said to occur [3]. The soft error rate (SER) is defined as the rate at which SEs are encountered on a predictive basis. The SER is expected to increase as feature size decreases, and it is very important to have design solutions for CMOS in the deep submicron/nano ranges for tolerating soft errors [4]. A large area of today’s chips (such as microprocessors) is occupied by embedded memories whose correct operation relies on data integrity. Hence, memories must be protected against SEs and TFs at a relatively low cost. Traditional techniques such as error detecting/correcting codes [5] can be used to protect the memories against SEs and TFs. The cost in terms of speed and power for protecting memories from TFs causing errors can be significant if only error detection/correction codes are utilized. Therefore, to preserve data integrity against TFs, new design techniques must be employed for storage elements. Among them, hardening has been proposed as a low-cost design solution for tolerating SEs [6] - [10]. Hardening techniques can be classified into two broad categories [10]. In the first approach, the storage cells are designed to be insensitive to TFs independently of the circuit electrical parameters such as sizing of the transistors and the capacitance of the nodes of a cell. This type of approach has the advantage of technology independence and possibly can be used at nano realm as well, but it may cause a significant design overhead due to the additional circuitry. In the second category, hardening is achieved by increasing the capacitance of critical nodes as well as the strength of the transistors. Such approaches must be scaled with the feature size of the employed technology and may result in unwanted penalties with respect to performance (i.e. an increase in delay), low stability, and high power dissipation [22].

An example of an approach in the first category has been reported in [6] and is commonly known as DICE. As shown in Fig.1, the DICE cell uses twice the number of transistors of the standard 6T memory cell to achieve a good immunity against TFs affecting any single node. It does not require sizing of the transistors and increasing the capacitance of some nodes. In a DICE cell, the node that is affected by a TF can be driven back to its previous state by other transistors due to the presence of a feedback path. For the second category of hardening designs, capacitors in SRAM cells can be utilized to absorb the excess

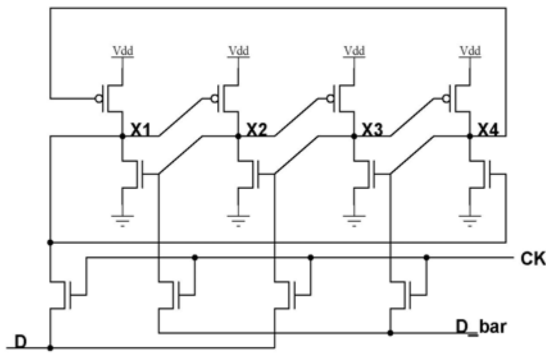

Figure 1. DICE cell proposed in [6]

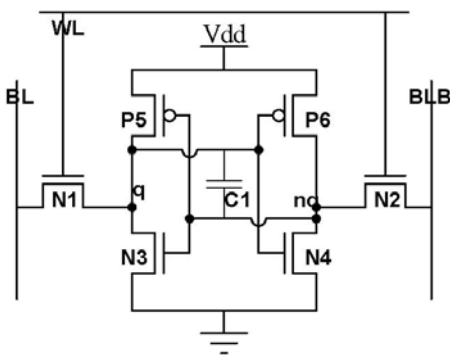

Figure 2. Hardened SRAM cell by using a capacitor (SRAM-C cell)

charge [11] [15]. A possible implementation of such an approach is shown in Fig.2. While error tolerance must be achieved, any performance metrics such as power delay product and stability should not be sacrificed.

The objective of this paper is to propose a new memory cell configuration which is applicable to CMOS at the nano range of 32nm. Using the technique of [15], the new hardened cell overcomes the problems of the previous design [15] by using additional read access transistors. Since this hardened configuration utilizes 14 transistors, optimum transistor sizing is required for proper operation as well as reducing area overhead. In this paper several different arrangements are proposed, and the pull-down transistors' size are reduced to half of the original size in the best sizing arrangement case for the pull-down transistors at only a 7% increase in layout (compared to a previous design [15]). Simulation results are provided to show the stability improvement of the proposed hardened memory design. The proposed circuit of a memory cell is also superior in terms of the critical charge, performance, and sensitivity to process variations (systematic and random) at 32nm feature size by utilizing its predictive technology file.

II. Soft Error Modeling

Dynamic stability of a memory is usually established by performing noise analysis on the cell in the presence of the soft errors. Soft errors occur when the collected energy Q at a particular node is greater than the critical charge, Q_{crit}. Q_{crit} is defined as the minimum charge that needs to be deposited at the sensitive node of a storage cell to change (flip) the stored bit. In the model proposed in [12] [13], the SER (Soft Error Rate) is given by:

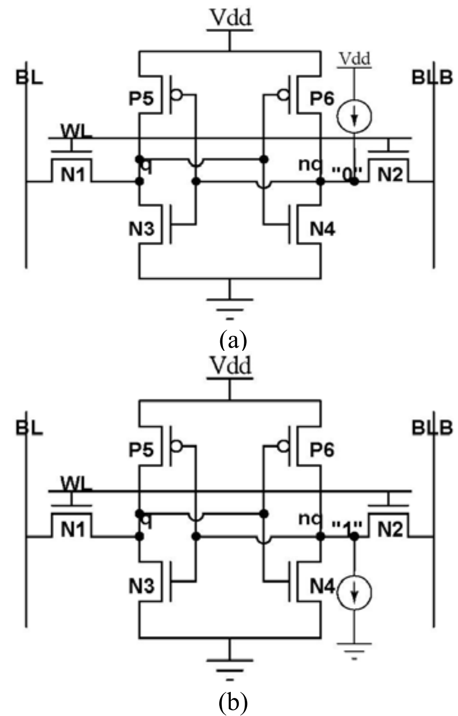

Figure 3. Equivalent circuits used for simulation of (a) positive and (b) negative glitches in a 6T SRAM cell

$$SER \propto N_{flux} \times CS \times e^{\frac{-Q_{crit}}{Q_s}} . \qquad (1)$$

N_{flux} is the intensity of the neutron flux, CS is the area of the cross section of the node, and Q_s is the charge collection efficiency (that strongly depends on doping). Q_{crit} is proportional to the node capacitance and the supply voltage. In Equation (1), Q_{crit} exhibits an exponential relationship with the soft error rate, and Q_{crit} has been widely used as metric for assessing the possible occurrence and tolerance to soft errors. The charges due to cosmic ray neutrons or α-particles at some node generate a large transient current at that node. Therefore, a critical charge generated on some node can be modeled as a current pulse for HSPICE simulation.

Fig. 3 shows the model for soft error occurrence in a unhardened 6T SRAM cell, which is used in this paper for simulation by HSPICE. In this figure, soft errors resulting in a signal glitch occur on the node 'nq'. Fig.3 (a) shows the case in which the SRAM cell stores a "1" and soft errors occurring at node 'nq' generate a positive pulse, whereas Fig.3 (b) shows the case where the SRAM cell stores a "0" and soft errors occurring at the node 'nq' generate a negative pulse. If it is also assumed that the duration time of the transient pulse is 0.1ns, then the current source in Fig. 3 is also turned on for 0.1ns.

As reported in [13], the critical charge, Q_{crit}, is estimated

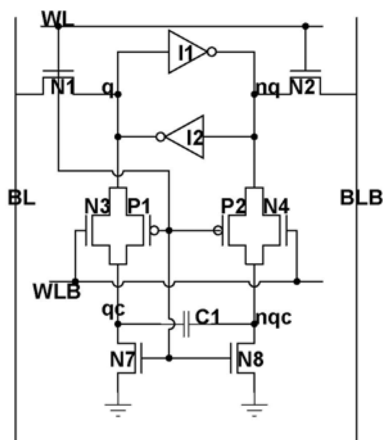

Figure 4. Hardened memory configuration of [15] (TCT cell)

only at specific nodes having a low value of Q_{crit} [13]. These nodes are usually experimentally identified. It is important to note that the PMOS transistors in a 6T SRAM cell are always used as load and very weak for fast write and low area. Therefore, the capability of the 6T SRAM cell to restore from a positive strike is stronger than its capability to restore from a negative strike due to the strong pull down NMOS. In this paper, the critical charge of the 6T SRAM cell implies the critical charge when there is a negative glitch on node 'nq' as shown in Fig.3.b.

III. Existing Hardening Approaches

As mentioned in the previous section, design approaches for hardening can be classified into two categories [10]. An example of the first category design is the DICE cell shown in Fig.1. In the second category, hardening is achieved in the design by increasing the capacitance of some nodes or the strength of the transistors. For the second category of hardened designs, additional capacitors are utilized to protect storage cells from TFs [15]. Fig.4 shows the basic cell for the hardening approach proposed in [15]. The cell consists of a regular SRAM configuration with addition of the two CMOS transistors connected in series with two NMOS transistors and a vertically stacked capacitor. In standby mode, the capacitor C1 is connected to the SRAM cell and acts as a charge buffer, which is similar to the configuration shown in Fig.2. Simulation results have shown that the critical charge of the SRAM improves significantly due to the capacitor attached to the storage node. When a 3fF capacitor C1 is connected to the storage node, an increase in critical charge from 2.13fC to 3.02fC is observed at 32nm feature size typical process corner, room temperature and 0.9V power supply. During the write or read mode, the capacitor is removed from the back to back inverter and transistors N7 and N8 discharge the capacitor. Therefore, the circuit speed is retained due to the removal of the capacitor during read and writes operations. However, this SRAM cell suffers from the read disturb problem. The Static Noise Margin (SNM) of the SRAM cell is small during the read

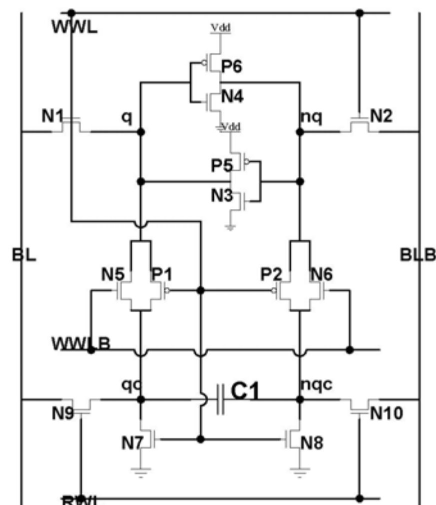

Figure 5. Proposed hardened memory cell

operation, thus limiting its application at deep submicron/nano scales in which a low power supply is employed in designs. Therefore a modified hardened design for a nanoscale memory configuration is proposed in the next section to overcome these issues.

IV. Proposed Hardened Memory Cell

The stability of SRAM cell is usually measured by the SNM (the SNM is defined as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit [17]). The conventional 6T SRAM cell has been found to be rather unstable in deep submicron/nano scale technology. This cell fails to meet the operational requirements due to low read SNM. When the conventional SRAM cell is in the read operation, the pass gate is turned on and pulls the node that stores the logic "0" (for example, the node identified by 'nq' in Fig.3.a) to a non-zero value. This decreases the read SNM, especially when a low power supply voltage is utilized. The hardened memory cell shown in Fig.4 suffers from the so-called read-disturb problem and is rather unstable during read operation. This memory cell achieves high performance and dynamic stability by connecting the capacitor C1 to the storage node during the standby mode and disconnecting the capacitor from the circuit during the operational mode. However, it shows a very low SNM during read operation like the conventional 6T SRAM cell. Therefore, the data stored in the memory cell is very vulnerable to external noise during the read operation.

The proposed hardened memory cell (14T) is shown in Fig.5. In this configuration, transistors N9 and N10 are added to the memory cell as access transistors to separate the read and write operations. During read operation, RWL is high, the data stored on nodes 'qc' and 'nqc' (the data on node 'qc' and 'nqc' are the same as the data stored on node 'q' and 'nq') are read to the bitlines such that the read operation is fast. Meanwhile, when

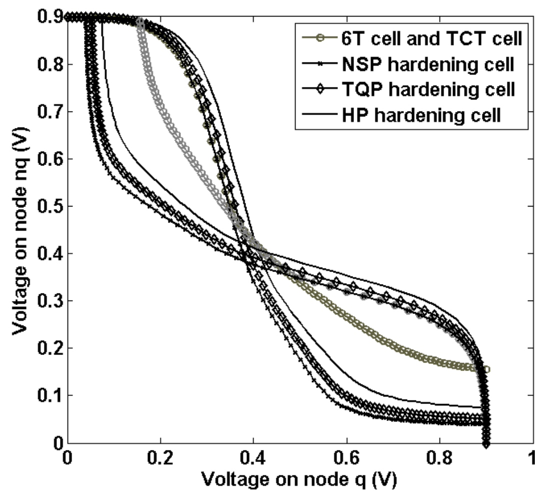

Figure 6. SNMs of SRAM cells

RWL is high and WWLB is high, the stack effect alleviates the read disturb problem on node ‘q’ or ‘nq’, thus a large read SNM is achieved in this memory cell. The proposed hardened memory retains a high dynamic stability in terms of critical charge (3.13fC at room temperature and 0.9V power supply), it also achieves high static stability in terms of SNM, i.e. 250mV at room temperature and 0.9V power supply, compared to a SNM of 88.3mV for the hardened cell of Fig. 4.

For a high density memory design, the SRAM cell should be sized as small as possible. On the other hand, a sizing constraint should be applied to the conventional 6T SRAM cell, for correct operation, and the pull-down to pass gate transistor ratio must be greater than 1.2 to avoid the read-disturb problem [18]. However, for the proposed memory cell of Fig.5, the size of the pull-down transistors (N3 and N4 in Fig.5) can be scaled down as the read and write operations have been separated. Scaling down the pull-down transistors not only improves performance (fast write), but it also reduces the overhead due to the additional transistors of the proposed hardened cell. In this paper, a pull-down transistor is reduced to either three-quarter of its original size (yielding so-called TQP cell) or half of its original size (yielding so-called HP cell). The effect of sizing of the transistors on the performance of the memory cell can then be assessed. Fig.6 shows the SNM of the conventional 6T SRAM cell, the hardened memory cell in Fig.4 (denoted as the TCT cell as in [15]), the proposed hardened memory cell without pull-down transistor scaling (NSP cell), the TQP hardened cell, and the HP hardened cell. It is shown in Fig.6 that the hardened cell of Fig.5 achieves a significantly larger SNM compared to the 6T cell and the hardened cell [15] of Fig.4 due to the stack effect. It is also shown in Fig.6 that scaling down the pull-down transistor shows little effect on the SNM of the 14T memory cell. This is a positive feature that will be used in the next section to reduce the area overhead in layout of the memory cell.

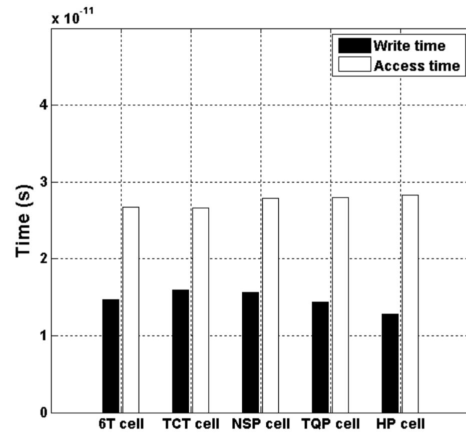

Figure 7. Write time and access time of SRAM cells

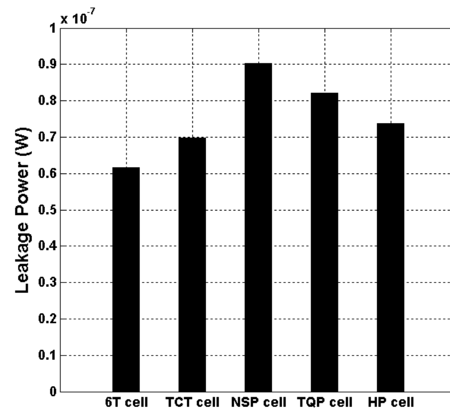

Figure 8. Leakage power of SRAM cells

V. TRANSISTOR SIZING

HSPICE simulation has been performed on the conventional 6T SRAM cell, the hardened cell of Fig.4 (denoted as the TCT cell as in [15]), the proposed hardened cell of Fig.5 without scaling (NSP cell), the TQP hardened cell, and the HP hardened cell to investigate their performance using the Berkeley Predictive Technology Model (PTM) at 32nm [19].

For the 6T SRAM cell shown in Fig.2, the transistor widths $W_{P5}/W_{N1}/W_{N3}$ are 80/120/160nm. For the TCT cell, the transistor dimensions of the access transistors and cross-coupled inverter are the same as the 6T SRAM cell, and minimum transistor widths (40nm) are used for all other transistors. The transistors of the NSP cell are the same as in the TCT cell with two additional read access transistors of 120nm width. The transistor widths of N3 and N4 in the TQP cell are 120nm while 60nm is used for the TCT cell and the NSP cell. Similarly, the transistor widths of N3 and N4 in the HP cell are 80nm.

The simulation results on the write/access times and the leakage power of these SRAM cells are plotted in Fig.7 and Fig.8. Due to the additional transistors, writing speed of the TCT and the NSP cells is slower than for the 6T SRAM cell. However, as the write and read operations are separated in the

TABLE I.
CRITICAL CHARGE, SNM, AND PERFORMANCE COMPARISON OF DIFFERENT MEMORY CELLS AT 0.9V POWER SUPPLY AND ROOM TEMPERATURE

Memory Cell Type	Critical Charge	SNM	Write Delay
Unhardened 6T memory cell	2.13 fC	88.3 mV	14.66 ps
SRAM-C cell (C=3ff)	3.74 fC	88.3 mV	44.12 ps
TCT cell (C=3ff)	3.12 fC	88.3 mV	15.94 ps
NSP cell (C=3ff)	3.16 fC	250 mV	15.69 ps
HP cell (C=3ff)	3.02 fC	212.5 mV	12.81 ps

NSP cell, the pull-down transistors are scaled down for fast write operation. The simulation results in Fig.7 show that the TQP and HP cells achieve 2% and 13% writing time improvements. It is also shown in Fig.7 that all five cells have almost the same access time due to the similar read scheme. The leakage powers of the 6T cell, the TCT cell, the NSP cell, the TQP cell, and the HP cell are plotted in Fig.8. Due to the two additional read access transistors (N9 and N10), the leakage power of the proposed hardened cell of Fig.5 (NSP cell) is 46% higher than the 6T cell. However with pull-down transistor scaling, the leakage power of the TQP and HP cells is reduced significantly. The leakage power of the HP cell is 19% higher than the 6T SRAM cell and 5% higher than the TCT cell. Simulation results show that the HP cell improves performance and power consumption of the proposed hardened cell compared to the NSP cell. Therefore, the HP cell has the best transistor sizing for the proposed memory cell of Fig.5.

Critical charge is often used as a metric for hardened memory designs [15] [22]. In the TCT cell, the NSP cell and the HP cell, the critical node (i.e. the node with the smallest critical charge) is the same as the unhardened 6T cell, i.e. node ‘q’ or ‘nq’ in Fig.4 and Fig.5. Table 1 summarizes the critical charge, SNM, and the write delay of the 6T memory cell, the SRAM-C cell in Fig.2, the TCT cell in Fig.4, the NSP cell and the HP cell in Fig.5. Compared to the unhardened 6T memory cell, the SRAM-C cell achieves the best critical charge, but it suffers from a low SNM and a very slow write delay. The TCT cell in Fig.4 achieves a high critical charge and a fast write, but it shows a low SNM, which makes this cell very unstable at a low power supply. The proposed NSP and the HP cells have a high critical charge, a high SNM, and a fast write time (as shown in Table 1), thus making them good candidates for high-stable and low power memory designs. In Table 1 shows the SNM of the HP cell is still relatively higher than the 6T and TCT cells and the cell has a high critical charge and a faster write delay. Table 1 also confirms that the transistor sizing of the HP cell is best for the proposed hardened memory cell of Fig.5.

The layouts of the TCT and the HP cells (based on MOSIS deep sub-micrometer design rules [20]) are shown in Fig. 9. The area of the TCT cell is as twice as the traditional 6T SRAM

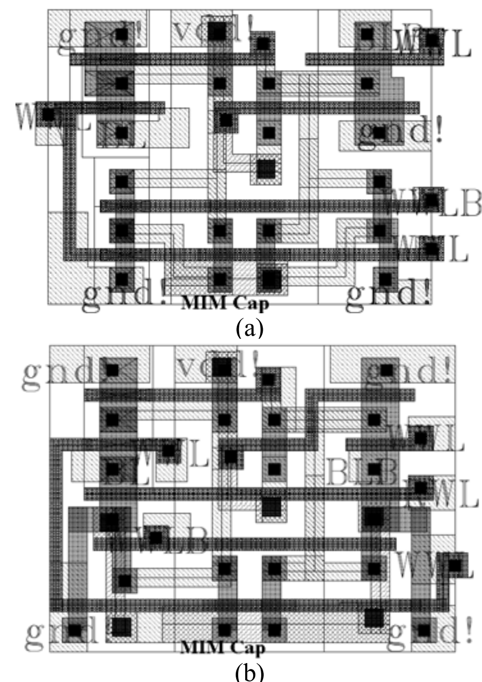

Figure 9. Layout of (a) TCT cell; and (b) HP cell

cell because of the additional six transistors. Two more transistors are added to the TCT cell[15]. The pull-down transistors’ sizes are, however, reduced yielding so-called HP cell. The layout of the HP cell is shown in Fig.9.b, and the area of the HP cell is only 7% larger than the TCT cell shown in Fig.9.a.

As shown in Fig.9, the additional capacitor can be implemented as a metal insulator metal (MIM) capacitor [21] on top of the SRAM cell as MIM capacitors are designed and realized at interconnect levels. A substantial area penalty will be incurred if its implementation is through a poly-diffusion capacitor. The capacitance density of the MIM capacitor is determined by the insulator material and thickness between two metal layers in the layout.

VI. CAPACITANCE AND PROCESS VARIATIONS

For the proposed hardened memory cell in Fig.5, the capacitor C1 is disconnected from the cross-coupled inverter during the write operation. An increase in the capacitance of C1 has a negligible effect on performance. However, an increase in the capacitance of C1 can have a significant effect on the critical charge. When the capacitance of C1 is 2ff, the critical charge is 2.66fC while the critical charge is 2.13fC for the 6T SRAM cell.

Fig.10 shows that the critical charge of the HP cell increases almost linearly as the capacitance of C1 increases. Simulation has also confirmed that there is no performance degradation when the capacitance of C1 increases. Therefore, the capacitance of C1 can be increased for high critical charge (hence better tolerance to soft errors) depending on the area that is allowed for implementing the capacitor.

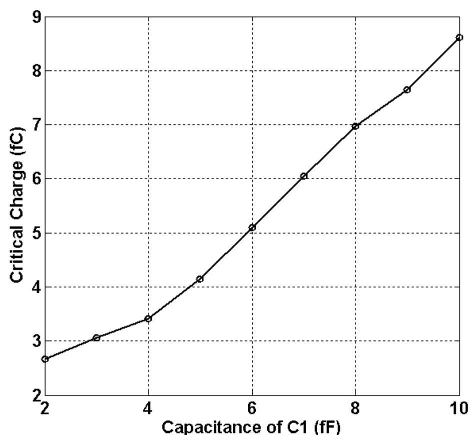

Figure 10. Capacitance vs critical charge plot of HP cell

Systematic and random variations in process and temperature are posing a major challenge for nanoscale CMOS integrated circuit design. Systematic variations (such as temperature variations) have strong impact on the critical charge of the 6T SRAM cell because both junction capacitance and electron mobility have large temperature coefficients. Fig.11 shows that the critical charge of the 6T cell decreases when the temperature increases. For the proposed cell configuration, this is dependent on the implementation of the capacitor.

In CMOS technology, bottom and top plate capacitors are usually implemented by two metal layers or ploy to ploy because they have a lower temperature coefficient. Fig.11 plots the critical charges of the SRAM-C cell of Fig.2 and the proposed hardened cell of Fig.5 with capacitors of 3fF and 5fF. As shown in Fig.11, the critical charge of the SRAM-C cell also decreases as the temperature increases, albeit at a slower rate compared to the 6T SRAM cell. For the proposed HP cell, the change in the critical charge due to temperature variation is significantly smaller. During standby mode, the HP cell operates as a SRAM-C cell, i.e. transistors N5, N6, P1, and P2

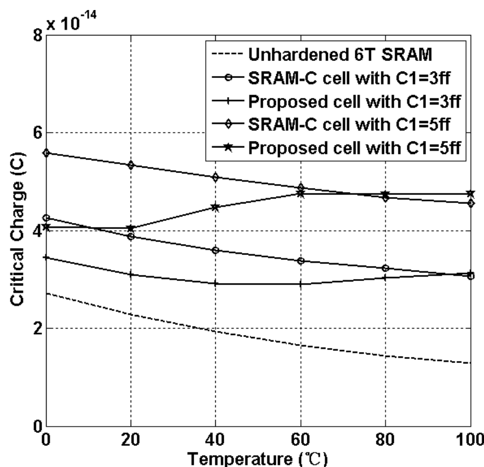

Figure 11. Temperature vs critical charge plot of SRAM cells

TABLE II.
PROCESS VARIATIONS IMPACT ON CELL STABILITY

Memory Cell Type	Critical Charge (fC)			SNM (mV)		
Process Corner	Typical	Fast	Slow	Typical	Fast	Slow
6T memory cell	2.13	2.82	1.60	88.3	145.5	35.4
TCT cell (C=3ff)	3.16	3.82	2.91	88.3	145.5	35.4
HP cell (C=3ff)	3.02	3.58	2.79	212.5	275.7	176.6

are on. Compared to the SRAM-C cell, when the temperature is low, the currents through transistors N5, N6, P1, and P2 in Fig.5 are low in short channel devices. Therefore, the connection between nodes ‘qc’ and ‘q’, and ‘nqc’ and ‘nq’ are weak, and the ability of absorbing an additional charge is weak. This makes the critical charge of the HP cell at low temperature smaller than for the SRAM-C cell. As temperature increases, the currents through transistors N5, N6, P1, and P2 increase, and the ability of absorbing an additional charge becomes stronger. Therefore, the critical charge of the HP cell is almost the same as the SRAM-C cell.

Random process variations are a serious concern due to uncertainty in the device and interconnect characteristics. Process variations negatively impact both static and dynamic stability of traditional SRAM designs. Table 2 shows the HSPICE simulation results on the dynamic and static stability of the 6T and HP memory cells in terms of the critical charge and SNM. The unhardened 6T SRAM cell is very unstable in terms of SNM and it has a low critical charge at the slow process corner. The TCT cell of [15] has the highest critical charge, but a very low SNM. By using the proposed high-stable design, the memory cell retains a relatively high SNM and critical charge even at a slow corner. Therefore, the proposed HP cell is less sensitive in the nanoscale regimes to process variations.

VII. CONCLUSION

This paper has presented a new design for a highly stable hardened memory cell in CMOS at 32nm feature size. A novel cell configuration has been proposed, analyzed, and simulated using the predictive technology for tolerance to soft errors. The proposed new hardened memory cell relies on connecting a capacitor to the storage node during the standby mode and disconnecting the capacitor during the write operation. Two additional read access transistors are added to the cell to overcome the stability problem encountered in [15]. As a high stability is achieved by separating read and write operations, the transistors in the proposed hardened memory cell can be resized to optimize power and performance. Simulation results shows that the half pull-down transistor scaling (HP cell) is the best transistor sizing for the proposed hardened memory cell at only a 7% increase in layout area.

Using HSPICE, simulation results have confirmed that the proposed memory cell accomplishes a higher critical charge compared to the 6T configuration and no performance is lost when the capacitance is increased to improve dynamic stability. The impact of process and temperature variations on the critical charge of the proposed hardening cell has been analyzed. It has been shown that the proposed hardened cell is very stable even in the presence of process and temperature variations. Consequently, the proposed hardened memory cell is preferable when designing memories for both high stability and performance.

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