

NEED FOR UNDERGRADUATE AND GRADUATE-LEVEL EDUCATION IN TESTING OF MICROELECTRONIC CIRCUITS AND SYSTEMS

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ABSTRACT

As deep-sub-micron and beyond technology emerges, quality assurance of microelectronic circuits and systems becomes more important than ever. Consequentially, (1) a strong need for well-educated microelectronic circuits and systems test engineers is desired by the industry, (2) graduate-level research efforts are also called to overcome numerous microelectronic circuits and systems test issues. This paper is to address issues related to increasing impact of the electronic circuits and systems test field on education in electrical and computer engineering and to propose suitable educational topics for undergraduate and graduate-level electrical and computer engineering courses.

1. INTRODUCTION

As deep-sub-micron and beyond technology emerges, test education of microelectronic circuits and systems becomes more important than ever [1, 2, 4, 5, 6]. The ITRS2002 (International Technology Roadmap for Semiconductors 2002) has numerous technology forecasts for chip characteristics and includes a number of sections regarding test [3]. Several of the forecasts have major impact on test education and research. For instance, chip gate count is projected to increase by approximately 30% per year and on-chip clock speed increases dramatically while the ATE (Automated Test Equipment) capability and test engineers' quality do not. Thus, current trend implies increasing yield loss due to imperfect test judgement.

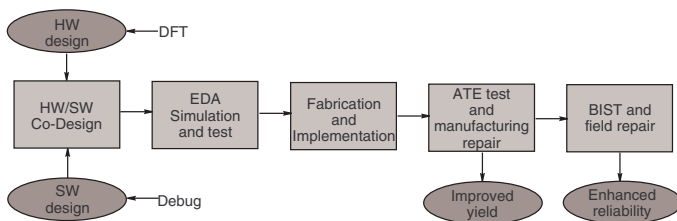


Figure 1. Design and test procedure for today's microelectronic systems

Today's microelectronic circuits and systems design and implementation cannot be done without conducting proper test procedure as shown in Figure 1. In the following, test steps at different design and implementation stages of microelectronic circuits and systems are summarized.

- The system under development is usually designed with

conjunction with test and this design methodology is commonly referred to as the *DFT* (Design For Testability).

- The SW subsystem is also co-designed and debugged for synergistic testability.
- Then, EDA tools are commonly used to perform behavioral and functional testing of the system under development.
- Since majority of defects and associated faults are usually incurred by imperfect manufacturing, not erroneous design, ATE (Automated Test Equipment) is then employed to test the fabricated system.
- To further enhance the reliability of the system, BIST (Built-In Self-Test) circuits are commonly embedded into the system at the DFT-level. Thus, the system can be tested and possibly repaired in the field for improved longevity.

Although there is a strong need for test education and research, both undergraduate and graduate-level courses of today usually do not properly address the test issues. In this paper, thus, we address issues related to increasing impact of the electronic circuits and systems test field on education in electrical and computer engineering and propose suitable educational topics for undergraduate and graduate-level electrical and computer engineering courses.

2. TEST EDUCATION AREAS FOR UNDERGRADUATE-LEVEL COURSES

In the following, the topics identified as suitable for undergraduate courses are listed.

1. Early design space exploration and utilization techniques
 - (a) Design for Testability (DFT) and reparability
 - Probing-point allocation at the gate level
 - Synthesis of scan chains (both partial and full), and integration of scan functionality into application-specific design [1]
 - (b) Built In Self Test (BIST), Diagnosis (BISD) and Repair (BISR)
 - BIST pattern generators for combinational and full-scan circuits
 - Synthesis for pseudo-random pattern testability
 - Memory BIST (i.e., march algorithms and redundancy reconfiguration)
 - (c) Test pattern generation and fault simulation

- For combinational circuits
 - For sequential circuits
 - Memory testing based on functional fault models
 - Combinational vector compaction
- (d) I_{DDQ} testing (Current-based testing)
- Single pass/fail threshold I_{DDQ} testing
 - Built-in current sensors (BICSs)
- (e) Synthesis for test and repair
- Redundancy reduction in combinational circuits

2. Debug, diagnosis and failure analysis

- Diagnosis which uses a single fault assumption from any of the legacy models (i.e., stuck-at fault model and poisson fault model)

3. TEST EDUCATION AND RESEARCH AREAS FOR GRADUATE-LEVEL COURSES

In the following, the areas identified as emerging, divided into seven main topics, are shown.

1. Defect and fault mechanisms and modeling

- Deep submicron and nano-scale defect issues
- Classifications/detection/repair of manufacturing defects and performance problems in embedded arrays including DRAM, SRAM and CAM.
- Defect and fault type identification, extraction, abstraction and modeling.
- High-level fault models (at the RTL and above) and low level fault models mapping.

2. Diagnosis, verification and failure analysis

- Diagnosis of failures due to defects discussed above.
- Fault diagnosis with BIST and design for BIST diagnosability.
- Diagnosis of reconfigurable architectures with FPGAs.
- Diagnosis of memories with redundancies.
- Design verification.

3. System performance testing

- High speed/frequency test. On-chip clock rates are reaching beyond 2GHz. Testing in such chips is challenging.
- Delay test in multi-clock designs (synchronized or not), including on-chip generated clocks.
- Delay testing incorporating interconnect, including both coupling capacitance and supply line effects and resistive bridges for multiple levels of metal.

4. Design methodologies: In addition to the topics for undergraduate education, the following topics may also be suitable for graduate education.

- (a) For circuits with primitives other than gates, such as tri-state elements
- (b) For asynchronous circuits
- (c) For analog and mixed signal circuits
- (d) Design for testability

- High-level design testability for SoC and embedded cores
 - For high-performance circuits
- (e) BIST
- For SoC and embedded cores
 - For sequential circuits
 - At-speed BIST
 - For high-performance circuits
- (f) Synthesis for testability
- Redundancy identification and removal for sequential circuits
 - Identification of false paths in combinational and sequential circuits
 - Circuit transformations to enhance testability
- (g) On-line testing
- System-level on-line testing

5. Test pattern generation

- At the RTL and above
- For high-performance circuits
- For circuits with primitives other than gates, such as tri-state elements
- For analog and mixed-signal circuits
- For asynchronous circuits

6. ATE and measurement issues

- High performance ATE architectures and requirements. Application of signals on chips with higher accuracy. ATE OTA (Operational Transconductance Amplifier) issues (i.e., accuracy assurance of waveform measurements).

7. Analog and mixed signal testing including MEMS and sensor technologies

Since design and test for microelectronic circuits and systems always come together, it is desirable to address test topics in existing design courses for a week or two. Small project and lab can be also given for in-depth education.

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