A Low Power 32 Nanometer CMOS Digitally Controlled Oscillator

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ABSTRACT

In this paper, a low power and low jitter 12-bit CMOS digitally controlled oscillator (DCO) design is presented. The CMOS DCO design is based on a ring oscillator implemented with Schmitt trigger based inverters. Simulations of the proposed DCO using 32nm Predictive Transistor Model (PTM) achieve controllable frequency range of around 570MHz~850MHz with a wide range of linearity. Monte Carlo simulation demonstrates that the time-period jitter due to random power supply fluctuation is under 75ps and the power consumption is 2.3mW at 800MHz and 0.9 power supply.

I. INTRODUCTION

Over the past two decades, the operating clock frequency of the modern VLSI circuits such as microprocessors and digital signal processors have increased greatly to the order of a few GHz. The corresponding increase in the number of operations that can be performed over time by the VLSI circuit have provided dramatic increase in the functionality of electronic computing systems such as laptops, cell phones, and so on. In order to provide such high performance circuits, the function blocks such as clock recovery and clock generator must operate at the same high frequencies.

In high-speed VLSI systems, clock is practically generated by an analog phase-locked loop. Typical analog PLLs include a phase-frequency detector, a charge pump, a loop filter, a voltage controlled or current controlled oscillator, and a frequency divider [1,2]. The controlled oscillator is the key component in the core of PLL. Recently, efforts have been made toward the development of fully digital PLLs. Compared to their analog counterparts, fully digital PLLs exhibit better noise immunity and they are invulnerable to DC offset and drift phenomena [3,4]. The digitally controlled oscillator (DCO) is a replacement of the conventional voltage or current controlled oscillator in the fully digital PLLs. They are more flexible and usually more robust than the conventional VCO compared to their analog counter parts. Furthermore, the design compromise for the frequency gain in voltage or current controlled oscillator is not necessary in DCOs because the immunity of their control input is very high.

There are two main techniques for the DCO design as shown in Fig. 1. One technique changes the driving strength dynamically using the fixed capacitance loading [5,6] while the other uses shunt capacitor technique to tune the capacitance loading [7]. Although they both have a good linear frequency response and a reasonable frequency operating range, the power dissipation hasn't been taken into consideration. Moreover, for the DCO design, there is a tradeoff between the operating range and the maximum frequency that DCO can achieve. As a result, the increase of the operating range by adding more capacitance loading will result in a lower maximum frequency and higher power consumption. Since power consumption is of extreme concern for the portable battery charged computing systems, the reduction of the power consumption has become a major concern.

This paper proposes a novel DCO circuit with reduced power consumption using binary controlled pass transistors and Schmitt trigger. The DCO is designed using the 32nm CMOS Predictive Transistor Model (PTM).

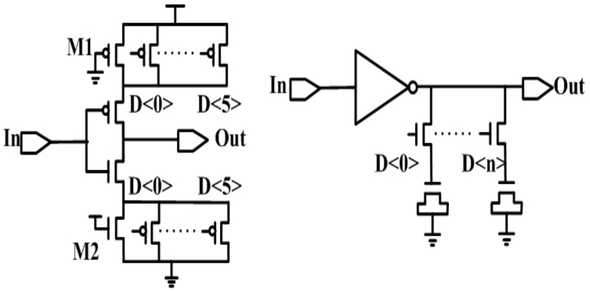


Figure 1: Standard Cell of Digitally controlled oscillator. (a) Driving strength controlled. (b) Shunt capacitance controlled.

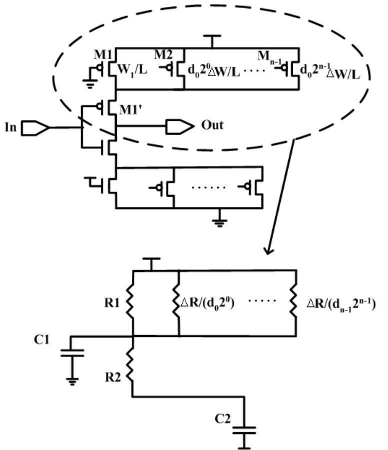


Figure 2. Equivalent circuit for the calculation of constant delay and delay tuning range.

II. DCO PRINCIPLE AND DESIGN

DCO should generate an oscillation period of T_{DCO}, which is a function of digital input word D given by

$$T_{DCO}=f(d_{n-1}2^{n-1}+d_{n-2}2^{n-2}+\cdots+d_1 2^1+d_0 2^0) \quad (1)$$

Typically, the DCO transfer function is defined such that the period of oscillation T_{DCO} is linearly proportional to D with an offset:

$$T_{DCO}=T_{offset}-D\cdot T_{step}, \quad \text{D: Digital Control Bits} \quad (2)$$

where T_{offset} is a constant offset period and T_{step} is the period of the quantization step. For the conventional driving strength controlled DCO shown in Fig. 2, the constant delay of each cell is calculated as follows:

$$T_{constant}=R_1(C_1+C_2)+R_2C_2 \quad (3)$$

$$R_{1,2}\propto W_{1,2} \quad (4)$$

where R_1, R_2 are the equivalent resistances of M1,M1'. Assuming they have the same driving strength, the delay tuning range of this standard cell is obtained as follows:

$$\frac{T_{tune}}{2}=(C_1+C_2)(R_1//\frac{\Delta R}{d_0}//\frac{\Delta R}{d_1 2}//\cdots//\frac{\Delta R}{d_{n-1}2^{n-1}})-(C_1+C_2)R_1 \quad (5)$$

$$=\frac{R_1(C_1+C_2)}{1+(D\cdot\Delta W)/W_1}-(C_1+C_2)R_1 \quad (6)$$

$$\approx R_1(C_1+C_2)\frac{D\cdot\Delta W}{W_1}, \quad \text{(Only if } \frac{D\cdot\Delta W}{W_1}<<1\text{)} \quad (7)$$

In order to have a good linear tuning range, the width of transistor M1 has to be increased as can be seen in Equation (7). Consequently, the equivalent resistance R_1 will decrease resulting in a smaller delay tuning range. One way to increase the tuning range while keeping the linear response is to increase the capacitance loading. However, this will reduce the maximum frequency that the DCO can accomplish and the power consumption will also be increased.

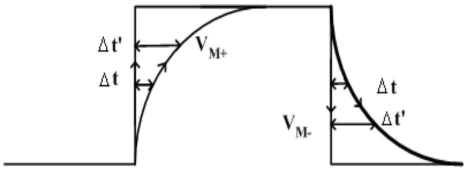


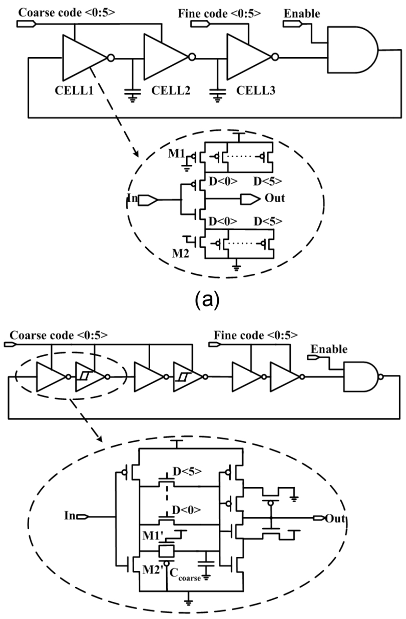
Figure 3. Delay comparison of Schmitt inverter and conventional inverter.

The proposed DCO employs a new approach to increase the delay tuning range using binary controlled pass transistor arrays and Schmitt trigger based inverters. The Schmitt trigger based inverter has a higher V_{M+} (low to high switching threshold) and lower V_{M-} (high to low switching threshold) compared to the conventional inverters as shown in Fig. 3. As a result, the proposed DCO circuit provides the same tuning range with smaller capacitance loading, which is beneficial for power consumption reduction. Moreover, in the conventional DCO circuit, the slope of the input signal to each stage decreases gradually due to the large delay between each stage. This results in not only a non-ideal rail-to-rail switch but also a poor power performance. The steep slope of the output signal from the Schmitt trigger based inverter minimizes this problem to a certain extend.

The circuit diagrams of the conventional DCO and proposed DCO are shown in Fig. 4. In order to compare the power consumption, both circuits are equally sized. Based on Equation 7, the minimum value of ΔW is required for large linear tuning range since T_{tune} is inversely proportional to the width of the pass transistor M1, M1', M2 and M2'. As a result, the binary controlled pass transistor array in the proposed DCO shown in Fig. 4b has the same sizing as the array in the lower half part of the conventional DCO shown in Fig. 4a with 6 control bits and the minimum device with of 32nm. The pass transistors M1', M2' are equally sized as M1, M2. Both DCO have two coarse delay cells, a fine delay cell, and a NOR gate for reset.

III. COMPARISON BETWEEN THE TWO DCO STRUCTURES

The proposed DCO and the conventional DCO are simulated and compared using 32nm CMOS



(a)

(b)

Figure 4. Digitally Controlled Oscillator. (a) Conventional DCO structure), (b) Proposed DCO structure

PTM (Predictive Transistor Model) with supply voltage of 0.9Volts. Table 1 shows the impact of each control bit on the period of the two DCO structures. Both structures have the same linear tuning range until the 5th bit is asserted. This is due to the fact that the requirement for the linear tuning range fails when $D\Delta W$ becomes too large comparing to W1. Although the decrease in the period of the proposed DCO becomes slower than that of the conventional DCO when the 5th bit is asserted, this is not a serious concern since only the linear delay tuning range is important.

Table 1: Impact of Each Control Bit on The DCO Period

Control Bits	Conventional DCO		Proposed DCO	
	Period (ns)	Delta (ps)	Period (ns)	Delta (ps)
100000	1.0138	68.1	1.0250	54.3
010000	1.0819	40.3	1.0793	37.5
001000	1.1222	22.2	1.1168	22.3
000100	1.1444	11.7	1.1391	12.6
000010	1.1561	6	1.1517	6.4
000001	1.1621	5.5	1.1581	6.2
000000	1.1676	-	1.1643	-

In order to compare the power consumption, the last 5 control bits are chosen instead of 6 since the first control bit contributes to non-linear tuning, which is not desirable for the digitally controlled oscillator. Moreover, since the two DCO structure have the same operating ranges, it is more reasonable for us to compare their power consumption. Compared to the conventional DCO, the proposed DCO saves approximately 40% power consumption as shown in Fig. 5. As discussed in Section II, this reduction is due to the comparatively smaller capacitance loading for the Schmitt trigger based inverter than the conventional inverter at the same operating frequency. The proposed DCO is clearly more power efficient than the conventional DCO as shown in Figure 5.

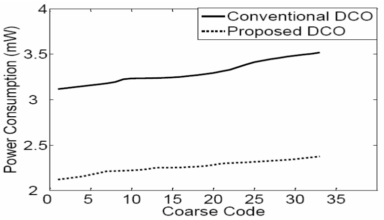


Figure 5. Power consumption of the two DCO structures

IV. IMPROVED STRUCTURE WITH LARGER OPERATING RANGE

The binary controlled DCO structure has a limited linear operating range as discussed above. In this paper, three stage constant delay chains and 4:1 Mux are used to increase the operating range, and the three stage constant delay is tuned by the fixed code such that each stage provides an accurate delay as shown in Fig. 6. The 6th bit is taken off for better linear response and the 1st bit is also taken off for larger coarse resolution. The fine-tuning block has the same structure as the coarse-tuning block except smaller capacitance loading.

IV. SIMULATION RESULTS

The proposed DCO structure with increased operating range is designed and simulated using the 32nm CMOS PTM model. The frequency ranges of the coarse and fine tuning loop are shown in Fig. 7. The curves have a good linearity, which is a key factor of PLL performance.

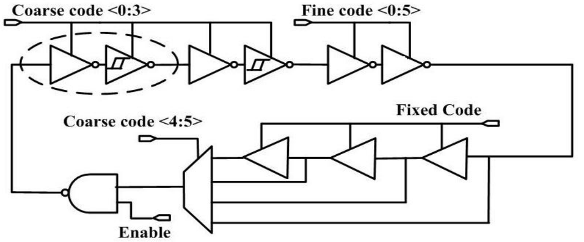
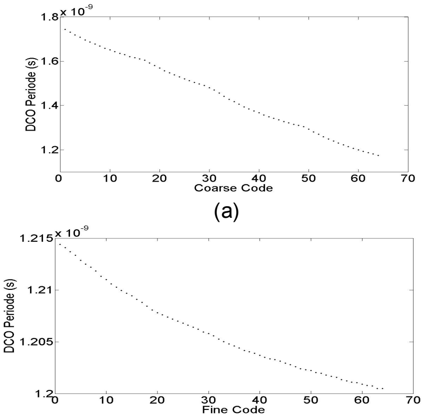


Figure 6. The proposed DCO structure with increased operating range



(a)

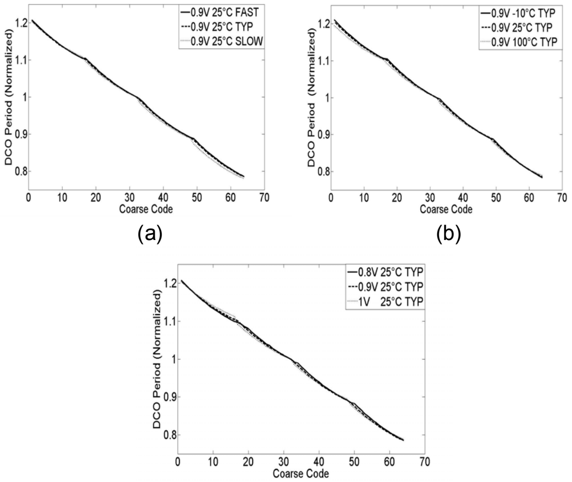
(b)

Figure 7. Operating range of the proposed DCO: (a) Coarse loop (b) Fine loop

Table 2: Characteristics of the DCO Structure

Items	Coarse Delay	Fine Delay
Resolution	6 bit	6 bit
Max. DCO Gain	13ps	0.5ps
Avg. DCO Gain	9ps	0.3ps
Operation Range	570MHz~850MHz	
Power Consumption	2.3mW @ 800MHz	

The operational frequency responses to the process, temperature and voltage variation are shown in Fig. 8. The curves show the normalized data with respect to the center frequency. Fig. 8 shows that the relative delay per code is almost same regardless of the process, temperature and voltage variations, which means this DCO design is very robust to PVT variations.



(a)

(b)

(c)

Figure 8. Delay characteristics of the coarse loop according to Process, Voltage and Temperature variations. (a) Process variation, (b) Temperature Variation, (c) Voltage Variation

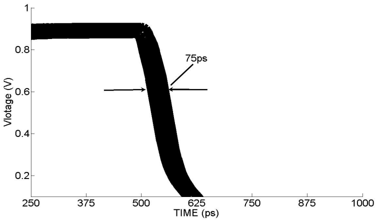


Figure 9. Time-period jitter of the proposed DCO.

The time-period jitter is the time difference between the measured cycle period and the ideal cycle period. The jitter performance of the proposed DCO is simulated by Monte Carlo analysis using a Gaussian distribution function and taking 10% power supply variation into account. The results are shown in Fig. 9 by overlapping every cycle period. A 75ps time-period jitter is measured from the simulation.

IV CONCLUSION

A low power 12-bit digitally controlled CMOS oscillator (DCO) design for low power consumption and low jitter is presented. The presented DCO demonstrates a good robustness to process, voltage, temperature variations, and better linearity comparing to the conventional design. Simulation of the proposed DCO using 32 nm CMOS Predictive Transistor Model achieves a frequency of 570MHz ~ 850MHz and power consumption of 2.3mW at 800MHz and 0.9V power supply. The performance, flexibility, and robustness make the proposed DCO viable for high performance fully digital PLL application.

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