Design and Analysis of a Quad-ferential Ampilifer

Tinna Marie Rookmaaker, Moon Seok Kim and Yong-Bin Kim
Department of Electrical and Computer Engineering
Northeastern University
Boston, MA, U.S.A
Tina.Rookmaaker@analog.com, moor27@coe.neu.edu and ybk@ece.neu.edu

Abstract—**This paper presents a design and analysis of a quad-ferential amplifier. A quad-ferential amplifier consists of four inputs, four outputs, and a V_{OCM} pin which controls the output common-mode voltage. It is similar to the differential amplifier in that it amplifies differences and rejects overall input common-mode. The transfer function shows that quad-ferential amplifier requires symmetry of feedback and gain resistors to approach its ideal behavior. Using a graphical approach the amplifier is compensated to drive a capacitive load of 50pF. The output current drive is designed for minimum load resistance of 150Ω. Statistical models are utilized in performing Monte Carlo simulations to evaluate offset voltage and common-mode rejection. These simulations show mean offset voltage of $265\mu V$ and a common-mode rejection of 126dB.**

I. INTRODUCTION

Traditional three color display devices provide limited brightness dynamic range. As a result of recent developments in display technology, display devices with four primary colors are becoming commercially available. The fourth color, yellow, is changing the signal processing from the traditional 3-channel RGB video to 4-channel RGBY. Design and analysis of the four channels provides an idea regarding the expanded version of the trifferential amplifier.

The trifferential amplifier, designed and patented by Stefano D'Aquino, is the first multi-ferential amplifier. The trifferential amplifier is used in a sub-circuit in a CAT5 (Category 5) video cross-point switch matrix. A cross-point switch matrix is utilized in environments where multiple video inputs are routed to multiple locations. The presence of unwanted common-mode signals in CAT5 video applications corrupts the information. Slight differences in the common-mode DC between the outputs from the cross-point switches can further exacerbate overall image quality due to the brightness variations between outputs.

The common-mode level needs to be controlled for two reasons. First, the overall common-mode must be kept constant to retain the dynamic range of the video signal. Second, the controlled common-mode level maximizes the amount of information that sent over to the CAT5 cable. The most efficient method of controlling the common-mode signal is to remove it from all inputs. Adding clamping circuitry to the inputs can remove the common-mode. The trifferential amplifier mitigates the need for multiple video clamping circuitries. It removes unwanted input common-mode and allows for the common-mode of the cross-point outputs to be controlled.

II. QUAD-FERENTIAL AMPLIFIER OVERVIEW

A. *Definition of a quad-ferential amplifier*

A quad-ferential amplifier is similar in function to the differential amplifier in that it responds to difference signals. The primary function of the quad-ferential amplifier is to remove the overall common-mode and amplify the differences. The quad-ferential amplifier accepts four input voltages and produces four output voltages such that:

- the voltage difference between any pair of output voltages is proportional to the difference between the corresponding pair of input voltages through the same pro-portionality constant. [1] [5]
- the average value of the 4 output voltages is constant and unrelated to the input voltages. [1]

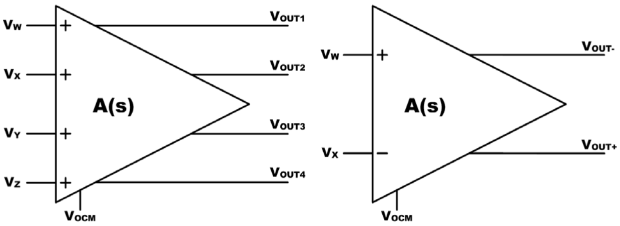


Figure 1. Block diagram of a quad-ferential amplifier.

The symbol of a quad-feretial amplifier is shown in Figure 1. It has 11pins, two supplies, four non-inverting inputs, four outputs, and output common-mode control, V_{ocm}. Similar to the differential amplifier, it is desirable for quad-ferential amplifier to reject input common-mode signals and allow the output common-mode to be controlled by the V_{ocm} pin. The input common-mode voltage is defined as

$$v_{IC} = \frac{v_X+v_Y+v_W+v_Z}{4} \tag{1}$$

The output common-mode voltage is

$$V_{ocm} = v_{OC} = \frac{v_{O1}+v_{O2}+v_{O3}+v_{O4}}{4} \tag{2}$$

Although the quad-ferential amplifier possesses four inputs and outputs, it amplifies six pairs of difference voltages, which is $v_{ID(1,2)}, v_{ID(2,3)}, v_{ID(3,4)}, v_{ID(4,1)}, v_{ID(1,3)}, v_{ID(4,2)}$, to produce the following six unique pairs of difference output voltages; $v_{OD(1,2)}, v_{OD(2,3)}, v_{OD(3,4)}, v_{OD(4,1)}, v_{OD(1,3)}, v_{OD(4,2)}$.

B. Block Diagram

A block diagram for the quad-ferential amplifier is presented in Figure 2.

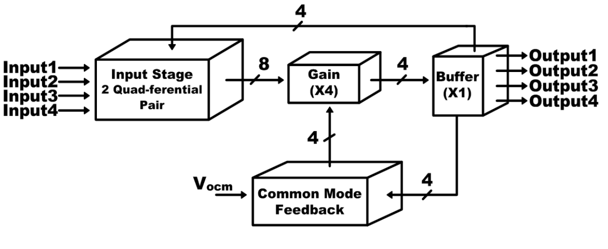


Figure 2. Block diagram of the quad-ferential amplifier.

From an architectural standpoint, the quad-ferential amplifier is an extension of the differential amplifier. Correspondingly, a quad-ferential amplifier processes its signals with three stages and two feedback loops: an input stage, a gain stage, an output stage, a quad-ferential feedback loop to establish negative feedback, and a common-mode loop to control the output common-mode voltage.

C. Transfer function

A typical configuration of the quad-ferential amplifier is two feedback pairs. Each feedback path contains a summing node, a gain resistor, and three feedback resistors. The quad-ferential amplifier establishes negative feedback by taking the average of three outputs and feeding it back to the complementary summing junction. [3]

A symmetry configuration of the quad-ferential amplifier allows for the common-mode term, v_{OC}, to be canceled and the two undesirable outputs with respect to $\frac{v_{OD(1,2)}}{v_{ID(1,2)}}$, $v_{O3}$and v_{O4}, to be canceled. Taking advantage of the symmetry, the non-ideal transfer function can be found by factoring and isolating the input and output signals. After Millman's theorem is applied, the resulting transfer function turns out to be of the canonical form and it is defined as

$$A_{CL(S)} = \frac{A(s)}{1+A\beta} \tag{3}$$

Where, $A(s) = \frac{a(s)}{R_F+3R_G}$, $\beta = \frac{R_G}{R_F}$, $a(s) = \frac{1}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}$

Pole p_1 and p_2 are a dominant pole of output voltages for channel 1. Pole p_2 is uncompensated pole, and pole $p_1$and p_2 are set by the amplifier. The loop gain, T(s), of the quad-ferential amplifier can be expressed as

$$T(s) = A(s)\beta = \frac{R_G}{R_F+3R_G}\frac{1}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \tag{4}$$

The "$3\,R_G$" term inside the loop gain in equation (4) implies there are three outputs being fed back to a summing node. If the open loop gain is sufficiently high, then (3) reduces to $\frac{1}{\beta}$ and the ideal closed loop gain can be simply proportion to R_F over R_G. Due to the inherent architecture of this amplifier, utilizing it in a balanced system is necessary. As a result of the balanced system, the non-ideal and ideal transfer functions remain true for any desire difference voltage.

III. QUAD-FERENTIAL AMPLIFIER DESIGN AND ANALYSIS

A. Quad-ferential pair

A quad-ferential pair amplifies the differences between any two input signals while rejecting common-mode components. A $g_m$cell is shown in Figure 3(a). Configuring all g_m cells such that the input voltage connections do not cross and connecting the resulting output currents accordingly yields a quad-ferential pair as show in Figure 3(b). Since a fundamental trait of a differential pair is its ability to keep the net change in output current zero, a quad-ferential pair thus produces a net Δ (delta) of zero when a difference is applied to the inputs.

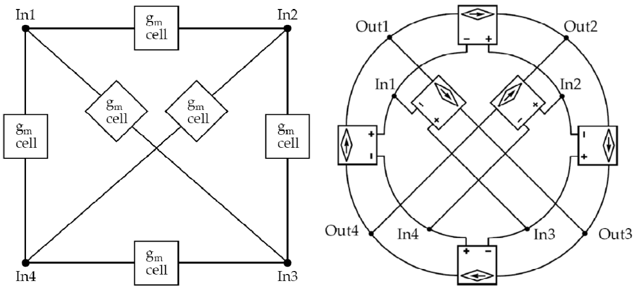


Figure 3. Configuring inputs (a) and a quad-ferential pair (b).

B. Input Stage

A quad-ferential input stage is comprised of two quad-ferential pairs. The positive quad-ferential pair is responsible for positive currents and the negative quad-ferential pair provides the complement to the positive currents. A Large signal and small signal of input stage analysis are presented.

(1) Large Signal Behavior

The output differential voltages of the quad-ferential pair can be expressed as [2]

$$V_{OD1} = \alpha I_{TAIL} R_C\left(\tanh\frac{-V_{ID(1,2)}}{2V_t} + \tanh\frac{V_{ID(4,1)}}{2V_t} + \tanh\frac{-V_{ID(1,3)}}{2V_t}\right) \tag{5}$$

$$V_{OD2} = \alpha I_{TAIL} R_C\left(\tanh\frac{V_{ID(1,2)}}{2V_t} + \tanh\frac{-V_{ID(2,3)}}{2V_t} + \tanh\frac{V_{ID(4,2)}}{2V_t}\right) \tag{6}$$

$$V_{OD3} = \alpha I_{TAIL} R_C\left(\tanh\frac{V_{ID(2,3)}}{2V_t} + \tanh\frac{-V_{ID(3,4)}}{2V_t} + \tanh\frac{V_{ID(1,3)}}{2V_t}\right) \tag{7}$$

$$V_{OD4} = \alpha I_{TAIL} R_C\left(\tanh\frac{V_{ID(3,4)}}{2V_t} + \tanh\frac{-V_{ID(4,1)}}{2V_t} + \tanh\frac{-V_{ID(4,2)}}{2V_t}\right) \tag{8}$$

As (5) through (8) reveal, subtracting two individual voltages of the same channel (i.e. $V_{O1P,D}$ and $V_{O1N,D}$) results in the summation of three tanh functions.

The behavior illustrated in Figure 4 is consistent with the large signal single-ended analysis of the quad-ferential pair responding to a differential input. The peaking in Figure 4 is a result of different rate of changes at the inputs, $(\frac{dV}{dt})$ resulting from two unique differential voltages.

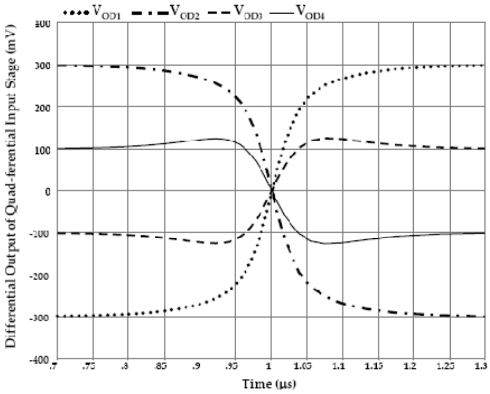


Figure 4. Differential output voltages for a quad-ferential input stage.

(2) Small Signal Behavior

The small signal differential output voltages of the quad-ferential pair can be expressed as

$$v_{od1} = \frac{-g_m R_C}{2} F_{v_{id(1,2)}} + \frac{g_m R_C}{2} F_{v_{id(4,1)}} - \frac{g_m R_C}{2} F_{v_{id(1,3)}} \quad (9)$$

$$v_{od2} = \frac{g_m R_C}{2} F_{v_{id(1,2)}} - \frac{g_m R_C}{2} F_{v_{id(2,3)}} + \frac{g_m R_C}{2} F_{v_{id(4,2)}} \quad (10)$$

$$v_{od3} = \frac{g_m R_C}{2} F_{v_{id(2,3)}} - \frac{g_m R_C}{2} F_{v_{id(3,4)}} + \frac{g_m R_C}{2} F_{v_{id(1,3)}} \quad (11)$$

$$v_{od4} = \frac{g_m R_C}{2} F_{v_{id(3,4)}} - \frac{g_m R_C}{2} F_{v_{id(4,1)}} - \frac{g_m R_C}{2} F_{v_{id(4,2)}} \quad (12)$$

where, $F = \frac{2+\frac{1}{g_m R_{EE}(1+\frac{1}{\beta_0})}}{1+\frac{1}{2 g_m R_{EE}(1+\frac{1}{\beta_0})}}$. As seen in (9) through (12), the common-mode terms are canceled when differential signaling is presented. However, the effect of the impedance from the tail current, R_{EE}, remains as shown in variable F.

C. Gain Stage

Theoretically, the transconductance of the input stage is equal to the second stage, G_{m2} [4]. However, due to base current losses in the second stage, $G_{m2} \neq G_{m1}$. Furthermore, due to the emitter degeneration of Q_{N1}, only 96% of G_{m1} is translated to the high impedance node. From a qualitative perspective, if channel 1 is modulating while channels 2, 3, and 4, are equal and constant, channel 1 will be $9.54dB$ larger in magnitude than the other channels. When the absolute value of $9.54dB$ is normalized to channel 1, 33% difference is realized between channels 1 and channels 2, 3, and 4. Evaluation of channel 1 yields the approximate single-ended gain at the high impedance gain node, $A_{V-SE,CHNL1} \approx 87.4dB$. In addition, the difference between $A_{V-SE,CHNL1}$ and $A_{V-SE,CHNL2}$ is attributed to the transconductance from the input stage. $G_{m1,CHNL1}$ of 11.7mS/mm results in $87.4dB$, and $G_{m1,CHNL2} = 3.8$mS/mm yields $A_{V-SE,CHNL2} \approx 77.5dB$. As expected, simulations of these gains reveal $86.3dB$ and $76.6dB$, and channels 2, 3, and 4 respond identically.

D. Output Stage

The output stage of the quad-ferential amplifier is compromised of four voltage buffers arranged in a parallel configuration. Each buffer is comprised of a diamond voltage buffer. The advantage in using a diamond buffer is that voltage between the input and output are approximately equal. For simplicity, ideal current sources, $I_{BIAS,P}$ and $I_{BIAS,N}$ are used for this analysis. The gain from the input to output is approximately unity. Furthermore, the relationship of the currents between I_{IN} and I_{OUT} are dependent upon the ratio of Q_4 to Q_1 and Q_3 to Q_2 when $I_{BIAS,P} = I_{BIAS,N}$.

To determine the necessary output drive capability, video applications typically require an amplifier be able to drive 150Ω loads. A load impedance of 150Ω results from 75Ω in CAT5 cabling and 75Ω from termination networks. The current driving requirement is $I_{OUT} = \pm 16.6mA$ to drive a load for $\pm 2.5V$ supply. The maximum output current at this output stage is capable of sinking and sourcing the required currents and they are limited by the base current Q_3 and Q_4. The β_P of Q_3 is a limiting factor to determine the DC output current drive. Thus, the requirement of driving $\pm 16.6mA$ in conjunction with $\beta_P \approx 85$ of Q_3 results in minimum $I_{bias} \approx 200\mu A$. With an emitter degenerated, this buffer allows for a signal swing to $\approx 1V$ of the rails with $V_{BE} \approx 0.8V$ and $V_{CESAT} \approx 0.2$. Additionally, the output impedance of output stage, R_O, is determined by the bias level of transistors Q_3 and Q_4 with I_C set to $200\mu A$. $R_O = 86.5\Omega$ satisfies output current drive at ambient when I_C is $200\mu A$.

E. Stability, Compensation, and Feedback

The closed loop transfer function and the loop gain are in equation (3) and (4). Examination of the uncompensated loop gain reveals the cross-over frequency to be 1.5GHz, with p_1 located at 1MHz and p_2 located at 358MHz. The phase margin is -30°, therefore the system is unstable and requires compensation. In practical, the amplifier drives loads up to 50pF. Inclusion of the load capacitance creates an additional pole, p_L. This pole is determined by C_{Load} in conjunction with the output impedance of the amplifier and result in $T(s)$ that has an additional term, $\left(1 - \frac{s}{p_L}\right)^{-1}$.

To compensate the quad-ferential amplifier, a graphical linear approximation is utilized. A dominant pole is introduced such that the loop gain crosses 0dB at the location of p_L resulting in minimum phase margin of 45° for $C_{LOAD} \leq 50$pF . The p_L is 37MHz with 50pF of C_{LOAD} and output impedance 85Ω. In turn, by using the definition of pole, the compensation capacitance turns out to be 7.7pF. Iterating Cc empirically with the simulator yields 45° of phase margin with a Cc= $7pF$. The iterative Cc = $7pF$ is approximately 10% different from the graphical linear approximation technique used. The phase margin of 48° for the common-mode loop is comparable to the differential loop. Thus, the compensation capacitor of Cc = $7pF$ satisfies the stability needs for both differential and common-mode loops.

To achieve negative feedback, the average of three outputs is fed back to the complementary summing node. The quad-ferential amplifier executes the functionality via its input stage in combination with feedback and gain resistors. If the outputs for channels 2, 3, and 4 sums together to form a net "negative Δ" and are fed back to a net "positive Δ" channel 1, a negative feedback for channel 1 is achieved. The

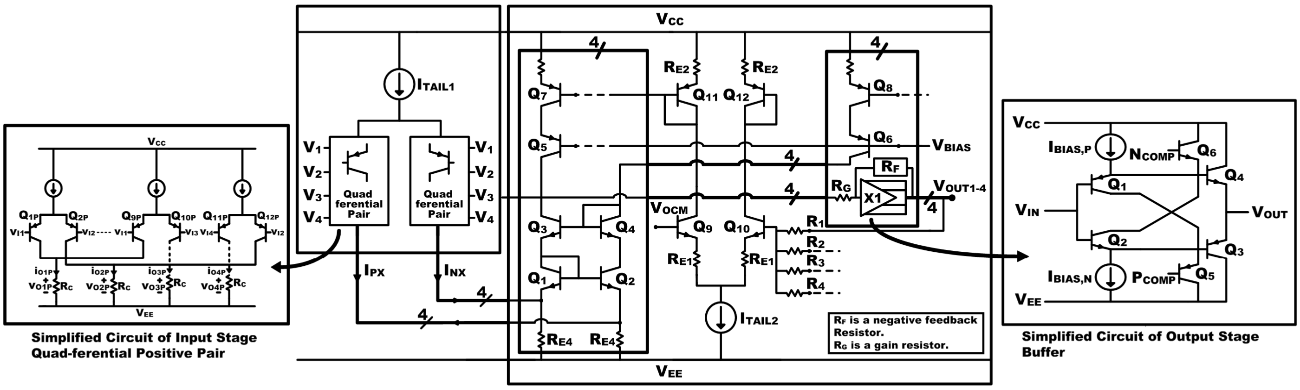
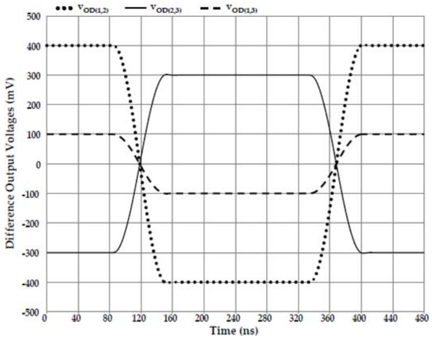


Figure 5. Simplified Circuit of a quad-ferential Amplifier

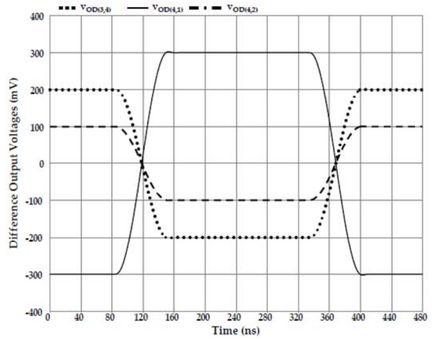
circuit schematic of the quad-ferential amplifier is shown in Figure5.

IV. SIMULATION RESULTS

A monolithic four inputs and outputs quad-ferential amplifier was designed and simulated. The optimum design is obtained with the following values: $V_S^+ = 2.5V, V_S^- = 2.5V, R_F = R_G = 1k\Omega, R_L = 1k\Omega, C_C = 7pF$ and $C_L = 50pF$. Furthermore, the detail of simulation shows that the small signal differential bandwidth is 89MHz. Statistical model is used in performing Monte Carlo simulations to evaluate offset voltage and common-mode rejection in Figure 6 and 7. The offset voltage mean is $265\mu V$ with standard deviation of $430\mu V$, and the common-mode rejection is 126dB**.**

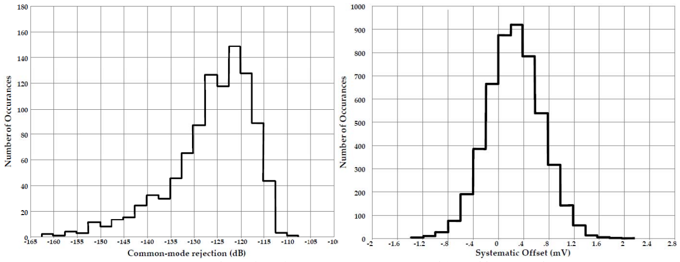


(a) Small signal outputs $V_{OD(1,2)}$, $V_{OD(2,3)}$ and $V_{OD(1,3)}$



(b) Small signal output $V_{OD(3,4)}$, $V_{OD(4,1)}$ and $V_{OD(4,2)}$

Figure 6. Small signal output transient response for G=+1. $R_F = R_G = 1k\Omega$, $R_L = 1k\Omega$, $C_L = 50pF$, $C_C = 7pF$



(a) Common-mode rejection (b) Offset Voltage

Figure 7. (a) Simulation of offset voltage for a quad-amplifier.
(b) Simulation of common-mode rejection for a quad-amplifier.

V. CONCLUSION

The design and analysis of the monolithic four inputs and outputs quad-ferential amplifier is presented. Transient simulations confirmed two fundamental aspects of the quad-ferential amplifier. First, it amplifies the differences. Second, the output common-mode voltage is controlled by V_{OCM}. Magnified small signal transient responses further describe the response of the amplifier. Based on the analysis, the bandwidth for the quad-amplifier is 89MHz. A potential option for increasing the bandwidth is the inclusion of an additional stage. Furthermore, the application within RGBY video chain or its application as two differential attenuators in a signal chain is possibilities.

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