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Journal:	*Transactions on Device and Materials Reliability*
Manuscript ID:	TDMR-2010-10-0124
Suggested Category:	Regular Paper
Date Submitted by the Author:	20-Oct-2010
Complete List of Authors:	Lombardi, Fabrizio; Northeastern University, ECE Kim, Yong-Bin; Northeastern, ECE Cho, Guenho; Northeastern University, ECE
Key Words:	Fault tolerance, Transistors

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Modeling Undeposited CNTs for CNTFET Operation

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Abstract—**The Carbon NanoTube Field Effect Transistor (CNTFET) is a promising device to supersede the MOSFET at the end of the technology roadmap of CMOS. When designing and manufacturing a CNTFET, additional features such as pitch, number and position of the CNTs must be considered to assess its performance. One of the defect types that can occur when fabricating a CNTFET, is the absence of some CNTs following the deposition/growth step. As result of this type of defect, a CNTFET will show a change in operational characteristics because drain current, gate capacitance, and delay will be affected due to the lower number of CNTs (and the uneven spacing between them) present in the channel of the transistor. This paper presents a new model by which the drain current, the gate capacitance and the delay can be found when not all CNTs are deposited on the substrate. This results in an uneven CNT spacing in the channel; new equations are derived and shown to be applicable to both defective and defect-free CNTFETs. The proposed model has been implemented in MATLAB and has been extensively simulated to show that defects due to undeposited CNTs have a significant impact on the operation of a CNTFET. Delay as degradation in performance is shown to be related to both the number and position of the defects; an extensive delay analysis on both deterministic and probabilistic basis is presented.**

Index Terms—**Defect model, CNT, CNTFET, manufacturing, emerging technologies**

I. Introduction

THE Carbon NanoTube Field Effect Transistor (CNTFET) has been advocated as one of the possible alternatives to replace the conventional MOSFET due to its excellent performance characteristics (13 times CV/I improvement over a bulk n-type MOSFET at a 32 nm feature size). Moreover, its operational principles and device structure are similar to those of a MOSFET device, thus showing excellent compatibility with CMOS manufacturing processes. In CNTFETs, ballistic or near-ballistic transport phenomena have been observed under low voltage, and the existing design infrastructure and fabrication process of CMOS-based MOSFETs can be also used for CNTFETs [1][2][3][4]. The I-V characteristics and gate capacitance of a CNTFET are different from those of the MOSFET because in addition to the dependency on well known parameters (node voltages, threshold voltage, gate width/length) for a MOSFET, the three device characteristics (pitch, number, and position of CNTs) must also be established. Due to the so-called screening effect [1][2], the current of a CNTFET changes depending on the spacing (pitch) and the position of the CNTs; so, the current of a CNTFET cannot be increased linearly by just increasing the number of CNTs. When considering the capacitance, the potential profile in the gate region is affected by a screening/imaging effect from the parallel conducting channels (i.e. the CNTs) [5].

For CNTFET manufacturing, CNTs are usually grown or deposited on a substrate at a fixed pitch prior to defining the CNTFET and the contacts. If the pitch is decreased, the processes for correctly aligning and positioning CNTs at the desired locations become difficult [6][7]. Moreover, following manufacturing, 10% to 70% of the CNTs are usually metallic and have to be discarded; only semiconducting CNTs must be utilized for a CNTFET [7]. For current technology, corrective processes can be employed when manufacturing CNTFETs; for example by using electrical burning and selective etching, defective CNTs (such as misaligned CNTs) can be removed [8][9]. Techniques for detection and correction have been proposed [7]. One of the likely defects occurs during the deposition of the CNTs, i.e. only some of the required CNTs are deposited. These defects change radically the performance of the fabricated CNTFET because for example, the delay can vary significantly due to the smaller number of CNTs present in the channel and the uneven spacing between them. Statistical approaches have been reported in the technical literature [10][11] using the HSPICE model of [1][2][12] to identify the impact of defects. However in [1][2], the spacing between CNTs of a CNTFET is constant and therefore, it cannot take into consideration the impact of undeposited CNTs. Furthermore, in [1] the screening effect is assumed to be symmetric, i.e. it is assumed that the distances at both sides of a deposited CNT with respect to adjacent CNTs are always the same; hence, a new analytical framework is required for modeling a CNTFET following the deposition of not all CNTs on the substrate.

In this paper, a MATLAB-based model for a CNTFET with undeposited CNTs as defects is proposed. Initially, a comprehensive characterization is pursued and new equations are found for the capacitance and drain current when

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undeposited CNTs are encountered following CNTFET fabrication. It is shown that CNTFET performance (and in particular the delay) depends on the number of defects as well as their position in the CNTFET, i.e. the so-called configuration of the defective CNTFET. An extensive analysis and simulation-based evaluation of the CNTFET configurations that yield the least and largest delays are pursued on deterministic and probabilistic basis.

II. CNTFET Structure and Model

CNTs are sheets of graphene rolled into tubes. The single-walled CNT can be either metallic or semiconducting depending on the chirality (i.e., the direction in which the graphene sheet is rolled). The diameter of CNT is also determined by the chirality [1]. Semiconducting nanotubes have attracted the widespread attention of device/circuit designers as an alternative channel implementation for high-performance transistors. In this paper, we focus on only single-walled semiconducting CNTs. A typical structure of a MOSFET-like CNTFET device is illustrated in Figure 1. For its fabrication, CNTs are grown or transferred (deposited) to a substrate using a fixed spacing (pitch) prior to defining CNTFET-based gates and contacts.

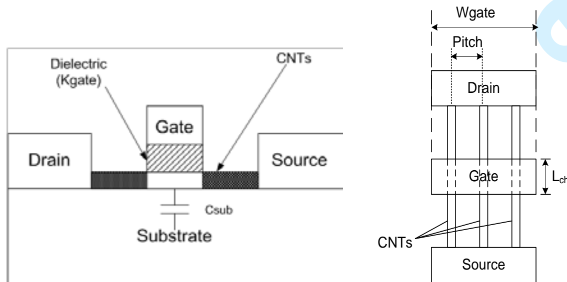

Fig. 1. CNTFET Structure

To evaluate the performance of a CNTFET, various simulation models have been proposed [12][13][14]. The CNFET HSPICE model of [12] is widely used in circuit design. For a CNTFET in addition to the dependency on node voltages (VGS and VDS), threshold voltage (Vth), and gate width/length such as in a MOSFET, the three features of pitch, number, and position of CNTs determine the gate capacitance and current, as presented in more detail next .

A. Gate Capacitance Model

The equation for the gate capacitance of a CNTFET ($C_{gg,CNTFET}$) is given in (1); the gate outer fringe capacitance to the doped source/drain regions is ignored because the gate outer fringe capacitance is significantly smaller than the other components when the gate height is 64nm and the source/drain length is 32nm (as used in this paper and the technical literature [1][2][5][15]). Moreover, the values are not changed depending on the position and the number of CNTs. The gate capacitance is function of the gate to channel capacitance (C_{gc}), the gate length (L_g), the gate to gate capacitance (C_{gtg}), and the gate width (W_g). C_{gc} is given in (2) and consists of three terms, as related to the unit capacitances of the gate to the cylinders (CNTs) at the two ends (C_{gc_e}), in the middle (C_{gc_m}), and the number of CNTs (N). As given in (2), this model is based on placing first the CNTs at the edges and then the remaining N-2 CNTs from the middle across the gate of a CNTFET.

$$C_{gg,CNTFET} \approx C_{gc} \times L_g + f_{miller} \times C_{gtg} \times W_g \tag{1}$$

$$C_{gc} = \min(N,2) \times C_{gc_e} + \max(N-2,0) \times C_{gc_m} \tag{2}$$

When considering C_{gc} (Figure 2 (a)), in the channel conduction is accomplished by identical objects (i.e. the CNTs) in parallel (in this case, 7 objects with the same pitch), and the gate electrode (the planar object #0); note also that the possible number of CNTs in a CNTFET is a function of the gate width, the diameter of CNTs, and the placement accuracy/resolution of the employed fabrication technology. To calculate the coupling capacitance (C_{01}) between object #0 and the object #1, the total effect of the other 6 objects around object #1 can be lumped and approximated by considering only the two nearest objects, i.e. objects #2 and #3 in Figure 2 (b). This assumption is valid, because objects located at a far distance from object #1 have a rather weak influence on the electric field distribution between electrode #0 and object #1. This is a commonly found assumption in the technical literature [5], thus effectively making the gate to channel capacitance independent of the number of cylinders in the model. Therefore, when calculating the screening/imaging effect of a CNT (Figure 2 (a)), only the two neighboring CNTs are considered for an internal (non boundary) CNT (Figure 2 (b)). For a boundary CNT (i.e. located at the edge), only one neighbor must be considered (Figure 2 (c)).

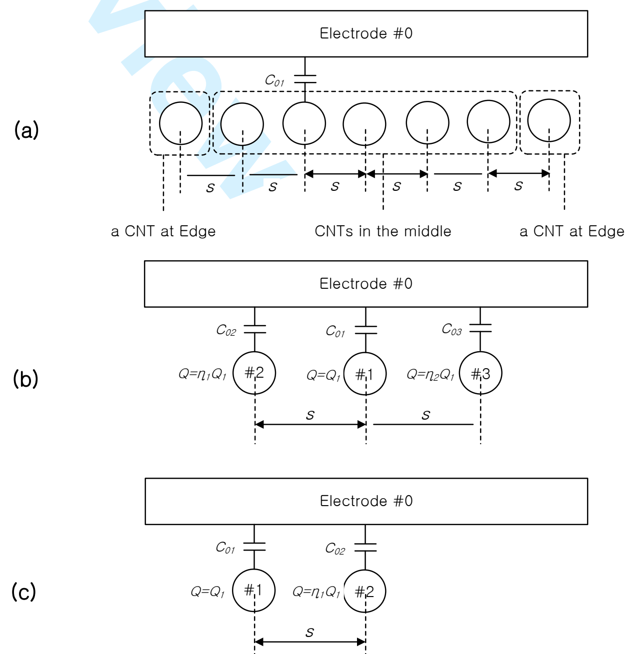

Fig. 2. Gate to Channel Capacitance Model

When a voltage V_1 is applied between objects #1, #2, #3, and the electrode #0, the charges Q_1, $\eta_1 Q_1$, and $\eta_2 Q_1$ are found on these three objects due to the different coupling capacitance C_{01}, C_{02}, and C_{03}. η_1 and η_2 are defined as the ratios of C_{02} to C_{01} and C_{03} to C_{01}, respectively, i.e.

$$\eta_1 = \frac{C_{02}}{C_{01}} \quad \eta_2 = \frac{C_{03}}{C_{01}} \tag{3}$$

From [5], C01 is given by

$$C_{01} = \frac{1}{\frac{1}{C_{\inf}} + \eta_1 \cdot \frac{1}{C_{sr_1}} + \eta_2 \cdot \frac{1}{C_{sr_2}}} \tag{4}$$

C_{sr_1} and C_{sr_2} are the equivalent capacitances due to the screening effects of objects #2 and #3, respectively; C_{inf} is the capacitance between electrode #0 and object #1 with no screening from all other objects. When C_{inf} and C_{sr} are replaced by C_{inf} and C_{sr} for calculating the gate to channel capacitance (C_{gc_sr} and C_{gc_inf}) of [5], C_{01} in (4) becomes the gate to channel capacitance (C_{gc}) of each CNT in a CNTFET. η_1 and η_2 are function of the geometry and the number/position of the objects in the model. Using [5], the following cases can be distinguished using (4): (A) when C_{gc_e} is found, η_1=1 and η_2=0 because the screening objects are located only on one side (Figure 2 (c)); (B) when C_{gc_m} is found, $\eta_1 = \eta_2 = C_{gc_e}/C_{gc_m}$ and $C_{gc_sr_1} = C_{gc_sr_2}$ because objects #2 and #3 are positioned at a same pitch on both sides of object #1 (Figure 2 (b)). Therefore, C_{gc_e} and C_{gc_m} can be written as (5) and (6) respectively (where $C_{gc_m_symmetric}$ is the capacitance for the case in which the pitch between the CNTs is constant; this feature will be discussed in more detail in a later section).

$$C_{gc_e} = \frac{C_{gc_\inf} \times C_{gc_sr}}{C_{gc_\inf} + C_{gc_sr}} \tag{5}$$

$$C_{gc_m} = 2C_{gc_e} - C_{gc_\inf} = C_{gc_m_symmetric} \tag{6}$$

B. Current Model

In [1][2], the current equations for a semiconducting CNT are given by (7) and (8) (the fitting parameters for the sub-threshold slope and the measured short channel effects are not relevant in this analysis and are ignored). $\Delta\Phi_B$ is the channel surface potential that can be achieved by solving (8). T_{LR} and T_{RL} are the transmission probabilities of the carriers flowing from the drain to the source (+k branch) and from the source to the drain (-k branch) respectively. $J_{m,l}$ is the current of the sub-state (m,l). $E_{m,l}$ is the carrier energy at the (m,l) sub-state. M and L are the number of sub-bands and the number of sub-states, respectively. In this paper, it is assumed that M=2 and L=9 because only the first 2 or 3 sub-bands and the first 10-15 sub-states have a significant impact on the current [1][2]. C_{gc_p} is found based on the position of the CNTs and is given by (9).

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = 2\sum_{m=1}^{2}\sum_{l=0}^{9}[T_{LR} J_{m,l}(0, \Delta\Phi_B)|_{+k} - T_{RL} J_{m,l}(V_{ch,DS}, \Delta\Phi_B)|_{-k}] \tag{7}$$

$$\Delta\Phi_B = \frac{e}{((C_{gc_p} \cdot + C_{sub})} \times \left[C_{gc_p} \cdot V_{ch,GS} - \frac{4e}{L_g} \sum_{m=1}^{2}\sum_{l=0}^{9} \left[\frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B)/kT}} + \frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B+eV_{ch,DS})/kT}} \right] \right] \tag{8}$$

$$C_{gc_p} = \begin{cases} C_{gc_m} & when \quad CNT \quad is \quad positioned \quad in \quad the \quad middle \\ C_{gc_e} & when \quad CNT \quad is \quad positioned \quad at \quad the \quad edge \end{cases} \tag{9}$$

III. Proposed Model

During fabrication, CNTs are usually grown or transferred (deposited) to a substrate at a fixed pitch prior to defining the CNTFET gates and the contacts (Figure 1) [6][7]. Among the grown (deposited) CNTs, only semiconducting CNTs are considered; metallic CNTs increase leakage and reduce the noise margin [11]. Other types of defect are mispositioned and misaligned CNTs and cause shorts and incorrect logic functionality [7]. Corrective and design techniques to remove CNT defects have been proposed [7][8][9]. It is likely that some CNTs will not be grown on the substrate, hence this type of defects (referred to as *undeposited CNT*) will result in a CNTFET in which the distance between deposited CNTs is not constant (Figure 3). In these cases, the model of [1][2] cannot be used due to the assumed even spacing between CNTs. Figure 3 shows that when three CNTs are undeposited, three different intervals (int_a, int_b, and int_c) exist, i.e. uneven spacing. Hereafter, the correct spacing between CNTs is defined by the pitch (s); in the presence of undeposited CNTs (as defects), the spacing between each pair of deposited CNTs is referred to as an interval (int) (Figure 3). Each int in a CNTFET is a multiple of the pitch (i.e. s); for example, in Figure 3, int_a=2s, int_b=3s, and int_c=1s. Next, new models for the gate capacitance and drain current are proposed under the CNTFET scenario of undeposited CNTs.

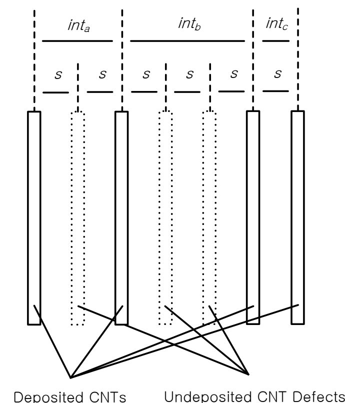

Fig. 3. CNTFET with Undeposited CNTs and Intervals

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A. Proposed Gate Capacitance Model

Let N_{CD} denote number of CNT defects (i.e. undeposited CNTs); hence, the number of deposited CNTs is given by $N\text{-}N_{CD}$ and intervals are present between some pairs of tubes. Initially, (2) is changed to (10) by taking into account the reduced number of deposited CNTs for calculating C_{gc}.

$$C_{gc} = \min(N - N_{CD}, 2) \times C_{gc_e} + \max(N - N_{CD} - 2, 0) \times C_{gc_m} \quad (10)$$

When C_{gc_m} is calculated from (4), in the defect free scenario (6) is obtained as CNTs are separated by the same spacing (i.e. even or constant pitch), as shown in Figure 2. However, when defects due to undeposited CNTs occur (Figure 3), the intervals between CNTs are uneven as dependent on the number and position of the defects. Therefore, (6) cannot be used and a new equation for C_{gc_m} must be found from (4). Prior to finding the new equation for C_{gc_m}, let the C_{gc_m} for two intervals of equal values be denoted as $C_{gc_m_symmetric}$ and the C_{gc_m} for two different intervals be denoted as $C_{gc_m_asymmetric}$. So, C_{gc_m} is function of the intervals (as in (11)) and $C_{gc_m_symmetric}$ is added to (6).

$$C_{gc_m} = \begin{Bmatrix} C_{gc_m_symmetric} & int_1 = int_2 \\ C_{gc_m_asymmetric} & int_1 \neq int_2 \end{Bmatrix} \quad (11)$$

Two cases can be distinguished: (A) If $C_{gc_m_asymmetric}$ is found from (4), then new values for η_1 and η_2 in (3) should be found. (B) If $C_{gc_m_symmetric}$ is found from (4), then $\eta_1 = \eta_2 = C_{gc_e} / C_{gc_m}$ and $C_{gc_sr_1} = C_{gc_sr_2}$ because $int_1 = int_2$ [5]. For $C_{gc_m_asymmetric}$, $int_1 \neq int_2$ (Figure 4), two values for C_{gc_e} (denoted by $C_{gc_e_int1}$ and $C_{gc_e_int2}$), two values of $C_{gc_m_symmetric}$ (denoted by $C_{gc_m_symmetric_int1}$ and $C_{gc_m_symmetric_int2}$), and two values of C_{gc_sr} (denoted by $C_{gc_sr_int1}$ and $C_{gc_sr_int2}$) must be found as related to the two intervals (int_1 and int_2). In this model (as consistent with the existing technical literature), it is assumed that CNTs that are spaced further apart from the two intervals considered, have a negligible effect, i.e. when calculating C_{gc_m} of CNT #1, only the two intervals (int_1 and int_2) to two adjacent deposited CNTs (#2 and #3) are considered. This is also assumed in the defect-free case when C_{gc_e} and $C_{gc_m_symmetric}$ are found from (4) as function of the pitch in a previous section [5]. As int is a multiple of the pitch (s), then this model is consistent and correct. By considering all components of C_{gc}, (3) and (4) can be modified as (12) and (13) (C_{inf} is not changed because it is independent of the pitch or the interval).

$$\eta_1 = \frac{C_{gc_e}}{C_{gc_m_symmetric}} \Rightarrow \frac{C_{gc_e_\text{int}1}}{C_{gc_m_symmetric_\text{int}1}} \quad (12)$$
$$\eta_2 = \frac{C_{gc_e}}{C_{gc_m_symmetric}} \Rightarrow \frac{C_{gc_e_\text{int}2}}{C_{gc_m_symmetric_\text{int}2}}$$

$$C_{gc_m_asymmetric} = \frac{1}{\frac{1}{C_{\text{inf}}} + \eta_1 \cdot \frac{1}{C_{sr_1}} + \eta_2 \cdot \frac{1}{C_{sr_2}}} = \frac{1}{\frac{1}{C_{\text{inf}}} + A + B} \quad (13)$$
$$A = \frac{C_{gc_e_\text{int}1}}{C_{gc_m_symmetric_\text{int}1}} \cdot \frac{1}{C_{gc_sr_\text{int}1}}$$
$$B = \frac{C_{gc_e_\text{int}2}}{C_{gc_m_symmetric_\text{int}2}} \cdot \frac{1}{C_{gc_sr_\text{int}2}}$$

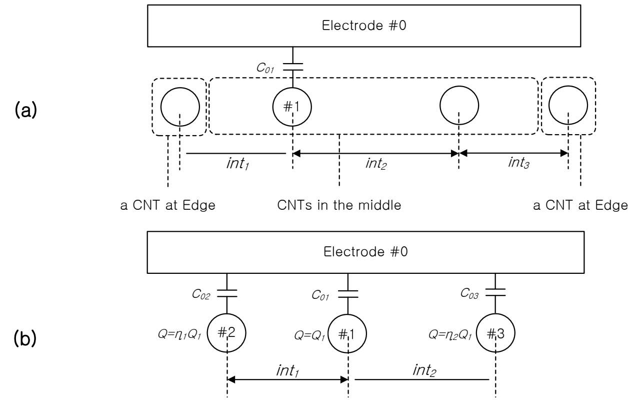

Fig. 4. Gate to Channel Capacitance Model for CNTFET with Defects

For comparing $C_{gc_m_asymmetric}$ with C_{gc_e} and $C_{gc_m_symmetric}$, its value is plotted versus a single interval (int_1) in Figure 5 (the second interval int_2 for $C_{gc_m_asymmetric}$ is denoted by $C_{gc_m_asymmetric_int2}$). For example, in Figure 5, $C_{gc_m_asymmetric_2s}$ denotes $C_{gc_m_asymmetric}$ when int_1 is changed from 1s to 7s and int_2 is 2s. As mentioned previously, intervals are multiples of s (and in this paper, the pitch is s=3.812 nm). The values of C_{gc_e} and $C_{gc_m_symmetric}$ as function of the interval (i.e. (5) and (6)) [1][2] are also plotted in Figure 5. As shown in Figure 5, when the two intervals are the same, $C_{gc_m_asymmetric}$ is the same as $C_{gc_m_symmetric}$,; however, when only one interval is changed for $C_{gc_m_asymmetric}$, the trend of $C_{gc_m_asymmetric}$ is similar to C_{gc_e}. Therefore, Figure 5 shows that the value of $C_{gc_m_asymmetric}$ found by the proposed model in the absence of defects (undeposited CNTs) is the same as the values of C_{gc_e} and $C_{gc_m_symmetric}$ in the original model of [1]. However, the proposed model can also capture the impact of defects on the gate capacitance if not all CNTs are deposited/grown as considered in this paper.

B. Proposed Drain Current Model

(7) and (8) require many parameters; however, C_{gc_p} mostly changes as function of the pitch (intervals). From (9) and (11), C_{gc_p} can be defined depending on the intervals (as given below in (14)). Once C_{gc_p} is found and the gate voltage (V_{GS}) is specified, then $\Delta\Phi_B$ can be calculated from (8); using $\Delta\Phi_B$ and the drain voltage (V_{DS}), the drain current of the CNTFET can be calculated from (7).

$$C_{gc_p} = \begin{cases} C_{gc_e} & int_1 = 0 \quad or \quad int_2 = 0 \\ C_{gc_m_symmetric} & int_1 = int_2 \\ C_{gc_m_asymmetric} & int_1 \neq int_2 \end{cases} \quad (14)$$

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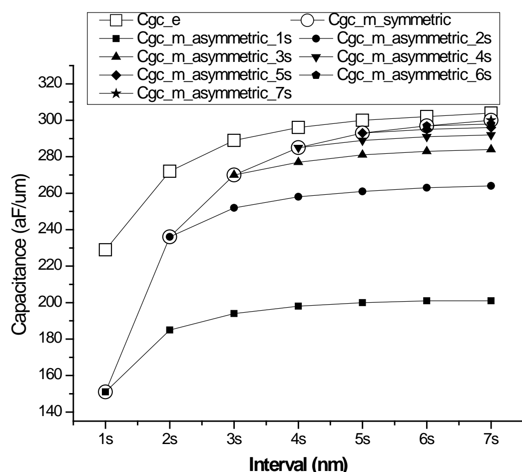

Fig. 5. C_{gc_e} ,$C_{gc_m_symmetric}$, and $C_{gc_m_asymmetry}$ vs. Interval

C. Simulation Results

In this section, the drain current, capacitance, and delay in a CNTFET are calculated by using MATLAB as function of N_{CD} for V_{GS}=0.9v, (19,0) as chirality vector, N=9, and W_g=32nm. The drain current is found over the range of V_{DS} (from 0v to 0.9v). (19,0) and N=9 are selected for consistency with the technical literature [1][2]; moreover under these parameter values, the CNTFET has better performance (delay and energy) than silicon CMOS when the pitch is 4nm [15]. The chirality vector of (19,0) corresponds to a CNT diameter (d) of 1.507 nm [1]. The pitch of a CNTFET is calculated in (15) using W_g, d, and N with the largest possible pitch, i.e. the pitch is given by 3.812 nm when W_g =32nm and N=9 or in general,

$$s = (W_g - d)/(N - 1) \qquad (15)$$

Figure 6 shows the plot of the drain current versus N_{CD}; the drain current is reduced almost linearly when N_{CD} increases because the CNTs are used in the conducting channel between source and drain of a CNTFET. However, at a fixed value of N_{CD}, the drain current of a CNTFET changes as function of the position of the undeposited CNTs (due to the new values of the intervals as spacing between CNTs). Figure 6 shows also the largest and least drain currents at a fixed value of N_{CD}; under these conditions, the gate capacitance and the delay are also calculated and plotted in Figure 7 and Figure 8 respectively. Figure 7 shows that the total gate capacitance decreases almost linearly by increasing N_{CD} because by (1), the gate capacitance consists of the sum of the capacitances of all deposited CNTs. The deviation in value depends on the position of the undeposited CNTs at a fixed N_{CD}. Having found the drain current and gate capacitance, the delay is calculated by using the CV/I equation [15] (Figure 8); this shows that the delay increases exponentially with N_{CD} and its value is also dependent on the position of the undeposited CNTs.

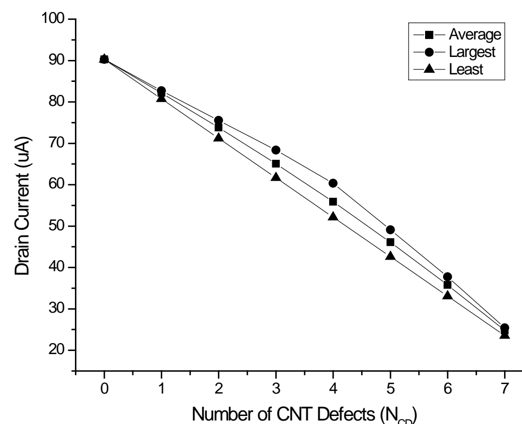

Fig. 6. Drain Current vs. Number of Defects (N_{CD}) (V_{GS}=0.9V, (19,0), N=9, W_g=32nm)

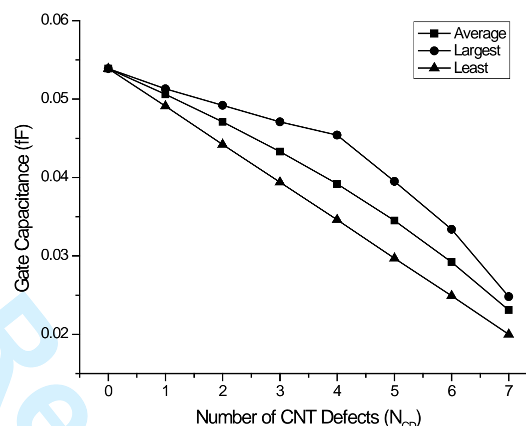

Fig. 7. Gate Capacitance vs. Number of Defects (N_{CD}) (V_{GS}=0.9V, (19,0), N=9, W_g=32nm)

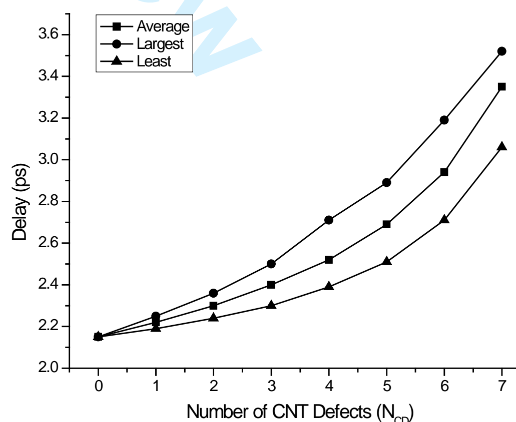

Fig. 8. Delay vs. Number of Defects (N_{CD}) (V_{GS}=0.9V, (19,0), N=9, W_g=32nm)

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IV. Delay Analysis

In this paper, the CNTFET is modeled following CNT deposition in the fabrication process; Figure 9 shows a CNTFET in which only 4 of the required 7 CNTs have been deposited. Its performance depends on the number of undeposited CNTs as defects (given by N_{CD}=3 in Figure 9) as well as their position. A CNTFET with N CNTs is represented by a N binary string in which the ith bit of the binary string is 0 (1) if the ith CNT is undeposited (deposited). This string (also referred to as *configuration*) denotes the state of the CNTFET with respect to the defects and is denoted by P_{CD}. The substrings of 0's are also referred to as *intervals*. Figure 9 shows also the corresponding P_{CD}, i.e. P_{CD} is given by{1 0 1 0 0 1} when N=7, N_{CD} =3 and two intervals exist. Let the number of combinations of N_{CD} defects be denoted by N_{CCD} and

$$N_{CCD} = \binom{N}{N_{CD}} = \frac{N!}{N_{CD}! \times (N - N_{CD})!} \qquad (16)$$

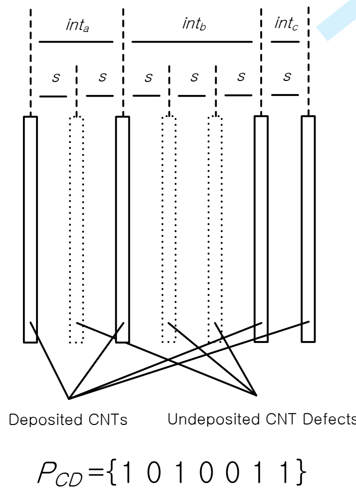

Fig. 9. Configuration of a CNTFET with Undeposited CNTs and Intervals

An algorithm for deterministically calculating the delay of a CNTFET with undeposited CNTs is proposed in this section using the previous presented model for the capacitance and current. This algorithm (referred to as Algorithm 1) utilizes a combinatorial routine (i.e. nchoosek in MATLAB) for finding all possible P_{CD}'s combination (N_{CCD}); every ith combination in the CNTFETs is considered. Then, in each P_{CD}, both intervals of deposited CNTs (N-N_{CD}) are established; for every jth CNT, both of its intervals are denoted as $int_1(j)$ and $int_2(j)$. Based on the values of the intervals, C_{gc_p} is determined using (5),(6),(13), and (14). Having found C_{gc_p}, the gate capacitance of the CNTFET is calculated by (1) (the current of each individual CNT can be calculated using C_{gc_p} by (7) and (8)). By adding the currents of all CNTs, the current of the CNTFET is found. Finally, the delay is calculated using the well known CV/I equation.

Algorithm *Delay*
begin
  do algorithm for choosing N_{CD} from N
  for i to N_{CCD}
    for j to N-N_{CD}
      if $int_1(j)$=0 or $int_2(j)$=0
        $C_{gc_p}(j)=C_{gc_e}(int_1(j), int_2(j))$
      else if $int_1(j)$==$int_2(j)$
        $C_{gc_p}(j)=C_{gc_m_symmetric}(int_1(j))$
      else
        $C_{gc_p}(j)=C_{gc_m_assymetric}(int_1(j), int_2(j))$
      end
      $C_{gc}(i) \bigcup \{C_{gc_p}(j)\}$
      Total_$I(i) \bigcup I_{semi}(V_{GS}, V_{DS}, C_{gc_p}(j))$
    end
    $C_{gg,CNTFET}(i)(W_g, L_g, C_{gc}(i))$
    $Delay_{gg,CNTFET}(i)=(4 \cdot C_{gg,CNTFET}(i) \cdot V)/$ Total_$I(i)$
  end
end

Algorithm 1. Delay Calculation for a CNTFET with Undeposited CNTs

To assess the deviation of the largest and least values with the average value in drain current, gate capacitance, and delay, the Relative Standard Deviation (RSD) is calculated; the results are plotted in Figure 10. Figure 10 shows that the RSDs for the rate of change in drain current and capacitance have different values. As both drain current and gate capacitance vary as function of C_{gc} (as related to the intervals int_1 and int_2 of each CNT), the rate of change for the gate capacitance is larger than for the drain current. Moreover, the maximum deviation point for the gate capacitance is different from the current, because the gate capacitance is affected not only by C_{gc}, but also by C_{gtg} and W_g (as in (1)). Therefore, the RSD for the delay is affected mostly by the gate capacitance. (16) is also plotted in Figure 11; N_{CCD} has maximum value when N_{CD} is 4 and 5, however the maximum deviation point for the delay does not occur at maximum N_{CCD}, therefore the deviation in delay cannot be simply expected from the number of combinations.

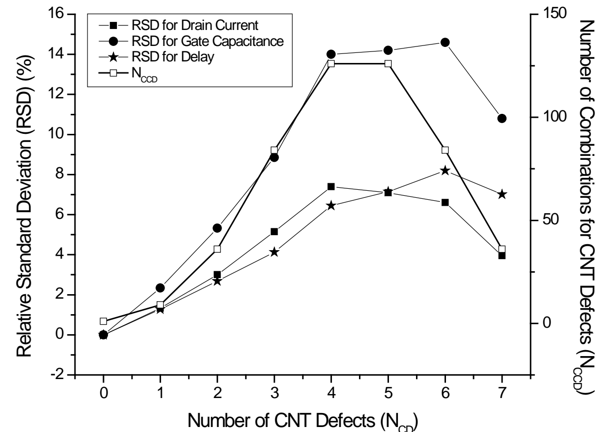

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Fig. 10. Relative Standard Deviation (RSD) and Number of Combinations for CNT Defects (N_{CCD}) vs. Number of CNT defects (N_{CD}) (V_{GS}=0.9V, (19,0), N=9, W_g=32nm)

A. *Largest and Least Delays*

In this section, the configurations (i.e. the P_{CD}) that result in the largest and least delays are established. Let the P_{CD} for the largest delay and the P_{CD} for the least delay be denoted as $P_{CD_Largest}$ and P_{CD_Least} respectively. Depending on P_{CD}, when the two intervals (int_1 and int_2) of each deposited CNT change due to defects, variations in current, capacitance, and delay (at a fixed N_{CD}) occur in the operation of the CNTFET. Tables 1 and 2 show the two intervals of CNTs for largest and least delays respectively. For example, when N_{CD}=6 in Tables 1 and 2 (this value is chosen because the RSD for the delay is maximum when N_{CD}=6 as reported previously in Figure 10), there are 3 deposited CNTs in a CNTFET and two different combinations of intervals. In Table 1, the two CNT intervals are ∞s and 4s nm, and all single CNT intervals are 4 nm. '∞' means that the CNT has only one adjacent CNT on one side (i.e. the CNT is positioned at the edge of the CNTFET). As mentioned previously, s denotes the pitch (in this case 3.812 nm). These CNT configurations are shown in Figure 11 (a). In Table 2, the two CNT intervals are ∞s nm and 1s nm, and all single CNT intervals are 1 nm. These CNTs are also shown in Figures 11 (b), (c), and (d) depending on P_{CD}. As shown in Tables 1 and 2 as well as Figure 11, when CNTs are not positioned between correctly deposited CNTs, all intervals between CNTs have the smallest values, thus the delay has the least value. When non-defective CNTs have the largest intervals, the delay becomes the largest. In general, when the intervals decrease, the drain current decreases due to the screening effect [1][2] and the gate capacitance also decreases due to the decrease of C_{gc} (Figure 7 and (1)). However, Tables 1 and 2 show that the delay decreases (as the delay is mostly affected by the gate capacitance in the CV/I equation). These results are consistent with the results of the RSDs of Figure 10.

TABLE I
TWO INTERVALS OF CNTS FOR LARGEST DELAY
(V_{GS}=0.9V, (19,0), N=9)

N_{CD}	int$_1$ (nm)	int$_2$ (nm)	Number of CNT
1	∞s	1s	1
	∞s	2s	1
	1s	1s	5
	1s	2s	1
2	∞s	2s	2
	1s	2s	2
	1s	1s	3
3	∞s	2s	2
	1s	1s	1
	1s	2s	2
	2s	2s	1
4	∞s	2s	2
	2s	2s	3
5	∞s	2s	1
	∞s	3s	1
	2s	3s	1
	3s	3s	1
6	∞s	4s	2
	4s	4s	1
7	∞s	8s	2

TABLE II
TWO INTERVALS OF CNTS FOR LEAST DELAY
(V_{GS}=0.9V, (19,0), N=9)

N_{CD}	int$_1$ (nm)	int$_2$ (nm)	Number of CNT
1	∞s	1s	2
	1s	1s	6
2	∞s	1s	2
	1s	1s	5
3	∞s	1s	2
	1s	1s	4
4	∞s	1s	2
	1s	1s	3
5	∞s	1s	2
	1s	1s	2
6	∞s	1s	2
	1s	1s	1
7	∞s	1s	2

V. PROBABILISTIC ANALYSIS

In practice, P_{CD} and N_{CD} are affected by manufacturing; so, a probabilistic process is also proposed to calculate the probability of a given P_{CD} to occur (this is denoted as $PROB_{PCD}$). Let the *random variable* for the number of CNT defects be denoted as X_{CD} with range $S=\{0,1,\ldots,N\}$; X_{CD} is assumed to be *independently distributed* and the probability of CNT defects is denoted by p_{CD} ($0\leq p_{CD}\leq 1$). Then, $PROB_{PCD}$ is given by

$$PROB_{PCD}[X_{CD}=N_{CD}]=\binom{N}{N_{CD}}\times p_{CD}{}^{N_{CD}}\times(1-p_{CD})^{(N-N_{CD})}\times 100 \quad (17)$$

Using (16) for N_{CCD}, (17) can be written as

$$PROB_{PCD}[X_{CD}=N_{CD}]=N_{CCD}\times p_{CD}{}^{N_{CD}}\times(1-p_{CD})^{(N-N_{CD})}\times 100 \quad (18)$$

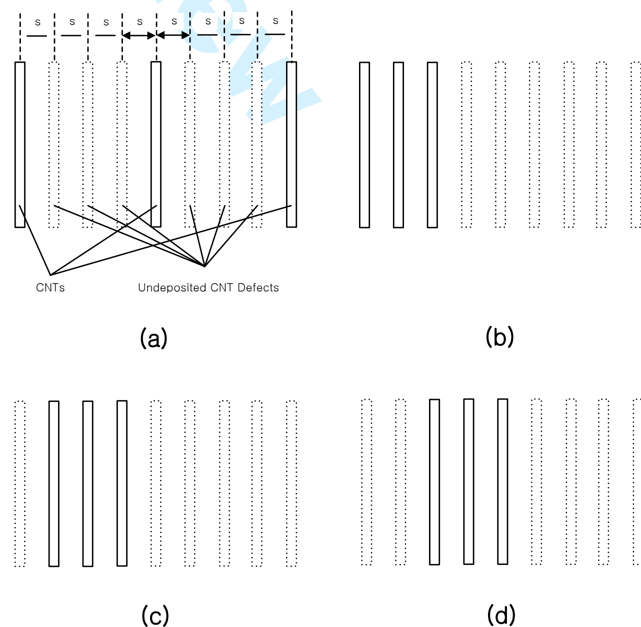

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Fig. 11. P_{CD} for largest delay ((a)) and P_{CD} for least delay ((b), (c), and (d)) (V_{GS}=0.9V, (19,0), N=9, N_{CD}=6, W_g=32nm)

For current technology, CNT synthesis techniques yield ~33% metallic CNTs; however, [16] has reported 4% metallic CNTs. Other CNT defects (due to misposition and mis-alignment) can occur [5]; 99.5% of all CNTs can be correctly aligned when the average density of the CNTs is 5-10 CNTs/µm. However, 250 CNTs/µm is required to ensure better performance (delay and energy) than silicon-CMOS [15]. This higher CNT density is used in this paper to measure the performance degradation with respect to an ideal CNTFET performance. Compared with [5] at least a 10% decrease in probability of correct alignment can be expected for more than two orders of magnitude increase in density [17,18], i.e. it is assumed that 90% of all CNTs are aligned when the CNT density is 250 CNTs/µm. As no relation has been established between the presence of metallic CNT and mispostioned (and misaliged) CNTs, p_{CD} can be calculated probabilistically as below in (19)

$$\begin{aligned} p_{CD} &= p_{CD_Metallic} + p_{CD_Mis-positioned} - p_{CD_Metallic} \times p_{CD_Mis-positioned} \\ &= 0.04 + 0.2 - 0.04 \times 0.2 \\ &= 0.232 \end{aligned} \quad (19)$$

Based on (19), $PROB_{PCD}$ can be calculated as function of N_{CD} using (18); the results are plotted in Figure 12. The average delay increase (in % from Figure 8) and RSD (in % from Figure 11) are also depicted in Figure 12. Figure 12 shows that $PROB_{PCD}$ decreases as N_{CD} increases; also, the average delay increases exponentially, and RSD cannot be ignored.

Previously, it has been shown that the delay is not strictly related to N_{CD} and there exist many configurations (P_{CD}) for which the intervals are the same (as shown in Figures 11 (b), (c), and (d)). The number of configurations (in this case denoted as N_{PCD}) with same interval(s), is dependent on the interval values, N_{CD}, and N. So, the corresponding $PROB_{PCD}$ that results in the largest ($PROB_{PCD_Largest}$) or least delay ($PROB_{PCD_Least}$), depends on N_{CD} and N . They can be calculated using (18), as

$$\begin{aligned} PROB_{PCD_Large} &= (N_{PCD_Large} / N_{CCD}) \times PROB_{PCD} \\ PROB_{PCD_Least} &= (N_{PCD_Least} / N_{CCD}) \times PROB_{PCD} \end{aligned} \quad (20)$$

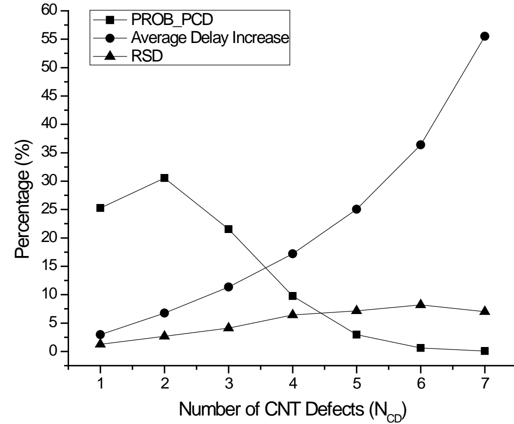

Fig. 12. $PROB_{PCD}$, Delay Increase, and RSD vs. Number of CNT Defects (N_{CD}) (V_{GS}=0.9V, (19,0), N=9, W_g=32nm)

$N_{PCD_Largest}$ and N_{PCD_Least} can be found by selecting the largest and least values of the configurations with the largest and least delays for $C_{gg,CNTFET}$ in Algorithm 1 (when N_{CD} and N are given as inputs). $PROB_{PCD_Largest}$, $PROB_{PCD_Least}$, $N_{PCD_Largest}$, N_{PCD_Least}, and N_{CCD} are reported as function of N_{CD} for N=9 in Table 3. When comparing $PROB_{PCD_Largest}$ with $PROB_{PCD_Least}$, the values of $PROB_{PCD_Largest}$ are smaller than for $PROB_{PCD_Least}$ because, in general, $P_{CD_Largest}$ requires configurations with large intervals and the number of such configurations is very small (P_{CD_Least} is found in configurations with small intervals, such that most CNTs are deposited and N_{PCD_Least} increases linearly as N_{CD} is increased).However, $PROB_{PCD_Least}$ does not simply increase as N_{CD} is increased because N_{CCD} changes differently; for example, when N_{CD} is 4 and 5, N_{CCD} has the largest value, and N_{CCD} decreases when N_{CD} increases or decreases from 4 or 5. As the values of N_{CCD} are larger than those of N_{PCD}, then the probability for least delay is affected more by N_{CCD} than N_{PCD}.

VI. Conclusion

This paper has presented a new analytical model for characterizing the delay performance of a CNTFET when undeposited CNTs occur as defects in the deposition/growth process for fabrication. One of the defect types that can occur when fabricating a CNTFET, is the absence of some CNTs following the deposition/growth step. It has been shown that this type of defect will change the operational characteristics of a CNTFET because drain current, gate capacitance, and delay are affected due to the lower number of CNTs present in the channel of the transistor. Hence, a new model by which the drain current, the gate capacitance and the delay are found when not all CNTs are deposited has been proposed. The uneven CNT spacing in the channel results in new equations that are still applicable for both defective and defect-free CNTFETs. The proposed model has been implemented in MATLAB and has been extensively simulated to show that defects due to undeposited CNTs have a significant impact on the operation of a CNTFET. Delay as degradation in performance is shown to be

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related to both the number and position of the defects; an extensive delay analysis on both deterministic and probabilistic basis has been presented.

TABLE III
CONFIGURATION PROBABILITY FOR LARGEST AND LEAST DELAYS
(V_{GS}=0.9V, (19,0), N=9)

Probability	N_{CD}						
	1	2	3	4	5	6	7
$PROB_{PCD_Largest}$ (%) ($N_{PCD_Largest}$,,N_{CCD})	5.616 (2,9)	0.848 (1,36)	0.513 (2,84)	0.077 (1,126)	0.047 (2,126)	0.007 (1,84)	0.002 (1,36)
$PROB_{PCD_Least}$ (%) (N_{PCD_Least}, N_{CCD})	5.616 (2,9)	2.545 (3,36)	1.025 (4,84)	0.387 (5,126)	0.140 (6,126)	0.049 (7,84)	0.017 (8,36)

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