



Design and Performance Evaluation of Radiation Hardened Latches for Nanoscale CMOS

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Design and Performance Evaluation of Radiation Hardened Latches for Nanoscale CMOS

Sheng Lin, *Student Member, IEEE*, Yong-Bin Kim, *Senior Member, IEEE*, and Fabrizio Lombardi, *Fellow, IEEE*

Abstract— Deep sub-micron/nano CMOS circuits are more sensitive to externally induced radiation phenomena that are likely to cause the occurrence of so-called soft errors. Therefore, the tolerance of the circuit to the soft errors is a strict requirement in nanoscale circuit designs. Since the traditional error tolerant methods result in significant cost penalties in terms of power, area and performance, the development of low-cost hardened designs for storage cells (such as latches and memories) is of increasing importance. This paper proposes three new hardened designs for CMOS latches at 32nm feature size; these circuits are Schmitt trigger based, while the third one utilizes a cascode configuration in the feedback loop. The Cascode ST latch has 112% higher critical charge than the conventional reference latch with only 10% area increase. A novel design metric (QPAR) for latches is introduced to assess the overall design effectiveness such as area, performance, power, and soft error tolerance. The novel metric (QPAR) shows the proposed cascode ST latch achieves up to 36% improvement in terms of QPAR compared with the existing hardening designs. Monte Carlo analysis has confirmed the robustness of the proposed hardened latches to PVT variations.

Index Terms—Radiation hardening, Nanoscale CMOS, Hardening latch, Circuit reliability, Robust design

I. INTRODUCTION

AS nanotechnology is fast moving from explorative to industrial practice, the operation of nanoscale circuits has been extensively analyzed. Due to the lower V_{dd} and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, thus making circuits more susceptible to spurious voltage variations caused by externally induced phenomena such as radiation due to cosmic ray neutrons and α -particles [1]. These energy particles travel through the silicon bulk and create minority carriers that may be collected by the source/drain diffusion, thus altering the voltage value of the nodes. This is particularly deleterious for storage cells such as memories and latches because data integrity is affected. The occurrence of this type of event may result in transient faults (TFs) as widely reported in the technical literature [22]. If a TF is latched by a sampling element (latch), then this may result in a so-called soft error (SE). The soft

error rate (SER) is defined as the rate at which a device (circuit or system) is expected to encounter soft errors. SER occurrence is significantly higher for deep submicron/nano CMOS [2]. Many error tolerant methods for soft errors occurring in logic circuits have been proposed. The cost in terms of area, speed, and power for protecting memories and latches from a TF can be significant. Therefore, data integrity against TFs is of the utmost importance for general-purpose applications. For SEs due to TFs affecting a sampling element, hardening has been proposed for robust design of memories and latches [3] - [7].

The objective of this paper is to propose novel low power and higher soft error tolerant designs for radiation hardening latch circuits in CMOS at the 32nm feature size. By addressing the design issues in the initially proposed in [15] in more detail, this paper presents the analysis of the novel features in detail and compares these designs with existing hardened latch configurations found in the technical literature [6] [7] [16] along with extensive simulations results. Tolerance to soft errors is achieved due to a higher critical charge that is also complemented by higher performance metrics such reduced area overhead. A metric (denoted as QPAR) to assess hardening as well as design figures of merit (such as delay, area and power) is introduced to compare the proposed latches with existing configurations. Area efficiency of the proposed latches is compared with the conventional hardening latches based on actual layout. Extensive simulation results are used to assess and compare the effectiveness of the new designs. It is shown that the proposed latches offer considerable advantages at the 32 nm feature size (using its predictive technology file) based on QPAR. An assessment of the process variation impact is also provided using Monte Carlo simulation.

II. EXISTING HARDENED LATCHES

A. Reference Latch

Fig.1 shows a widely used latch circuit, which is referred to as the reference latch in this paper. D denotes the input node, CLK and NCLK are the system clocks, node In1, lo1 and nq are the internal nodes belonging to the latch feedback loop, and Q is the latch output node. As reported in [8], the critical charge, Q_{crit} , is estimated only at specific nodes having a lowest Q_{crit} . Such nodes can be experimentally identified by inspection. Once they are identified, current pulses that model charge generation using

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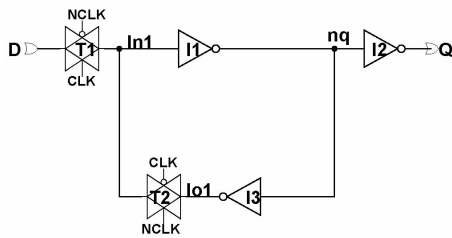


Figure 1. Reference (unhardened) latch

HSPICE are applied to these nodes. Experimental results show that the value of Q_{crit} at node In1 is the lowest among nodes In1, nq, and lo1. Furthermore, this is only one tenth of Q_{crit} of the other two nodes.

B. Existing Hardened Latches Designs

Most of the existing hardened latch designs hardening is achieved by increasing the capacitance of some nodes or the strength of their transistors in the design [7]. The addition of gate capacitance to a critical node is one of the common methods to harden CMOS devices. A soft error masking latch using Schmitt trigger circuit (SEM-latch) has been proposed in [7]. Schmitt trigger has a larger hysteresis property in voltage so that it can mask a transient pulse on the input. Meanwhile, it also increases the critical charge of node In1. As shown in Fig.2, transistors M1 and M2 are added to the reference latch to make a Schmitt trigger. The equivalent gate capacitance at node In1 is increased, thus also increasing the critical charge at node In1. A split internal node low-cost latch (SIN-LC latch) has been proposed in [6]. Rather than adding node capacitance, the SIN-LC latch utilizes an alternative feedback approach to harden the node [6]. In this paper, two inverters are added to the SIN-LC latch of [6] for a fair comparison with the reference latch design. However, the input-output delay worsens its performance due to conflicts between the transistors at the feedback loop and the latch input driver [6]. A SER-tolerant path-exclusive latch has been proposed in [16]. The SER-tolerant path-exclusive (STPE) latch employs a standard path-exclusive latch and a DICE-like [3] redundant clocked keeper to achieve a high SER-tolerance. As for the STPE latch, an inverter is added to the output of the STPE latch for comparison with the reference latch design, i.e. the inverter is required to generate the output. For the STPE latch, the redundant circuits stop the glitches from propagating to the output node. However, as shown later in this manuscript, the redundant circuitry incurs in a high area penalty and large power consumption, thus limiting its application in design.

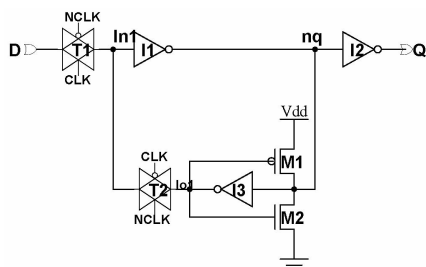


Figure 2. A Schmitt trigger based hardening latch

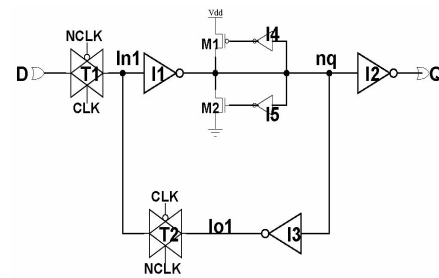


Figure 3. Modified soft error masking latch design

III. PROPOSED HARDENED LATCHES

In this section, three new designs of hardened latches are proposed and analyzed.

A. Modified SEM-Latch

The Schmitt trigger configuration used in the SEM-latch is shown in Fig.2. This design can mask a transient pulse on the input node D when CLK is high because the Schmitt trigger can suppress the glitches on the input. However, a TF will still propagate when a larger transient pulse strikes the node In1 and the positive feedback loop from M1 and M2 (together with inverter I1) amplifies the transient pulse. Thus, a TF causes a SE on the latch. The SEM-latch provides little improvement to the critical charge on node In1. A modification of the SEM-latch design can, however, provide a significant improvement in critical charge. This new design is shown in Fig.3, where the positive feedback transistors M1 and M2 in Fig. 2 are replaced by inverters I4, I5 and transistors M1, M2. In the modified soft error masking latch, the feedback scheme is retained and the positive feedback from node In1 is removed. Therefore, the modified SEM-latch can still suppress the pulses on the input node D and node In1, while improving the critical charge on node In1. Simulation results show that the critical charge of the modified SEM-latch is 2.63fC at 32nm CMOS feature size, 0.9V power supply, and room temperature, while the critical charge of the SEM-latch is 2.33fC. Therefore, a 13% critical charge improvement is achieved.

B. Alternative Schmitt Trigger Latch

Similarly to the reference latch in Fig.1, the node In1 of both the SEM-latch and modified SEM-latch is also connected to an inverter. An alternative hardened Schmitt trigger (ST) based latch is proposed in Fig. 4. In the ST latch, node In1 is connected to a Schmitt trigger that consists of six transistors [9]. When node In1 is low, node nq is high, M6 is on, and node int2 is charged. If a TF on a node goes from low to high, to change the state of node nq, the charge at node int2 needs to be discharged first. A similar scenario occurs when there is a negative pulse striking node In1. Therefore, this Schmitt trigger can provide better tolerance capabilities (robustness) to soft errors due to the charge at nodes int1 and int2. The proposed latch will be slower due to the hysteresis property of the Schmitt trigger. When CLK is low and NCLK is high, the feedback loop retains the data and the Schmitt trigger configuration provides better tolerance

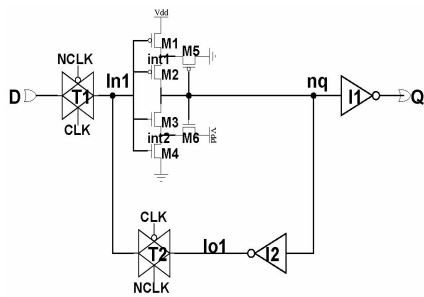


Figure 4. Proposed Schmitt trigger based latch

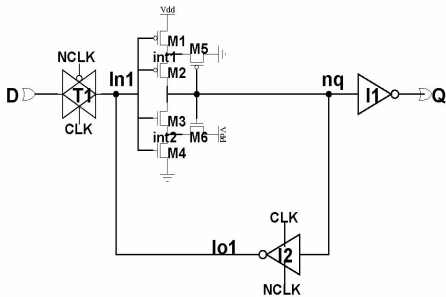


Figure 5. Cascode feedback Schmitt trigger (Cascode ST) latch

capabilities (robustness) to soft errors.

C. Cascode Schmitt Trigger Latch

In the ST latch shown in Fig.4, the feedback loop consists of an inverter I2 and a clock-controlled transmission gate T2. An alternative configuration of the feedback loop is shown in Fig.5, in which both latches work exactly the same using a digital cascode configuration. The feedback configurations in Fig.4 and Fig.5 are different from the operation of exiting the metastable state at the data-retaining phase. As reported in [13], the cascode configuration provides a better capability to exit the metastable state than the transmission gate configuration due to the reduced Miller effect that will degrade performance when used for a small-signal amplifier. Simulation results show that the ST latch with a cascode feedback (Cascode ST Latch) achieves a critical charge of 3.34fC at 32nm CMOS feature size, 0.9V power supply, and room temperature, compared to 3.00fC of a ST latch with a transmission gate feedback. When CLK is high and NCLK is low, the latches in Fig.4 and Fig.5 operate similarly, and there is no significant difference between the power and delay performance of the ST latch and the Cascode ST latch. Compared to the ST latch in Fig.4, the Cascode ST

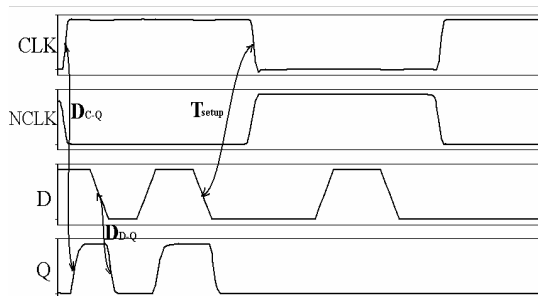


Figure 6. Timing diagram of the Cascode ST latch

latch achieves 11% critical charge improvement with no loss in power and performance.

IV. ASSESSMENT AND COMPARISON

Several hardened latches have been discussed in previous sections. Simulations have been performed to investigate the performance and the critical charge of these different hardened latches.

A. Timing and delay

Fig.6 shows the basic timing diagram of the Cascode ST latch. CLK and NCLK are the system clock, D is the data input and Q is the data output. D_{C-Q} is the propagation delay of the latch from the clock signal CLK to the output Q. D_{D-Q} is the propagation delay of the latch from the data signal D to the output Q. T_{setup} is the minimum time between a change in the data signal and the trailing edge of the clock signal such that the new value of D can propagate to the output Q of the latch and stored in the latch during the non-transparent phase. The performance of the different latches is compared based on simulations of the switching characteristics of each latch for different values of data setup as proposed in [10], i.e.

$$D = T_{setup} + D_{C-Q}. \quad (1)$$

For T_{setup} and D_{C-Q} , the max delay between positive and negative transitions (i.e. the larger value between a high to low transition and a low to high transition) is selected as the performance metric for latch. T_{setup} and D_{C-Q} of the latches are listed in Table I.

B. Area

The layouts are designed based on MOSIS deep sub-micrometer design rules [12]. Table I lists the area of the reference latch, the SEM-latch, the modified SEM-latch, the STPE latch, the ST latch, and the Cascode ST latch. The proposed ST latch has only a 10% area increase compared with the reference latch in Fig.1, and 4.7% area increase compared with the SEM-latch shown in Fig.2.

C. Critical charge

As mentioned above, the critical charge, Q_{crit} , is estimated only at specific nodes (i.e. those having a low Q_{crit}). A lower Q_{crit} between positive and negative transient pulses is selected as the critical charge of a latch.

Experimental results show that the nodes that have the lowest Q_{crit} in the reference latch, the SEM-latch, the Modified SEM-latch, and the ST latch are the same, i.e. node In1 in all circuits has the lowest Q_{crit} . Comparison of these six latches on critical charge, performance, and power consumption is presented in Table I. For fair comparisons, the latches presented in this paper have equivalent transistor sizes to keep the same transistor size ratios. In particular, all transistor sizes of the SEM-latch and the Modified SEM-latch are the same as in the reference latch. In the ST and Cascode ST latches, the transmission gate T1 (Fig.4 and Fig.5) has been increased by 50% to drive two more transistors connected to T1. Simulations have been performed on these four Schmitt trigger based latches

at 32nm CMOS feature size, 0.9V power supply, and room temperature. Table I shows that by utilizing Schmitt trigger configuration, the critical charge of the latch increases 43%, 62%, 85% and 112% for the SEM-latch, the Modified SEM-latch, the ST latch, and the Cascode ST latch, respectively, while the delay and power performance degrade at a smaller penalty. The above simulations use the predictive technology file at 32nm [14], and the simulation based on the netlists extracted from the layouts confirms the critical charge improvement of the latches. Tables I also shows that the high critical charge of the STPE latch is accomplished at the expenses of degradations in power, performance (delay), and area (in these Tables, a bold entry identifies the best value of each figure of merit among the hardened latches).

To assess the different hardened latch configurations, a comprehensive metric for performance (as a function of the delay, critical charge, area, and power dissipation) is introduced. Using the simulation results in Tables I, a comparison can then be quantitatively assessed. The proposed metric combines the first few figures of merit in Tables I: The critical charge should be as high as possible for a highly error-tolerant design. However, for high performance and low power operation, delay, power consumption and setup time should be as small as possible. An increase in critical charge can be achieved by increasing the capacitance of the critical node, but this may require larger transistors, thus increasing power consumption and area. The new metric is given by dividing the critical charge by the product of the power, delay and area, which is referred to as the charge (Q) to PDP-Area Ratio (i.e. QPAR). Therefore, the QPAR is given as follows:

$$QPAR = \frac{\text{Critical Charge}}{\text{Power} * (T_{\text{setup}} + D_c - q) * \text{Area}} \quad (2)$$

As in (2), a high value of QPAR corresponds to a high soft error tolerance, high performance (low delay/compact area) and low power in hardened latches. The QPARs of all proposed and existing latch configurations are also listed in Table I. Table I

TABLE I
COMPARISON OF LATCHES

Latch	reference latch	SEM-latch	STPE latch	Modified SEM-latch	ST latch	Cascode ST latch
Qcrit (fC)	1.62	2.33	5.00	2.63	3.00	3.44
Power Consumption (nW)	189.0	206.7	287.6	217.7	212.9	209.6
Tsetup (ps)	9	19	33	20	16	16
Dc-q (ps)	44.48	49.19	43.80	50.75	54.40	53.90
D (ps)	53.48	68.19	76.80	70.75	70.40	69.90
Area (μm^2)	1.958	2.284	2.828	2.6112	2.393	2.393
QPAR	8.2e-5	7.2e-5	8e-5	6.5e-5	8.4e-5	9.8e-5

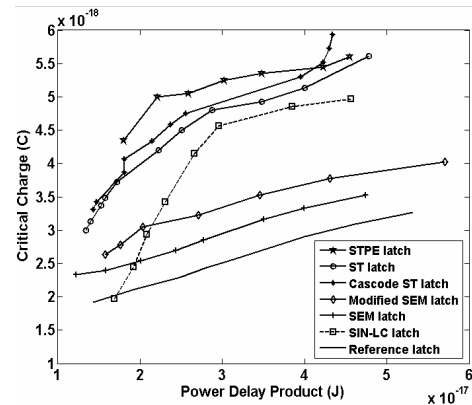


Figure 7. Plot of power-delay product vs. critical charge for different latch designs

shows that the proposed Cascode ST latch has the highest QPAR, which is 36% higher than that of SEM-latch and 22% higher than that of STPE latch.

D. Power-delay Product and Critical Charge

Soft error tolerance must not be achieved at the expense of power dissipation and performance. The power-delay product is a widely used metric for logic circuits. It is also used in this paper to establish the power and performance of the hardened latches. While area is not explicitly considered in this section, transistor sizing can have a significant impact on the critical charge of CMOS circuit [11]. The critical charge can be increased by increasing the gate capacitance at critical node. All of these techniques result in an increase of both power consumption and propagation delay of the hardened latches, thus degrading the power-delay product as metric for digital CMOS circuits.

Therefore, the relationship between the power-delay product and the critical charge for the different latch circuits is further assessed by not explicitly considering the area (as in the QPAR) as an immediate measure of performance. So the increase in transistor sizing of the hardened latches is implemented. For example, in the reference latch and the SEM-latch, the transistors of the inverter I1 are increased. For the Modified SEM-latch in Fig.3, the transistor sizes of M1 and M2 are increased. Unfortunately by utilizing an increase in gate sizing, the power-delay product will increase as well. Fig.7 shows the relationship between the power-delay product and the critical charge on the reference latch, the SEM-latch, the Modified SEM-latch, the SIN-LC latch, ST latch, Cascode ST latch, and STPE latch. As shown in Fig.7, the SEM-latch and the Modified SEM-latch utilize a parallel additional inverter to the existing feedback loop during the non-transparent state, so they have a similar slope in the plot. The ST latch, the Cascode ST latch, STPE latch, and the SIN-LC latch achieve a significantly larger value of critical charge at a lower power-delay product compared to the SEM-latch and the Modified SEM-latch. The STPE latch has the highest critical charge at low values of power-delay product. However, as the transistor sizes increase, the critical charge of the Cascode ST increases faster than that of the STPE latch. As shown in Fig.7, the proposed Cascode ST

TABLE II.
CRITICAL CHARGES AND HARDENING FAILURE PROBABILITY OF LATCHES

Latch	Critical Charge (fC)	Hardening Failure Prob @ 3fC
reference latch	1.62	100%
SEM-latch	2.33	100%
Modified SEM-latch	2.63	97.76%
ST latch	3.00	43.1%
SIN-LC Latch	3.22	10.23%
Cascode ST latch	3.34	0.41%
STPE latch	5.00	0%

latch has the highest critical charge at higher values of power-delay product. Therefore, this latch should be utilized in these cases for the highest soft error tolerance.

V. PROCESS VARIATIONS

The effect of variations (process, voltage, and temperature) on soft error tolerance is increasing with technology scaling. The soft error tolerance of the latches is also evaluated in the presence of process variations. In this paper, Monte Carlo simulation based on 10K samples is used for assessing the latch design under PVT variations. To model PVT variations in the Monte Carlo simulations, parameters including voltage, temperature, and process (threshold voltage and channel length) are swept and simulations are run using a $\pm 5\%$ Gaussian distribution with variation at the ± 3 -sigma level. Table II shows the failure probability of hardening the original designs (whose QPAR is given in Table I) of the reference latch, the SEM latch, the Modified SEM latch, the ST latch, the SIN-LC latch, the Cascode ST latch, and the STPE latch when a fixed charge of 3fC is applied to the critical node of each latch. The results of Table II confirm that as the induced charge is constant, then the probability of failure of hardening is smaller when a larger Q_{crit} is present in the latch. However, difference in the probability of failure between the Cascode ST and STPE latches is negligible.

VI. CONCLUSION

This paper has presented new designs for the radiation hardening of latch circuits in nano CMOS. Novel configurations for latches have been proposed, analyzed, and simulated using the predictive technology file at 32nm [14] for tolerance to soft errors caused by radiation. By extending the initial results of [15], three configurations of the hardened latches have been proposed and designed. In all cases, simulations have shown that the proposed designs have excellent tolerance to soft errors, low delay, low power dissipation, and high performance. These figures of merit have been comprehensively assessed within a single metric, denoted as QPAR. Using QPAR, the proposed designs offers significant advantages over the existing latch configurations and provide excellent performance at the reduced feature size of 32nm. The proposed Cascode ST latch

has the highest QPAR; Monte Carlo simulation has also been performed under PVT variations. The following conclusions can be drawn from the results of this paper:

1. The STPE latch [16] has the highest critical charge and the highest tolerance at low values of PDP. However, this latch has the highest power dissipation and the largest area.
2. The SEM and the proposed Cascode ST latches have the lowest power dissipation, thus making them excellent candidates for low power designs.
3. As for performance, the SEM and the proposed Cascode ST latches have again the lowest values. Due to a very high set-up time, the STPE latch has the highest delay.
4. Using QPAR as single metric to assess all figures of merit (delay, area, power consumption and critical charge) for a hardened latch design, two of the proposed designs (the ST and the Cascode ST latches) achieve the best performance among latch configurations known to the authors. This improvement over existing designs is checked even in the highest increase in critical charge at higher values of PDP (i.e. by not explicitly considering the area of the latch).

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9 Dear Editor and Reviewers:
10

11 We would like to thank you for the constructive comments that have provided to us as part of the review
12 process for our previous manuscript submitted to IEEE TVLSI.

13 Please find enclosed below the changes appearing in the revised version (indicated in italics) of our
14 original manuscript to address your comments (also enclosed).
15
16
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18 EIC Comments

19 Please revise as a brief.
20
21

22
23 *Response: the manuscript has been revised to fit a brief format (5 pages); material has been added to*
24 *fully address the comments from the referees while overall reducing the length of the original*
25 *submission.*
26
27

28 Associate Editor

29 Comments to the Author:

30 Both reviewers agreed that the paper needs a minor revision. Please respond to the reviewers comments
31 and modify the manuscript.
32
33
34
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36 Reviewer's Comments

37 Reviewer: 1

38 SPECIFIC FEEDBACK TO AUTHORS

39 Well organized with good background information and introduction into the technical content.

40 The presentation of the data with comparisons across the spectrum of the existing and new structures
41 with a defined performance metric was good and relevant.
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46 One thing I was not sure of. Was the simulation based on layout extracted netlist? Parasitics would have
47 impact on the results and thus how a cell is laid out is relevant. Need to mention this.
48
49

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51 *Response: As mentioned in Section IV.C of the revised manuscript, simulation for the critical charge is*
52 *based on using the predictive technology file at 32nm [21]. Simulations based on the netlists extracted*
53 *from the layouts shown in the original paper submission (omitted in the revised paper due to lack of*
54 *space to fit the EIC request for a brief format of 5 pages) have confirmed the critical charge*
55 *improvement of the proposed latches. A statement has been added in the Section IV to make it clear.*
56
57

58 I saw results for only one PVT. Not enough of data point. If not, need to mention.
59
60

Response: As mentioned in Section V of the revised manuscript, PVT variations are modeled by Monte
Carlo simulation. Parameters such as voltage, temperature, and process (threshold voltage and channel

length) are swept using a $\pm 5\%$ Gaussian distribution with variation at the ± 3 -sigma level. 10K(10,000) samples were simulated to assess the impact of PVT variations. These results are reported in the revised manuscript. This experimental method has been added explicitly in the Section V of the revised paper.

The sizing of the transistors will have big impact. Not very clear of sizing relationships of the transistors in each configuration from the manuscript.

Response: This is actually a good point. As mentioned in Section IV.C of the revised manuscript, the transistors of all latches presented in this paper are equivalently sized to keep the same transistor size ratio for fair comparisons. Transistor sizing of the hardened latches is then increased in Section IV.D to investigate the relationship between the power-delay product and the critical charge. A few sentences have been added in the subsection C of the section IV in the revised manuscript.

Reviewer: 2

SPECIFIC FEEDBACK TO AUTHORS

This paper presents three new existing radiation hardened latches and also an evaluation metric QPAR. While the designs proposed are more of an enhancement to existing methods, the characterization and comparison of existing Radiation Hardened latches with the proposed ones is not comprehensive. Specifically

1) The use of SEU injection simulations, representing the high particle strike responses on the proposed latches

Response: For SPICE-level simulation as reported in the existing technical literature (references [6] and [7] in particular), particle strikes are modeled as a current source; this is injected into a node to find the amount of charge prior to the change in the value of the node itself. It is a fairly standard method to simulate the effect of the particle strike.

2) The robustness of the internal nodes for each of the latches is important factor for the radiation hardened designs. It will not only need the critical charge parameter (used in QPAR), but also the corresponding process parameters (using curve fitting methods). The QPAR only considers the power, area and the setup times.

Response: The PVT variation effects have been considered in this paper and we appreciate the reviewer's comment since it is one of the critical issues in deep submicron technology based design. The robustness of the internal nodes for each of the latches has been investigated as a function of different parameters by Monte Carlo simulation in Section V of the revised paper. The voltage, temperature, and process (such as threshold voltage and channel length) variations are modeled using a $\pm 5\%$ Gaussian distribution with variation at the ± 3 -sigma level. A 10K (10,000) samples are used in the simulation to quantify the impact of PVT variations. This PVT variation simulation method using Monte Carlo simulation has been explained and added to the revised manuscript to clarify the setup of our simulation results at the end of the Section V.

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Figure 9 is just a representation of the level-sensitive latch. Instead the authors should provide the functional simulation results of the proposed latches and compare their performances (if any degradations in the signal range).

Response: In the revised manuscript, the functional simulation results of the proposed latch are shown now in Figure 6 to reflect the reviewer's comment; this figure replaces Figure 9 in the original manuscript.

For Review Only