

A Technique for Low Power Dynamic Circuit Design in 32nm Double-Gate FinFET Technology

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Abstract— In this paper, a new technique is presented for low power high-speed dynamic circuits design using double gate FinFET. In this technique, the clock signal is used to control the threshold voltage of the front gate; the threshold voltage of the front gate is reduced during the evaluation phase for a fast transition and increased during the pre-charge or standby phase to reduce the leakage current (this is accomplished by connecting the back gate to the clock signal of the dynamic circuit). By controlling the threshold voltage of the FinFET, the proposed technique achieves a power reduction of up to 34%, and no delay compared to other approaches at a 32nm feature size.

I. INTRODUCTION

The dramatic scaling of CMOS technology has led to a large increase in energy consumption for both active and idle states. This problem will likely continue in the future due to the large integration density and transistor leakage current in VLSI designs. Furthermore, leakage power has been the major contributor to total power due to short-channel effects and the long standby time in circuit operation. These trends have been challenging issues for heat dissipation and battery lifetime, so it is important to develop efficient techniques to handle and reduce energy consumption, while retaining other performance metrics such as circuit speed. For example by tuning V_{dd} into the sub-500mV regime, more than 80% of switching power can be saved [1][2]. However, scaling of the supply voltage alone leads to a heavy penalty in circuit speed and data stability; in particular, this occurs when V_{dd} is close to or below the threshold voltage (V_{th}).

By considering trade-offs between performance and leakage power, V_{th} must be controlled dynamically for a low-voltage design: V_{th} should be scaled down for high performance active switching and should be maintained high in the idle mode to reduce leakage. Such a dynamic V_{th} control technique will provide low power consumption with no speed degradation (as switching power is almost independent of V_{th} scaling).

Several approaches have been proposed to dynamically control the threshold voltage; these include dynamic-threshold voltage MOS (DTMOS) [4], body biasing [5], and multiple-threshold CMOS (MT-CMOS) [6]. However, these approaches have significant limitations. To overcome them, a novel design technique is proposed in this paper. By taking advantage of the independent double gate FinFET, V_{th} is controlled dynamically by biasing the back gate especially for designing dynamic domino circuits. Extensive simulation results are provided; they show that the proposed technique is readily applicable to a 32nm technology.

Section II gives an overview of the FinFET technology and proposes a circuit model for detailed analysis and optimization. In Section III, the proposed technique for designing dynamic domino circuits is presented, while Section IV shows the simulation setup and results, followed by conclusion in section V

II. FINFET TECHNOLOGY

The FinFET transistor is a vertical double-gate device and is regarded as a promising alternative device for sub-45 nm bulk devices [7]. Figure 1 illustrates the 3D structure of a FinFET. In this paper, the model of the FinFET is configured as a pair of FD (Fully Depleted) SOI devices, in which the source and drain of a device are connected to those of the other device.

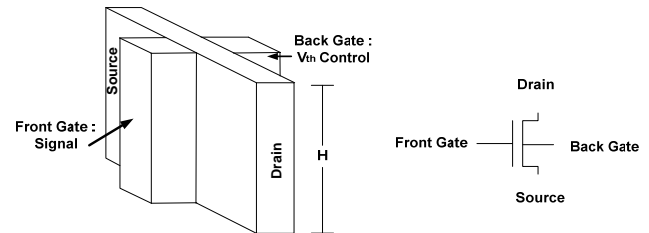


Figure 1. FinFET structure and symbol

Figure 1 shows the structure of a multi-fin double-gate FinFET device [8]. Current flow is parallel to the wafer plane; the thickness t_{si} of a single fin is equal to the silicon channel thickness. Each fin provides the width of device, where H denotes the height of each fin. HSPICE has been used to study FinFET and bulk CMOS circuit behavior using the Predictive Technology Model for 32 nm FinFET and 32 nm bulk CMOS technologies.

One of unique properties of the FinFET is the electrical coupling between the front and back gates. One of the implication of this coupling is that the threshold voltage of the front gate (V_{thf}) is not only governed by process, but also it can be controlled by the back gate voltage (V_{Gb}). This is similar to the body effect in a bulk transistor. This coupling effect can be modeled as a capacitive partition among the gate capacitance (C_{oxf} and C_{oxb}) and the silicon body capacitance (C_{si}) as

$$\partial V_{Thf} / \partial V_{Gb} = -(C_{si} \parallel C_{oxf}) / C_{oxf} \propto t_{ox} / t_{si} \quad (1)$$

The threshold voltage of the front gate can be reduced during switching (i.e., V_{Gb} is high) and increased during standby (i.e., V_{Gb} is low) by controlling the back gate bias. Therefore, the V_{th} of a FinFET is dynamically tunable depending on the operation mode as well as other technology parameters (i.e., t_{ox} and t_{si}).

Given a FinFET device, the difference in V_{th} (ΔV_{th}) between the high and low states is the highest by reducing the body thickness and increasing the gate oxide thickness (Eq. (4)[9]). In practice for a low-power design, a larger ΔV_{th} is preferred for high-speed and low leakage while V_{Gb} is varied between 0 and V_{dd} .

To maximize ΔV_{th} , t_{ox} and t_{si} have to be optimized [9]. If ΔV_{th} is given by 100mV, then t_{ox} and t_{si} are 2.1nm and 8nm, respectively. A thicker t_{ox} and a thinner t_{si} are preferred to increase the ratio of t_{ox} / t_{si} , and in turn, a larger ΔV_{th} value is accomplished, i.e. this is favorable for the best balance between high switching speed and better leakage control. For selecting the threshold voltage change ΔV_{th} , t_{ox} and t_{si} will be constrained by design objectives, the selected application and the process feasibility.

III. LOW POWER DESIGN OF DYNAMIC CIRCUITS IN FINFET

The leakage current characteristics of dynamic CMOS circuits have been analyzed in [10] and several techniques for low leakage dynamic circuit design in CMOS technology have been proposed in [10][11][12]. Most of these techniques use MTCMOS technology or a sleep transistor (thus requiring an additional type of transistor and an expensive technology). Therefore, these dynamic CMOS-based circuit design techniques are not suitable for designs using FinFET. FinFET can replace MTCMOS technology because it is simple to control the threshold voltage for speed and low power operation with no need for an additional type of device.

A. Proposed technique

Adapting dual-Vt transistors for subthreshold leakage current reduction in dynamic logic circuits was first proposed

by Kao [11]. The critical signal transitions that determine the delay of a dynamic domino logic circuit occur along the evaluation path. Therefore in a dual-Vt domino circuit, all of the transistors that can be activated during the evaluation phase, have a low-Vt. The precharge phase transitions are not critical for the performance of the dynamic circuit; therefore, those transistors that are active during the precharge phase, have a high-Vt for leakage current. The clock is gated high, turning off the high-Vt precharge transistor when a dynamic logic circuit is active. Dynamic domino circuits using FinFET rely on the same methods to reduce the subthreshold leakage current. Precharging PMOS FinFETs have a high V_{th} , while the pull-down network NMOS FinFET transistors have a low V_{th} during the evaluation phase (they have a high V_{th} in idle mode). A variable threshold voltage can be achieved by controlling the FinFET's back gate voltage V_{Gb} .

Figures 2 and 3 show the proposed method for designing dynamic circuits using FinFET, in which V_{th} depends on the back gate voltage. For a NMOS FinFET, a high V_{Gb} makes V_{th} low and a low V_{Gb} makes V_{th} high. For a PMOS FinFET, the reverse scenarios are applicable. Usually the inputs of the circuits are connected to the front and back gates. For a NMOS FinFET, if the input is high, then V_{th} will be reduced by a high V_{gb} (gate voltage of the back gate) to make a fast signal transition. If the input is low, then V_{th} will be high due to a low V_{gb} . However by connecting the front and back gates together more leakage current will be generated in the presence of many high input states (this occurs because these inputs make V_{th} low). In this paper, a new design technique is presented to overcome these problems by modifying V_{th} using V_{gb} . This technique connects the clock signal to the back gate of the precharging PMOS transistor; this modifies V_{th} using V_{gb} in the right direction to reduce the leakage current, while preserving the desired level of performance.

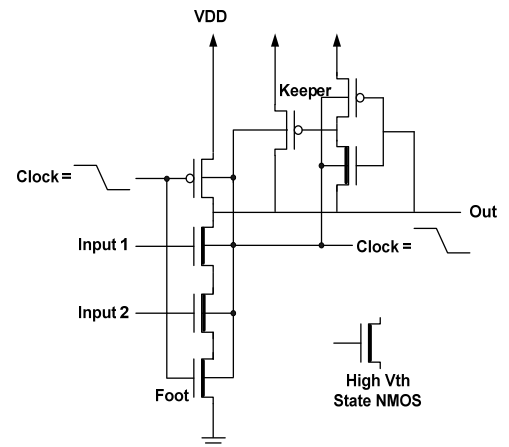


Figure 2 Proposed dynamic circuit in precharging

Sometimes, it is necessary to design dynamic domino circuits such that the precharging time becomes faster depending on the application and design style. If the clock signal is connected to the back gate of the PMOS precharging transistor, then V_{th} will be lower. So, the precharging process can be fast. Similarly, if the clock is connected to the back gate of the NMOS FinFET and the clock is low, then V_{th} will

be high. This increase in V_{th} contributes to a reduction of the leakage currents.

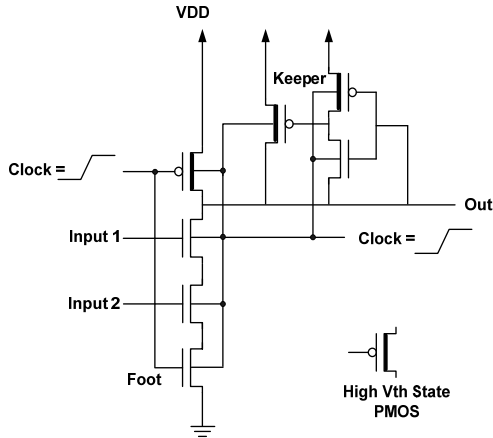


Figure 3. Proposed dynamic circuit in evaluation

During the evaluation phase, fast signal transitions are desirable because the delay of a dynamic circuit is determined by the signal evaluation path. If the back gate is connected to the clock, during the evaluation period, the V_{th} of the NMOS FinFET is low and the V_{th} of the PMOS FinFET is high. This results in fast transition in NMOS Pull down circuit and PMOS FinFET will have low subthreshold leakage current.

IV. SIMULATION RESULTS

A. Simulation Setup

To show the efficacy of the proposed design technique, a set of domino bench mark circuits have been designed and simulated with two different circuit design techniques in 32nm double gate FinFET technology; the first scenario is the “tied” case in which front and back gates are tied together; the second scenario (referred to as “clock”) corresponds to the case in which the front gate is connected to the input signal and the back gate is connected to the clock signal

The device parameters of the technology are given as follows; $V_{thn0} = |V_{thp0}| = 0.22V$ and $V_{dd}=0.8V$, $t_{si} = 8.4nm$, $t_{ox} = 2.1nm$. A 3.3GHz clock signal is used for the dynamic circuits. For comparison, the circuits are sized to have the same worst-case propagation delay for both scenarios. To compare the results, 2-input, 4-input domino AND gates, 2-input, 4-input OR gates, and a dynamic full adder have been designed and simulated. The two sets (“tied” and “clock”) of circuits have been designed to and simulated compare using HSPICE. The activity factor, α , is assumed to be 0.01 throughout this analysis. A lower value of α will be more favorable to the results of this study, as the leakage power will account for a larger portion of the total power consumption.

B. Threshold Voltage Changes

The change in threshold voltage has been simulated for various V_{Gb} and constant V_{Gf} of 1V. Figure 4 shows that as V_{Gb} is changed, V_{th} also changes in the opposite direction. To increase ΔV_{th} , a thicker t_{ox} and a thinner t_{si} are desirable as described in the previous section.

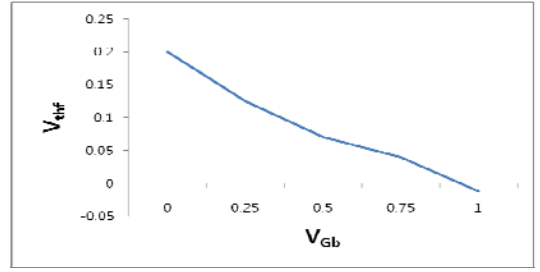


Figure 4. Threshold voltage when V_{Gb} is applied and $V_{Gf} = 1$

Table I shows the leakage current for various V_{th} in NMOS FinFet. Like traditional CMOS transistor, large amount of leakage current flows in NMOS FinFET when the V_{th} is low. On the other hands, high V_{th} keep the leakage current very low

TABLE I. LEAKAGE CURRENT ACCORDING TO THE V_{th}

V_{th}	0.35	0.3	0.25	0.2
$I_{leakage}$	8.93nA	46.4nA	234nA	1.12 μ A

C. Leakage Power Consumption and PVT

The leakage power consumption of a full adder circuit for both scenarios is shown in Figure 6. Front and back gate tied circuits (named ‘tied’ in Figure 6) consume more power than the proposed approach, in which the front gate is connected to the input signal and the back gate is connected to the clock signal. When the input signal is high, then V_{th} of the NMOS is reduced, causing a high leakage current. If the circuits stay in the idle state or pre-charge state, leakage will be reduced for NMOS with a low V_{th} . This is shown by the simulation results of Figure 6. When the gates have the same delay with the same power supply voltage, the power consumption of the front and back gate tied circuit is almost 34% lower than “clock” circuits. The proposed technique shows that it saves leakage current in the pre-charging period by controlling V_{th}

Comparison of power consumption is shown in Figure 6 for dynamic AND2, AND4, OR2, OR4, and the full adder circuit. The energy consumption is measured at the same speed for all gates to ensure a fair comparison. These results are normalized with respect to the ‘tied’ circuit. In all cases, the proposed method consumes less power. If the clock is applied to the back gate, V_{th} fluctuates between V_{thmin} and V_{thmax} and the average is almost $(V_{thmin} + V_{thmax})/2$. Note that the speed of the ‘clock’ circuit is same as the ‘tied’ circuit because in the evaluation mode (that determines the propagation delay of a domino circuit), both of them have the same V_{th} . In the precharging mode, ‘clock’ circuits have a low V_{th} while ‘tied’ circuits have high or low V_{th} depending on the input value.

Figure 7 shows the leakage current profile of the 2-input NAND dynamic circuit for process, temperature, and threshold voltage variation (PVT). With the threshold voltage changing, the leakage current changes exponentially, and the leakage current increases rapidly as temperature increases, especially for low V_{th} .

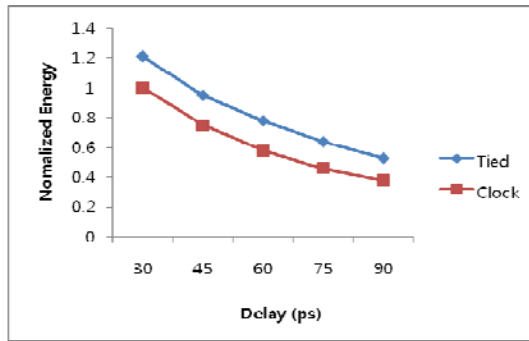


Figure 5. Normalized energy consumption of full adder by delay.

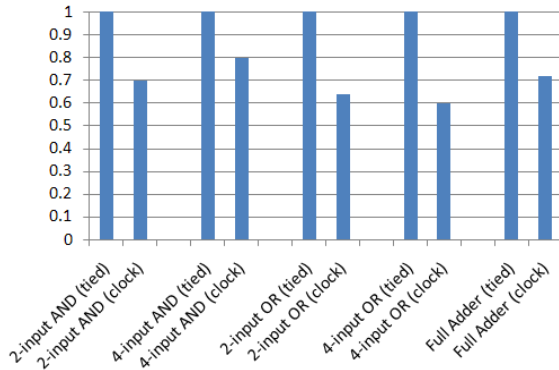


Figure 6. Normalized energy consumption of the dynamic 2-input AND, 4-input AND, 2-input OR, 4-input OR, full adder 'tied' and 'clock' circuits

However, by controlling the threshold voltage of the dynamic circuits during evaluation period as well as pre-charge period, a significant amount of power can be saved.

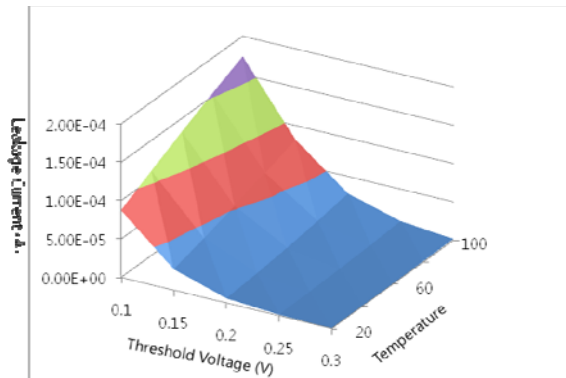


Figure 7. Process variation for leakage current with threshold voltage and temperature

This can be done by connecting the back gate to the clock signal of the dynamic circuit as described in this paper, which reduces the threshold voltage of the front gate during the evaluation phase for a fast transition and increases the threshold voltage during the pre-charge or standby phase to reduce the leakage current. The effect of this technique is more manifest at high temperature since the leakage current

increases rapidly at high temperature as shown in Figure 7.

V. CONCLUSIONS

In this paper, a high speed low power dynamic circuit design technique has been presented for FinFET technology. Using the characteristics of dynamic V_{th} control in a FinFET device, a low leakage power dynamic circuit can be designed without degrading operational speed. A thicker t_{ox} and a thinner t_{si} cause an increase in the difference in V_{th} between switching and the standby modes. The circuit can control V_{th} dynamically and efficiently by applying the clock signal to the back gate of the FinFET device. During the pre-charging period, V_{th} of PMOS is controlled low so that a fast pre-charging can occur; the V_{th} of NMOS is controlled high to keep the low leakage state with a high V_{th} . During the evaluation period, V_{th} of the PMOS is high while in the NMOS it is low; therefore, this accomplishes fast signal switching and a low leakage current in the PMOS. In the implementation of a logic circuit, more than 36% in energy reduction can be achieved using the proposed technique and controlling V_{th} dynamically; moreover circuit performance is preserved, i.e. no degradation in speed is encountered.

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