

# A 32nm SRAM Design for Low Power and High Stability

Sheng Lin, Yong-Bin Kim and Fabrizio Lombardi  
Department of Electrical and Computer Engineering  
Northeastern University  
Boston, MA, USA

**Abstract**—A SRAM cell must meet stringent requirements for operation in the sub-micron/nano ranges. A nine transistor (9T) cell at a 32nm feature size in CMOS is proposed to accomplish improvements in stability, power dissipation and performance compared with previous designs for low-power memory operation. Initially, this paper presents the optimal transistor sizing for this 9T SRAM cell considering stability, energy consumption, and delay. A write bitline balancing scheme is proposed to reduce the leakage current of the SRAM cell. By optimizing size and employing the proposed write circuitry scheme, a saving of 32% in power dissipation is achieved in memory array operation compared with a conventional 6T SRAM based design. The impact of process variations is investigated in detail, and the HSPICE simulation shows that the 9T SRAM cell has an excellent tolerance to process variations.

## I. INTRODUCTION

Advances in CMOS technology have made it possible to design chips for high integration density, fast performance, and low power consumption. To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to very small features and dimensions. Over the last few years, devices at 45nm have been manufactured; the deep sub-micron/nano range of 32nm is foreseen to be reached in the very near future.

Technology scaling results in a significant increase in leakage current of CMOS devices. As the integration density of transistors increases, leakage power has become a major concern in today's processors and SoC designs. Considerable attention has been paid to the design of low-power and high-performance SRAMs as they are critical components in both handheld devices and high-performance processors. Different design remedies can be undertaken; a decrease in supply voltage reduces quadratically the dynamic power and reduces leakage power linearly to the first order. However, with an aggressive scaling in technology as predicted by the Technology Roadmap, substantial problems have already been encountered when the conventional six transistors (6T) SRAM cell configuration is utilized at an ultra-low power supply; this cell shows poor stability at very small feature sizes. Moreover, the hold and read static noise margins are small for robust operation at a feature size of 32nm. A nine transistors (9T) SRAM cell configuration is proposed in this paper, which is amenable to small feature sizes encountered in the deep sub-micron/nano CMOS ranges. Compared with the 8T and 10T cells of [1] and [2],

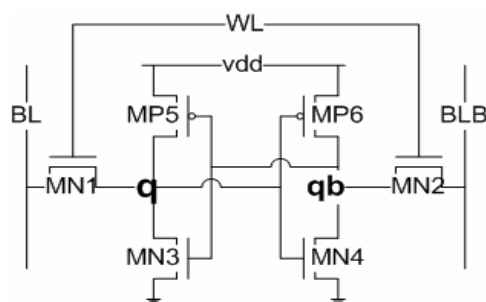


Figure 1. Conventional 6T SRAM cell

the 9T scheme offers significant advantages in terms of power consumption.

The objective of this paper is to investigate the transistor sizing of the 9T SRAM cell for optimum power and delay. An innovative precharging and bitline balancing scheme for writing operation of the 9T SRAM cell is also proposed for maximum standby power savings in an SRAM array. HSPICE simulation results confirm that the proposed scheme achieves 32% of power savings compared to the conventional SRAM cell array based on the 6T configuration.

The paper starts with introducing the proposed 9T cell and the design method used to find the optimal transistor sizing for the proposed SRAM cell. Then, the leakage current paths in the 9T SRAM cell are shown, and the bitline balancing scheme is proposed to reduce the standby leakage current. Finally, the impact of process variation on the cell's stability and power consumption is analyzed to show that the 9T SRAM cell has a very good tolerance in the presence of process variations.

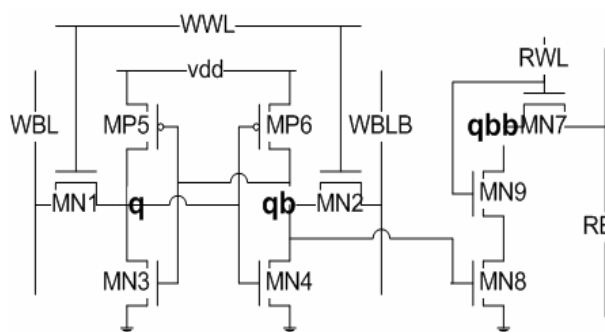


Figure 2. Proposed 9T SRAM cell

## II. OPTIMAL SIZING FOR 9T SRAM CELL

### A. Proposed 9T SRAM Cell

Issues due to process variations and power supply voltages have been reported for conventional SRAM cells. The conventional 6T SRAM cell shown in Fig. 1 has been found to be rather unstable at deep sub-micron/nano scales since the cell fails to meet operational requirements due to a low read Static Noise Margin (SNM). A 9T structure is proposed to improve the SNM by separating the read access structures of the original 6T cell, thus making the read SNM equal to the hold SNM. Fig. 2 shows the proposed 9T SRAM cell. Similarly to the 8T cell of [1], the configurations from MN1 to MN4 and from MP5 to MP6 are unchanged (same as the one in the 6T SRAM cell). The read SNM margin is maintained by retaining the write access circuit and adding a NMOS transistor (MN9) between MN7 and MN8. As shown in [2], the leakage current through MN7, MN8, and MN9 can be reduced significantly by the so-called stack effect when MN7 and MN9 are off.

### B. Sizing of Conventional 6T cell

The SRAM cell should be sized as small as possible to achieve high density in memory design. However, issues related to robustness impose a sizing constraint to the 6T SRAM cell. Fig. 1 shows the conventional 6T SRAM cell configuration. The transistor ratio between MN3 and MN1 must be greater than 1.2 to keep a proper SNM during the read operation [3]. However, in the 9T SRAM cell, when the read is enabled (RWL=1), the read bitline (RBL) is conditionally discharged through the pull-down transistors MN7, MN9, and MN8 depending on 'qb'. The cell node is isolated from the bitline during the read operation, thus retaining a hold mode SNM. Therefore, the transistor ratio between MN3 and MN1 can be decreased to achieve better performance in its operation.

### C. Optimal sizing of 9T SRAM cell

#### 1) Power-delay Product

Power-delay optimization is one of the most critical issues in digital circuit design. As the pull down transistors NM3 and NM4 are the largest transistors, power consumption of the cell will decrease most when these transistors are scaled down. As the loading capacitance of the access transistors NM1 and NM2 decreases, a decrease in the write delay will also be attained. Fig. 3 shows the power-delay product of the 9T

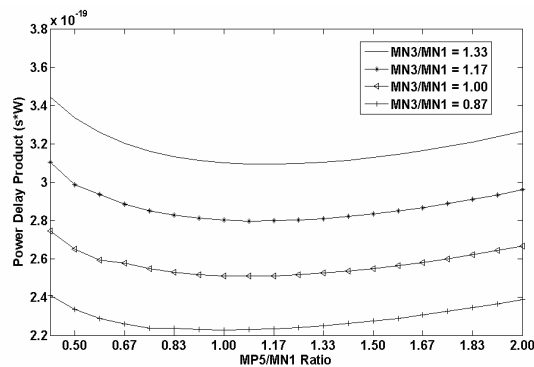


Figure 3. Power-delay product plot of the 9T SRAM cell

SRAM cell at 0.6V of the power supply voltage for various transistor sizes. As the transistor size of MN3 decreases, the ratio between MN3 and MN1 decreases, thus both power consumption and write delay of the SRAM cell decrease. Fig. 3 also shows that the lowest power-delay product is achieved when the ratio between the pull up transistor MP5 and the access transistor MN1 is equal to 1.00. By taking the cell area into consideration, the optimal value for MP5/MN1 occurs at 0.83.

#### 2) Stability Constraints

Pull down transistors NM3 and NM4 cannot be scaled down much due to stability considerations. Proper data retention strength is needed for the SRAM cell, especially for the 9T cell that must operate at an ultra-low power supply. The stability of a SRAM cell is usually defined by the SNM as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit [4]. The SNM can be graphically measured on the butterfly curve. However, its drawback is the inability to measure the SNM with automatic inline testers because the static current noise margin (SINM) still has to be derived by mathematical manipulation of the measured data after measuring the butterfly curves of the cell. An alternative definition for SRAM stability is based on the N-curve of the cell [5] as measured by inline testers. The typical N-curve of the SRAM cell is measured by reading the input current at the internal storage node when sweeping the storage node voltage from 0V to V<sub>dd</sub>.

A voltage is swept from 0V to V<sub>dd</sub> at node "qb" in Fig. 2 and the N-curves of the 9T SRAM cell at different MN3/MN1 ratios are extracted. Finally, the same voltage sweep is applied to the node "qb" of the 6T cell during a read operation. Fig. 4 shows the N-curves of the SRAM cells for different transistor size ratios. The voltage difference between points A and B indicates the maximum tolerable DC noise voltage at node "qb" prior to changing its content. This metric is referred to as the static voltage noise margin (SVNM). The peak current between A and B can also be used to characterize the stability of the cell. This metric is referred to as the static current margin (SINM). It is defined as the maximum value of DC current that can be injected in the SRAM cell prior to a change in its content. Fig. 4 shows that when the MN3/MN1 ratio is 1.00, the SINM of the 9T cell is still larger than the read SINM of the 6T cell while the larger SVNM of the 9T cell is retained due to the separate read and write operations. Table 1 shows the noise margin comparison between a 6T SRAM cell with MN3/MN1=1.33 and a 9T SRAM cell with MN3/MN1=1.

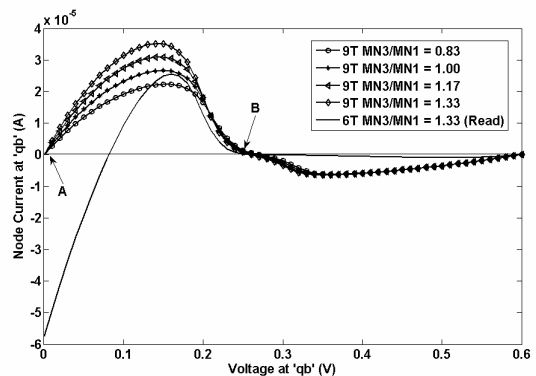


Figure 4. N-curve of the SRAM cell

TABLE I.  
NOISE MARGIN COMPARISON

SRAM cell	Read SNM	SVNM	SINM
6T (MN3/MN1=1.33)	80mV	180mV	25.40uA
9T (MN3/MN1=1.00)	270mV	260mV	26.68uA

Following the proposed SRAM cell design method described above, for a 9T SRAM cell at 32nm feature size, the transistor size ratios among the pull up PMOS, the pull down NMOS, and the access transistor are found for best power, delay and stability performance. In this particular case, the power, delay, and stability performance are optimized when  $MP5/MN1 = 0.83$  and  $MN3/MN1 = 1.00$ .

### III. LEAKAGE CURRENTS OF THE 9T SRAM CELL

#### A. Leakage Currents Component

Gate length scaling increases device leakage exponentially across technology generations. Leakage current is the main source of standby power for a SRAM cell. In nano-scale CMOS devices, the major components of leakage current are the sub-threshold leakage, the gate direct tunneling leakage, and the reverse biased band-to-band-tunneling junction leakage. The sub-threshold leakage, which is defined as a weak inversion conduction current of the CMOS transistor when  $V_{gs} < V_{th}$ , represents a significant leakage current component in the off-state.

The equation for the sub-threshold leakage current is given by (1)

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_{th}}{\eta kT/q}} (1 - e^{\frac{-V_{ds}}{kT/q}}). \quad (1)$$

where 
$$I_0 = \mu_0 C_{ox} (W/L) \left(\frac{kT}{q}\right)^2 (1 - e^{-1.8}). \quad (2)$$

$W$  and  $L$  are the transistor's channel width and length,  $\mu_0$  is the low field mobility,  $C_{ox}$  is the gate oxide capacitance,  $k$  is Boltzmann's constant, and  $q$  is the electronic charge.

#### B. Leakage Current Paths in the 9T SRAM cell

Equation (1) shows that the sub-threshold current increases exponentially due to the voltage difference between drain and source of the MOSFET. Fig. 5 shows three main leakage current paths in the 9T SRAM cell

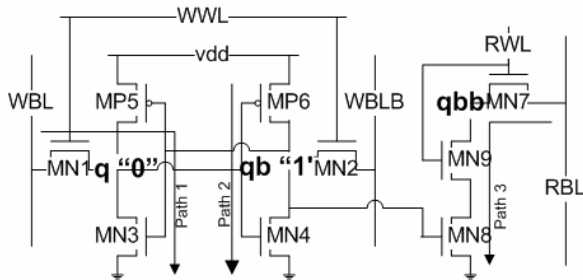


Figure 5. Main leakage current paths of the 9T SRAM cell

when the SRAM cell stores "0" (this is the worst-case leakage current scenario for the 9T SRAM cell). The sub-threshold current of path 3 is significantly reduced by adding MN9 between MN8 and MN7 (generally known as the stack effect). Equation (2) shows that the sub-threshold leakage current is proportional to transistor size. Therefore, the leakage current of path 2 is reduced by scaling down the size of the pull down NMOS NM4. The leakage current of path 1 can be also reduced by lowering the voltage at WBL; this will be discussed in the next section in detail.

### IV. WRITE BITLINE BALANCING CIRCUITRY FOR STANDBY POWER REDUCTION

In a conventional 6T SRAM cell based design, both bitlines must be restored to  $V_{dd}$  following a write operation to ensure a successful read operation. The write amplifier circuitry of [3] ensures that the selected bitline is back to a "high" value by generating a negative pulse to precharge the selected bitline high after driving the bitline low to write "0" into a SRAM cell. Therefore, both bitlines (WBL and WBLB in Fig. 5) will be restored to "high" state after write operation. When the SRAM cell in Fig. 5 stores "0", the voltage difference between drain and source of MN1 is  $V_{dd}$ , causing a large sub-threshold current from WBL to ground when the SRAM cell is in standby mode.

An innovative write bitline balancing circuitry is shown in Fig. 6. When the  $WR\_EN$  signal is enabled, the NMOS transistor NM1 is turned off, and a negative pulse is generated by XDL or XDR to precharge the bitline that is going to be in the "high" state for a fast write. The  $WR\_EN$  signal always arrives faster than the WWL and SEL signals, so there is sufficient time to precharge the high rising bitline to a proper "high" state prior to accessing the SRAM cell. After the write operation, the  $WR\_EN$  signal is removed from the column and MN1 is turned on to balance the voltage at both bitlines to half  $V_{dd}$ . As shown in (1), the sub-threshold current in path 1 decreases exponentially due to the reduced  $V_{ds}$  of the access transistor MN1. The voltage drop at WBLB may increase the sub-threshold current through MN2. However,

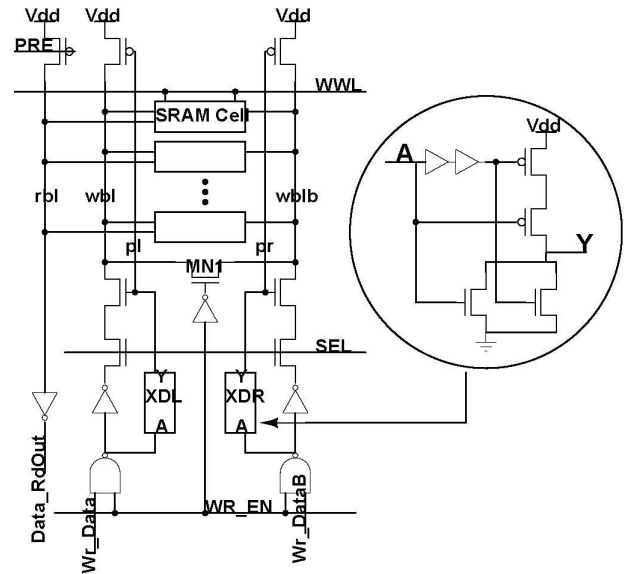


Figure 6. Proposed write bit line balancing circuitry

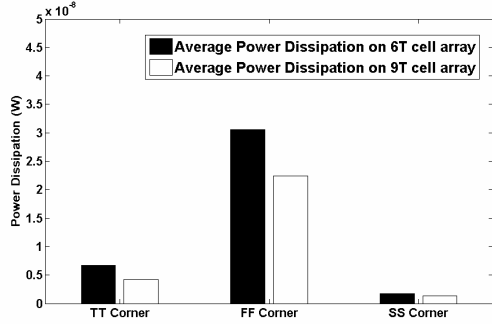


Figure 7. Average power dissipation of the SRAM cell arrays

simulation results show that the total sub-threshold leakage current is reduced more than the sub-threshold current increase through MN2 by balancing the voltage at WBL and WBLB to half V<sub>dd</sub> when the SRAM array holds data.

A 1x128 SRAM cell array at a power supply voltage of 0.6V is used to compare the power dissipation on one column of a memory chip. Both the conventional 6T SRAM cell based array and the proposed 9T SRAM cell based array have been simulated and the Fig. 7 shows the simulation results. The proposed 9T SRAM based array achieves a significant power reduction at three different process corners, i.e. power savings of 32%, 27%, and 25% at typical, fast, and slow corners, respectively.

#### V. IMPACT OF PROCESS VARIATIONS

As CMOS technology scales, process variations are becoming a serious concern as a result of uncertainty in the device and interconnect characteristics such as gate length, thickness of gate oxide, and doping concentrations. Process variations will negatively impact speed, stability, and power consumption of the traditional SRAM designs. The proposed 9T cell achieves a high read SNM by employing separate read and write operations. Table 2 shows the Monte Carlo analysis on the impact of channel length variations on the stability of the 9T SRAM cell. Simulation results show that the 9T cell achieves better stability in the presence of process variations.

Monte Carlo analysis has also been done to a 1x128 SRAM cell array to examine the impact of geometric variation on the power consumption of the individual SRAM cell. Fig. 8 shows the distribution of power consumption for transistor geometry variations. All power consumption results are normalized to the mean of the typical power consumption of the proposed 9T SRAM cell when WBL and WBLB are equal to half V<sub>dd</sub>. Fig. 8 shows that the power consumption of a 9T SRAM cell is lower than the 6T SRAM cell even when process variations are taken into consideration. As shown in fig. 8,

TABLE II. IMPACT OF PROCESS VARIATIONS ON THE STABILITY OF THE 9T SRAM CELL

SRAM cell	Read SNM	SVNM	SINM
9T Best Case	290mV	279mV	30.47uA
9T Worst Case	240mV	238mV	23.61uA
6T (MN3/MN1=1.33)	80mV	180mV	25.40uA

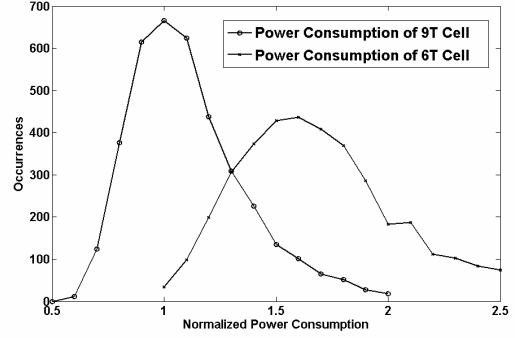


Figure 8. Power consumption distribution of the 6T and 9T SRAM

the power consumption variance of the 9T SRAM cell is much lower compared to the distribution of the 6T SRAM cell. The scheme to lower the bitline voltage during standby mode mitigates the impact of process variations on power consumption.

#### VI. CONCLUSION

This paper presents a new design method for the optimal sizing of a 9T SRAM cell by examining the power-delay product and the N-curve. Different techniques have been proposed to reduce the standby leakage current of the SRAM cell. Along with the transistor sizing method, an innovative bitline balancing scheme has been proposed to reduce the leakage current. Simulation results show that this write circuitry scheme for the proposed 9T SRAM cell based array achieves a 32% reduction in power consumption at a 0.6V power supply voltage and typical process corner compared with a conventional 6T SRAM cell based array. Finally, the impact of process variations on stability and power consumption has been analyzed using a Monte Carlo analysis. The simulation results show that much better tolerance to process variation is achieved using the proposed 9T SRAM cell.

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