Offset Voltage Analysis of Dynamic Latched Comparator

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Abstract— **In this paper, the proposed dynamic latched comparator, which has a separated dynamic differential input gain stage and output stage combined with a latch, is analyzed. A method to estimate the input-referred offset voltage and to maximize the gain of the dynamic pre-amplifier is presented. The difference between the HSPICE and the estimated input-referred offset voltage using the proposed approach turns out to be within 12% range.**

I. INTRODUCTION

Dynamic latched comparators are used for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs), and data receivers due to their fast speed, low power consumption, high input impedance, and full-swing output. However, an offset voltage, resulting from the transistor mismatches such as threshold voltage V_{th}, μC_{ox} and the internal parasitic node capacitances and output load capacitances variations, deteriorates the accuracy of such comparators [1], [2]. Because of this reason, the input-referred offset voltage is one of the most important design parameters of the latched comparator. If large devices are used for the latching stage, a low offset can be achieved at the cost of the increased delay due to slowing the regeneration time and the increased power dissipation. To meet the specifications such as offset voltage and power dissipation in a limited area, it is necessary to fully understand the correlations between sizes of transistors. Conventionally, the latch offset voltage can be reduced by the gain of a static pre-amplifier preceding the regenerative output latch stage. However, the pre-amplifier based comparators suffer not only from large power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance r_{ds} due to the continuous technology scaling [3].

The double-tail sense amplifier presented in [4], which consists of a separated dynamic differential input gain stage and output latch stage, consumes no static power. However, this comparator requires both *Clk* and *Clkb* for its operation and high accuracy timing between them. The dynamic comparator from [5] replaced *Clkb* with two of the internal node voltages and reduced the input-referred offset voltage by increasing the gain of the output latch stage. However,

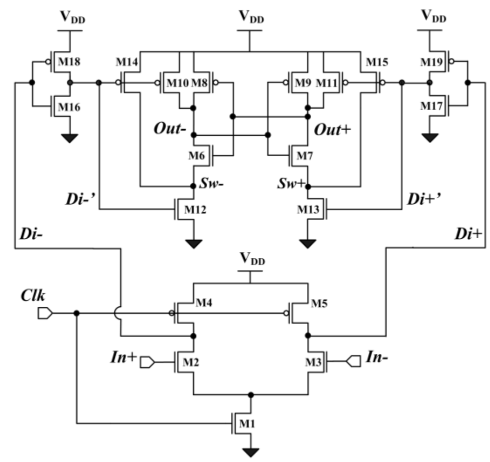

Figure 1 Schematic of the proposed comparator [6]

the output load drivability is weakened and hence delay is increased. The proposed comparator in Figure 1 can take advantages of the both circuits above with two additional inverters inserted between the input- and output-stage. Even with the additional inverter delay, since the complementary version of output-latch stage has bigger drive current capability at the same area, the proposed circuit is faster especially for larger load capacitance. The gain preceding the regenerative latch stage is improved. In this paper, the offset voltage of the proposed dynamic latched comparator, which has a separated dynamic differential input gain stage and output stage combined with a latch, is analyzed.

The remaining sections of the paper are organized as follows. Section II provides a brief operational principle of the proposed comparator. Section III (a) describes the method to obtain the maximum gain and the analytic expression of the offset voltage for the dynamic differential gain stage. In section III (b), the offset voltage of the output stage combined with a latch is derived first, then the input-referred offset voltage of the whole circuit is presented, and conclusion is drawn in Section IV.

II. OPERATIONAL PRINCIPLE OF THE PROPOSED COMPARATOR

The comparator shown in Figure 1 is used for our offset voltage analysis. For its operation, during the pre-charge (or reset) phase (Clk=0V), both PMOS transistors M4 and M5 are turned on and they charge Di nodes capacitance to V_{DD}, which, in turn, make both NMOS transistor M16 and M17 of the inverters on and Di' nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M16 are turned on and "*Out*" nodes and "*Sw*" nodes are charged to V_{DD} while both NMOS transistors M12 and M13 are off.

During evaluation (decision-making) phase (Clk=V_{DD}), each Di node capacitance is discharged from V_{DD} to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between Di+ and Di- nodes. Once either Di+ *or* Di- node voltage drops down below around V_{DD}-$|V_{tp}|$, the additional inverter pairs M18/M16 and M19/M17 invert each Di node signal into the regenerated (amplified) Di' node signal. Then the regenerated and different phased Di' node voltages are relayed to the output-latch stage by M10- M13. As the regenerated each Di' node voltage is rising from 0V to V_{DD} with a different time interval (or a phase difference which increases with the increasing input voltage difference ΔV_{in}), M12 and M13 turn on one after another and the output latch starts to regenerate the small voltage difference transmitted from Di' nodes into a full-scale digital level: *Out*+ node will output logic high (V_{DD}) if the voltage difference at Di' nodes $\Delta Di'(t)$ is negative ($Di+'(t) < Di-'(t)$) and *Out*+ will be low (0V) otherwise. Once either of the *Out* node voltages drops below around V_{DD}-$|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

In the following section, the proposed circuit is divided into sub-circuits: dynamic differential input gain stage and output latch stage, and both stages are analyzed.

III. OFFSET VOLTAGE IN THE PROPOSED COMPARATOR

A. *Dynacmic Differential Input Gain Stage*

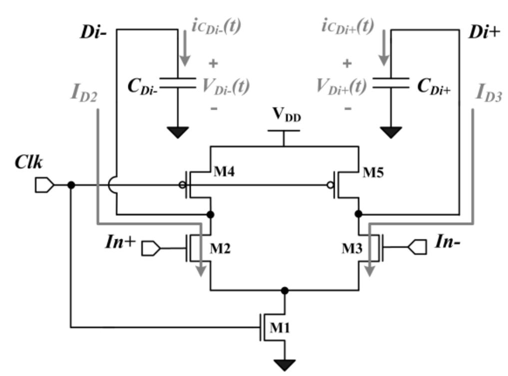

Figure 2 Simplified schematic of dynamic differential input stage when *Clk* is changing from 0V to V_{DD}

The simplified first stage of the proposed comparator is show in Figure 2. During the evaluation phase (Clk=V_{DD}), the input differential pair discharges each Di node voltage down to 0V with a different time rate proportional to the input voltage. For $V_{DS2,3} \geq V_{GS2,3}-V_{tn}$ ($V_{Di} \geq V_{com}-V_{tn}$), assuming that the time (t) is $t_1 \leq t \leq t_2$ in this section, since the transistor M2 and M3 operate in saturation region, the drain currents I_{D2} and I_{D3} can be expressed as (for simplicity, assuming $\lambda = \gamma = 0$ and $V_{D1}(t)$ is constant over $[t_1, t_2]$);

$$C_{Di-}\frac{dV_{Di-}(t)}{dt} = i_{C_{Di-}}(t) = -I_{D2} \quad (1)$$

$$C_{Di+}\frac{dV_{Di+}(t)}{dt} = i_{C_{Di+}}(t) = -I_{D3} \quad (2)$$

By integrating both sides of (1) and (2) over $[t_1, t]$ and applying the initial condition: $V_{Di}(t_1)=V_{DD}$, the following equations are obtained;

$$V_{Di-}(t) = V_{DD} - \frac{I_{D2}}{C_{Di-}}t \qquad V_{Di+}(t) = V_{DD} - \frac{I_{D3}}{C_{Di+}}t \quad (3)$$

$$\Delta V_{Di}(t) = V_{Di-}(t) - V_{Di+}(t) \quad (4)$$

Then, with the assumption that ΔV_{in} (= V_{in+}-V_{in-}) is constant over the integration time $[t_1, t]$, the dynamic gain of the first stage can be defined as

$$A_{V1}(t) = \frac{\Delta V_{Di}(t)}{\Delta V_{in}} \quad (5)$$

If we apply the small signal approximation: $2(V_{GS2,3} - V_{tn}) >> \Delta V_{in}$ and assume $C_{Di-} = C_{Di+} = C_{Di}$, Equation (5) can be expressed as

$$A_{V1}(t) = -\frac{g_{m2}}{C_{Di}}t \quad (6)$$

Equation (6) implies that as long as transistor M2 and M6 operate in saturation region and ΔV_{in} does not change over $[t_1, t_2]$, the dynamic gain $A_{V1}(t)$ keeps increasing with increasing t. Since t is proportional to $C_{Di}/I_{D2,3}$, in order to maximize the gain, $|g_{m2}/I_{D2,3}|$ should be maximized during integration time. Except for the sub-threshold operation, g_m/I_D is larger in saturation operation than linear operation. Therefore, as the size (W_1) of transistor M1 is reduced, the input transistor remains in saturation region longer. This, in turn, increases the gain of the first stage at the cost of increasing delay. In addition, by increasing the channel length of input transistor, for example 90nm to 120nm in 90nm technology, one can get higher gain with the same $W_{2,3}/L$ ratio by reducing short-channel effects such as a dynamic conductance variation due to DIBL. If a negative supply voltage is available, by replacing the ground of the input differential pair with a negative supply voltage and further reducing the size of transistor M1, one can get wider common mode input range. Therefore, this differential input stage can be designed in a different way depending on the requirements such as the speed, offset voltage and common mode input voltage range.

To calculate the offset voltage ($V_{OS,\ pre}$) of the input differential pair, both input transistors and node capacitances are assumed to have mismatch. Then, device parameters and node capacitances can be express as;

$$\begin{aligned} &(\mu_n C_{ox})_2 = \mu_n C_{ox} && (\mu_n C_{ox})_3 = \mu_n C_{ox} + \Delta\mu_n C_{ox} \\ &V_{tn2} = V_{tn} && V_{tn3} = V_{tn} + \Delta V_{tn} \\ &C_{Di-} = C && C_{Di+} = C + \Delta C \end{aligned} \quad (7)$$

Now we need to find the value of $V_{OS}=V_{GS2}-V_{GS3}$ which make $\Delta V_{Di}=0$. From (3) and (4), we can derive $I_{D2}C_{Di+}=I_{D3}C_{Di-}$. Thus, if the Di node capacitances are mismatched $C_{Di+}\neq C_{Di-}$, $I_{D2}\neq I_{D3}$. Then, assuming $I_{D2}=I_D$ and $I_{D3}=I_D+\Delta I_D$, $\Delta I_D/I_D=\Delta C/C$ is obtained. Therefore, he offset voltage is derived by following way [7].

$$V_{OS,pre} = V_{OS2,3} = V_{GS2} - V_{GS3} \tag{8}$$

$$= \frac{V_{GS2,3} - V_{tn}}{2}\left[-\frac{\Delta I_D}{I_D} + \frac{\Delta(\mu_n C_{ox})}{\mu_n C_{ox}}\right] - \Delta V_{tn} \tag{9}$$

$$= \frac{V_{GS2,3} - V_{tn}}{2}\left[-\frac{\Delta C}{C} + \frac{\Delta(\mu_n C_{ox})}{\mu_n C_{ox}}\right] - \Delta V_{tn} \tag{10}$$

Equation (10) shows that V_{OS} is affected by device mismatches and bias conditions. V_{OS} increases directly proportional to the threshold voltage mismatch and also increases with the increase of V_{com} and *Di* node capacitance and transistor mismatch.

$$V_{OS2,3}{}^2 = \left(\frac{V_{GS}-V_{tn}}{2}\right)^2\left\{\left(\frac{\Delta C_D}{C_D}\right)^2 + \left[\frac{\Delta(\mu_n C_{ox})}{\mu_n C_{ox}}\right]^2\right\} + \Delta V_{tn}{}^2 \tag{11}$$

B. Output Stage Combined with Latch

The inputs of the output latch stage are the gates of transistor M10-13 which are connected to Di-' and Di+' nodes. During the evaluation phase ($Clk=V_{DD}$), if $V_{in+}\neq V_{in-}$, each Di' node voltage rises from 0V to V_{DD} with a different time interval, therefore, the output stage can make a decision whether logic high or low. However, if $V_{in+}=V_{in-}$ and no mismatch exists, both Di' node voltages rise up exactly the same time rate. This makes both branches of the output stage maintain in a balanced state, which means $V_{out+}(t)=V_{out-}(t)$ during all the transient time.

However, if a mismatch exits in the output stage, the circuit will be unbalanced making $V_{out+}(t)\neq V_{out-}(t)$. In order for the circuit to be balanced, a voltage $V_{OS,\,latch}$ should be applied between the output of the inverter (M18/M16) and *Di-'* node to compensate the mismatch when *Di'* nodes rises. In order to calculate the offset voltage $V_{OS,\,latch}$ of the output stage, the mismatch in μC_{ox} and threshold voltage V_{th} are assumed to be the dominant factors to cause the offset voltage and W/L mismatch will be considered as a parasitic node capacitance mismatch in this analysis.

The operation regions of the transistors of the output stage vary with time, however, at the time point when *Di'* node voltage is around V_{tn12}, transistor M12 and M13 just turn on and operate in saturation region. Once $V_{D12,13}$ node drops down below $V_{DD}-V_{tn}$ from V_{DD}, transistor M6 and M7 also start to turn on and operate in saturation region since both their drain and gate voltages are dropping down at the same rate under the balanced condition. Also, the transistor M10 and M11 operate in linear region since both V_{out+} and V_{out-} are still around V_{DD}. Since the reset transistor M14 and M15 are designed to be much smaller than transistor M12

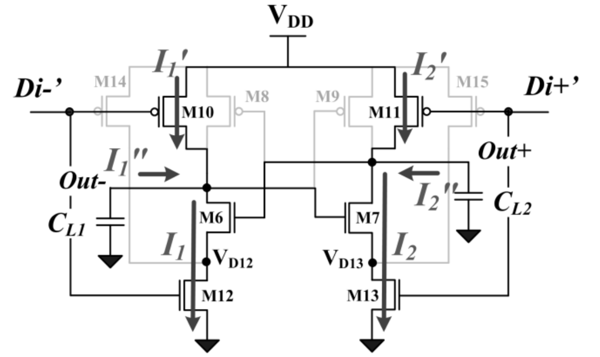

Figure 3 Simplified schematic of the output stage combined with latch when V_{di}' is around V_{tn}

and M13, their effects on node $V_{D12,13}$ are negligible. Also, the effect on *Out*± nodes from transistor M8 and M9 are ignored since they are in cut-off region. Therefore, the output latch stage can be drawn in Figure 3 for the time of our analysis.

First, mismatch between transistor M12 and M13 is considered and other pairs are assumed to be perfectly matched. In our analysis, the load capacitance C_{L1} and C_{L2} include the parasitic capacitances at *Out*± nodes. At this time, C_{L1} and C_{L2} are assumed to be the same as C.

$$I_{D12} = I_1 \qquad I_{D13} = I_2 \triangleq I_1 + \Delta I_1 \tag{12}$$

$$I_1'' = -C_{L1}\frac{dV_{out-}}{dt} \qquad I_2'' = -C_{L2}\frac{dV_{out+}}{dt} \tag{13}$$

Since in the balanced condition, $V_{out-}=V_{out+}$, $dV_{out-}/dt = dV_{out+}/dt$, it is fair to say that

$$I_1'' = I_2'' \triangleq I'' \tag{14}$$

Also, from KCL and KVL, the followings are obtined.

$$I_1' = I_1 - I_1'' \qquad I_2' = I_2 - I_2'' \tag{15}$$

$$I_1'R_{10} = I_2'R_{11} \tag{16}$$

From (12), (14), (15) and (16),

$$\frac{\Delta I_1}{I_1} = \frac{\Delta I_D}{I_D} = \frac{R_{10} - R_{11}}{R_{10}}\left(1 - \frac{I''}{I_1}\right) \tag{17}$$

By applying (19) into (10),

$$V_{OS12,13}^2 = \left[\left(\frac{V_{di}' - V_{tn}}{2}\right)^2\left(\frac{\Delta\mu_n C_{ox}}{\mu_n C_{ox}}\right)^2 + \Delta V_{tn}^2\right] \cdot \left\{1 + \frac{V_{di}' - V_{tn}}{2\left(V_{DD} - V_{di}' - |V_{tp}|\right)}\left[1 - \frac{I''}{I_1}\right]\right\}^{-2} \tag{18}$$

The equation (18) explains that with aid of transistor M10 and M11, which are both reset switch and input transistors for output latch stage, V_{OS} is reduced by the factor of the additional term once either or both transistor M12 and M13 turn on: V_{di}'>V_{tn}. In addition, as V_{di}' increases from V_{tn} to around V_{DD}-|V_{tp}|, V_{OS} is further reduced. Therefore, we can only consider the worst case offset voltage V_{OS} when $V_{di'}$ is around V_{tn}.

For mismatch between transistor M6 and M7, from the fact that $I_{D12}=I_{D6}$ and $I_{D13}=I_{D7}$, we have

$$V_{OS6,7}^2 = \frac{W_6}{W_{12}}\left[\left(\frac{\Delta\mu_n C_{ox}}{\mu_n C_{ox}}\right)^2 \frac{(V_{out\pm} - V_{D13} - V_{tn})^2}{4} + (V_{D13} - V_{D12})^2 + \Delta V_{tn}^2\right] \quad (19)$$

Equation (19) shows the offset voltage caused by the mismatch between the transistor M6 and M7 is the function size of transistor M6(M7) and M12(M13). Therefore, it is possible to find a particular W/L ratio which makes an optimum tradeoff between random offset voltage and transistor size of WxL.

In a similar way, the offset voltage $V_{OS10,11}$ caused by the transistor mismatch between M10 and M11 can be found

$$V_{OS10,11}^2 = \left(\Delta V_{tp}^2 + \left(\frac{\Delta\mu_p C_{ox}}{\mu_p C_{ox}}\right)^2 \left(V_{DD} - V'_{di} - |V_{tp}|\right)^2\right)$$

$$\cdot\left\{1 + \left[1 + \left(\frac{\Delta\mu_p C_{ox}}{\mu_p C_{ox}}\right)\right]\left(V_{DD} - V'_{di} - |V_{tp}|\right)\left(\frac{\mu_n C_{ox}\left(\frac{W_{12}}{L}\right)(V'_{di} - V_{tn})}{I_1 - I''}\right)\right\}^{-2} \quad (20)$$

To calculate the offset voltage caused by load capacitance including parasitic capacitance at *Out*± node, it is necessary to assume that C_{L1}=C and C_{L2}=C+ΔC. Applying them to equation (13),

$$I_1'' = I'' \qquad I_2'' = I'' + \Delta I'' \quad (21)$$

From (9), (15), (16) and (21),

$$V_{OS\,Cload}^2 = \left(\frac{V'_{di} - V_{tn}}{2}\right)^2 \left(\frac{I_1'' - I_2''}{I_1}\right)^2$$

$$*\left\{1 + \frac{V'_{di} - V_{tn}}{2(V_{DD} - V'_{di} - |V_{tp}|)}\left[1 - \frac{I_1''}{I_1}\right]\right\}^{-2} \quad (22)$$

Equation (27) shows that the offset voltage caused by capacitance mismatch at the output nodes increases as V_{di}' increases and can be reduced by increasing the size of transistor M12 and M13. Similarly, the former term is reduced by the same factor of equation (18).

IV. Simulation Results

The proposed comparator is designed using 90nm PTM technology [8] and the offset voltages of the output latch stage caused by mismatches in the transistor pairs (M6/7, M10/11, M12/13) are simulated with HSPICE. For our simulation, all variations are assumed to be normally distributed about nominal values. Also, the V_t standard deviation is assumed as

$$\sigma(V_t) = \frac{3\text{mV}}{\sqrt{WL}} \text{ where W, L are in } \mu\text{m} \quad (23)$$

TABLE I. V_{OS} FROM THE MISMATCH IN THE CRITICAL PAIRS

Mismatched Tr. Pairs	σ_{Vt}	*Calculated Latch* σ_{Vos}	*Simulated Latch* σ_{Vos}	*Calculated Input-referred* σ_{Vos}	*Simulated Input-referred* σ_{Vos}
M12/M13	9.13 mV	7.02 mV	8.78 mV	0.70 mV	0.68 mV
M10/M11	10 mV	0.41 mV	0.79 mV	0.04 mV	0.07 mV
M6/M7	10 mV	8.33 mV	8.71 mV	0.83 mV	0.74 mV
M2/M3	7.07 mV	7.07 mV	7.07 mV	7.07 mV	7.07 mV

To verify the equation (18)-(20), the nominal design values, $V_{out\pm}$~0.998V, V_{D12}~V_{D13}=0.702, V_{tn}=|V_{tp}|=0.2V, at the balanced state when V_{di}'=0.46V, are used. The calculated and simulated offset voltages of the output latch stage and input-referred offset voltages caused from V_t mismatches are listed in Table 1. For simulated results, 100 iterations of Monte Carlo transient simulations are performed for each mismatch for the critical pair with a σ(V_t) standard deviation modeled by equation (23) and at the operation conditions of V_{DD}=1V, f_{CLK}=3GHz, V_{com}=0.7V and C_L=7fF. With the gain (~10V/V) of the dynamic pre-amplifier, the input-referred offset voltages for each mismatch pair are reduced by a factor of 10 where around 2 times of the gain is produced by the inverter pairs (M18/16 and M19/M17) followed by the *Di* node gain of around 5. The simulated results show a good agreement with our calculation and the input referred latch offset voltages can be reduced by the gain of the dynamic pre-amplifier stage when the mismatches of inverter pairs are ignored.

V. Conclusion

The proposed dynamic comparator has been analyzed in terms of the dynamic input differential gain and offset voltages of input and output stage. The offset voltage analysis used in this paper can be a good reference for comparator design optimization for performance and area.

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