# Carbon Nanotube Bundle Interconnect: Performance Evaluation, Optimum Repeater Size and Insertion for Global Wire

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***Abstract*—To remove the bottleneck of the interconnect especially at semi-global and global level, performance evaluation of local, semi global, and global interconnect is presented in this paper based on carbon nanotube (CNT) interconnect bundle model. For the greater length of the wire, a methodology is presented to find the optimum insertion and size of buffer for CNT bundle interconnects. The performance analysis for repeater shows that the CNT bundle can run 2.58 times longer without repeater insertion and requires 31% less buffer size than Cu wire.**

## I. INTRODUCTION

With the arrival of complex Systems-On-Chip(SoC), many modules are integrated into a single chip that forms the on-chip communication network itself [1]. This requires the fast interconnect techniques to improve the bandwidth density and global interconnect latency to resolve the interconnect bottleneck [2]. As interconnect feature size decreases, resistance of the copper wire increases and hence it causes significant performance and reliability issues in modern VLSI [3] [4]. Table I shows resistivity for the copper wire for different technology nodes [3] [20].

Carbon nanotube has been proposed to alleviate this problem due to its excellent current carrying capability, thermal stability, and thermal conductance [5]. However, there are still several challenges remaining to use the carbon nanotube as interconnect, and the challenges are its imperfect contact resistance, its high resistance (more than 6.45KΩ), and controllability of chirality. High resistance problem can be reduced by using CNT bundle. However, not all the CNTs in the bundle are metallic due to lack of control over chirality and it reduces the density of the metallic CNT per area and hence increases resistance. This paper addresses the performance evaluation of the nanotube bundle and designing of repeater in case of global interconnect.

TABLE I. COPPER RESISTIVITY WITH DIFFERENT TECHNOLOGY NODE

| | Copper $\rho$ (μΩ-cm) | | |
|---|---|---|---|
| | *45nm* | *32nm* | *22nm* |
| Local | 3.26 | 3.93 | 4.67 |
| Intermediate | 3.09 | 3.49 | 4.23 |
| Global | 2.57 | 2.96 | 3.38 |

This paper is organized as follow. Section II will present the physical circuit model of the carbon nanotube bundle and Section III will give the performance evaluation and comparisons with conventional copper wire interconnect for different lengths. Section IV will give the optimal repeater design method followed by the conclusion of this paper in Section V.

## II. PHYSICAL CIRCUIT MODEL FOR CNT BUNDLE

### A. Resistance

Resistance model discussed here depends on the number of metallic carbon nanotubes present in bundle and the length of the wire linearly. There are some analysis presented in [6] about the non linear dependency over length due to the electron-defect scattering. This paper will follow linear resistance model.

There are three contributions towards the resistance of the CNT bundle; Contact resistance, Fundamental resistance, and Ohmic or scattering resistance. Contact resistance is mainly due to imperfect contact between metal and CNT interconnect and it can be as high as 120KΩ [7]. But laboratory experiments have shown much smaller than the total resistance [8] [9]. Fundamental resistance (which is given by $h/4e^2$, where h is plank's constant and e is electron charge) is present in CNT for all length due to spin degeneracy and sub-lattice degeneracy of electrons in grapheme [10]. Additional, scattering resistance is present for

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the length greater than the mean free path (>1μm) of CNT [11] as electron movement will no longer be ballistic and it scatters (which is given by $R_f*l/l_o$, where $Rf$ is fundamental resistance, $l$ is interconnect length and $l_o$ is electron mean free path of CNT). The total resistance of the CNT bundle is given by:

$$R_{bundle} = (R_c + R_f + R_{sc}*l)/N \quad 1)$$

Where, $R_c$, $R_f$, and $R_{sc}$ are metal contact, fundamental, and ohmic resistances respectively. N is number of metallic CNTs and $l$ is length of interconnect, respectively.

### B. Inductance

There are two components that contribute to inductance of the CNT; Kinetic inductance, Mutual inductance. Kinetic inductance is present where there is no voltage drop across the given interconnect length and that only happens for the length less than the mean free path of the CNT [12]. The inductance of the CNT bundle is given by:

$$L_m = \frac{\ }{2\pi} * \ln(\, y / d \,) \quad 2)$$

$$L_k = h/2e^2 v_f \quad 3)$$

$$L_{bundle} = L_{cnt}/N \quad 4)$$

Where, Lm and $L_k$ are mutual and kinetic inductances, respectively. $y$, $v_f$ and $d$ are distance above ground plane, diameter of CNT and fermi velocity respectively. For length less than mean free path, includes both Lm and Lk in $L_{cnt}$, else includes only mutual inductance given by Equation 2.

### C. Capacitance

Capacitance is the trickiest part to formulate for the carbon nanotube bundle. Capacitance arises from two sources; quantum capacitance and electrostatic capacitance. The quantum capacitance accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Quantum capacitance is used to model the energy needed to add an electron at an available quantum state above the Fermi level and it is turning out around 400aF/μm*N [13] for CNT bundle where N is number of metallic CNTs in bundle. Basic equation for the capacitances of single CNT can be formulated as per Equations 5 and 6, where $C_e$ and $C_q$ are electrostatic and quantum capacitances:

$$C_e = 2\pi\varepsilon / \ln(y / d) \quad 5)$$

$$C_q = 2e^2/h*v_f \quad 6)$$

Electrostatic capacitance for the bundle can be extracted from 3D field solver tools such as FastModel [14], RAPHEL [15], MAXWELL [16] and CNIA [17] online tool or from [18] the equation 7:

$$C_b = 2Cen + (nw-2)*Cef/2 + 0.6*(nh-2)*Cen \quad 7)$$

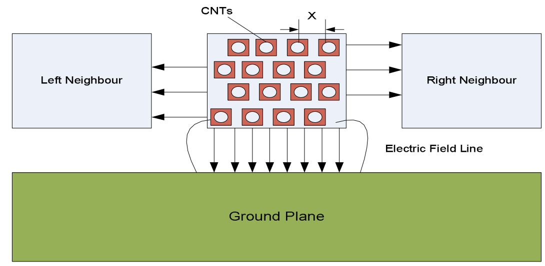


Figure 1. Electric field lines for the CNT bundle, CNTs are approximated to square; the same can be applied for any 3D field solver tools to estimate capacitance for the bundle. X is the probability factor for metallic tubes in CNT bundle and that can be viewed as spacing factor between tubes. For example, X with value 1 will give the bundle with 100% metallic tubes.

TABLE II. ELECTROSTATIC CAPACITANCE ESTIMATION WITH SPACING OF 1.73NM BETWEEN CNTS [18] (DIFFERENT SPACING GIVES DIFFERENT VALUES FOR EQUATION 7)

| | Total Bundle Capacitance $C_b$ | | | | |
|---|---|---|---|---|---|
| | 50 μm | 100 μm | 300 μm | 500 μm | 700 μm |
| CNIA Tool | 2.12fF | 4.41fF | 13.2fF | 22.1fF | 30fF |
| As per equation 7 | 96.34 fF | 192.6 fF | 971.8 fF | 1.61 pF | 2.26 pF |

Where, $C_b$, $C_{en}$ and $Cef$ are total bundle electrostatic, near end electrostatic and far end electrostatic capacitances, respectively. nw and nh are number of CNTs across width and height respectively.

Electric field lines associated with electrostatic capacitance for given wire geometry can be viewed as shown in Figure 1, where CNTs in bundle is approximated to square for illustration. As all the CNTs in bundle are at the same potential, we can neglect the coupling capacitance between them and at the same time consider only metallic CNTs across edges of height and width to calculate the capacitance between neighbors and ground plane.

Equation 7 tends to overestimate the capacitance for given technology node of the CNT bundle in absence of proper values of $n_w$ and $n_h$. Therefore, it is better to use field solver tools for given wire geometry with assumption that all the CNTs are at the same potential. The estimation and comparison of values for 45nm node and different lengths are shown in Table II.

Total capacitance per length of the bundle can be calculated by the following Equation 8) which has series combination of quantum ($4*C_q$) and electrostatic capacitance ($C_b$) [18]:

$$Cbundle = \frac{4*(Cb*Cq)}{(Cb+4Cq)} \quad 8)$$

## III. PERFORMANCE EVALUATION AND COMPARISON

This paper will refer the wire model shown in Figure 2 for the semi-global and global interconnect simulations while model remains same for local wire except exclusion of ohmic resistance ($R_{sc}$). Comparison is made for 45nm technology node.

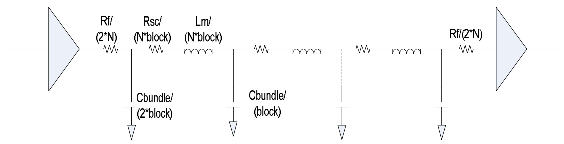


Figure 2. Wire model for global and semi-global interconnects [21].

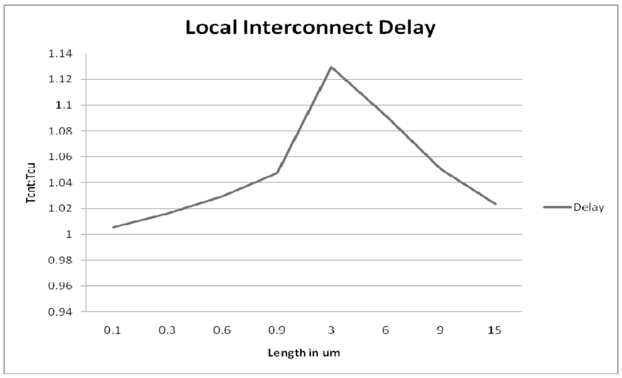


Figure 3. Local interconnects performance evaluation with 1.73nm spacing between CNT tubes.

### A. Local Interconnect

For local interconnect, Cu wire interconnect performs better than CNT bundle [20]. However, monolayer CNT structure can perform better than Cu interconnects [22] by having thick dielectric layer. In that case, capacitance is found to be lower than that of the Cu wire interconnect. However, at the same time, the resistance becomes comparable to the driver resistance. Therefore, one should take care of designing driver for the monolayer CNT structure. Increase in performance can be achieved by adjusting the number of metallic tubes in CNTs in the bundle as shown in Figure 3, where Tcnt:Tcu is the delay ration between CNT bundle and Cu interconnect.

### B. Semi-global and global Interconnect

At semi-global and global level, CNT bundle interconnect completely outperforms the Cu wire interconnect. For long interconnect, buffers should be inserted to reduce latency. In the next Section, repeater insertion method will be explained in detail. The following Figures 4 and 5 show the comparisons between Cu and CNT bundle, where Tcnt:Tcu is the delay ration between CNT bundle and Cu interconnect.

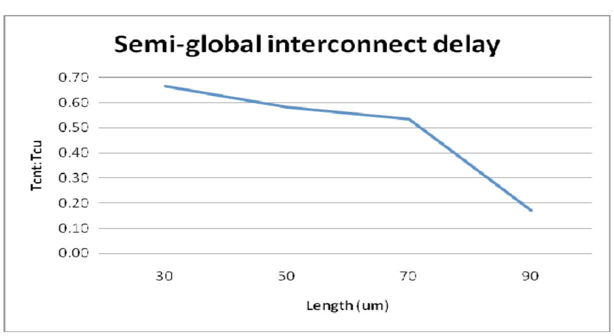


Figure 4. Semi-global interconnect delay comparison

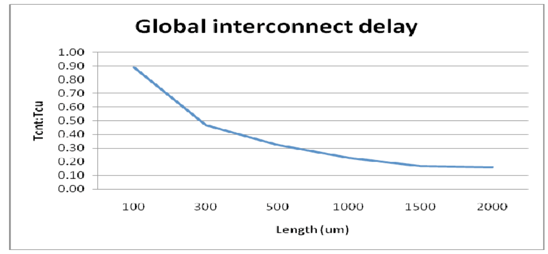


Figure 5. Global interconnect delay comparison

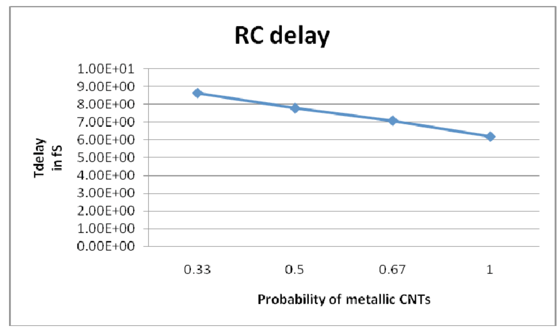


Figure 6. Performance evaluation of CNT bundle with different probability of metallic tubes

Performance improvement in case of intermediate and global interconnect is due to the low resistance comparing to the Cu wire while capacitance still remains comparable.

However, these performances depend on the number of metallic tubes present in the bundle and level of interconnect i.e. local, intermediate and global, since resistance decreases with the increase in number of tubes while capacitance increases at the same time. Effect of the number of CNTs in the bundle on the interconnect delay is shown in the Figure 6 for length of 200um.

## IV. REPEATER FOR CNT BUNDLE

When the resistance of the interconnection is comparable to or larger than the on-resistance of the driver, propagation delay increases as the square of the interconnection length because both capacitance and resistance increase linearly with length. The use of repeaters makes time delay linear with length by dividing the interconnection into smaller subsections.

CNT bundle model used so far has inductance included, while we can still ignore the inductance with maximum of 10% error in delay estimation [19]. RC delay model only becomes inaccurate when following inequality matches:

$$Z_{dr}*C < 0.5*RC < Z_o C \quad 9)$$

Where, $Z_{dr}$ and $Z_o$ is driver and interconnect characteristic impedances respectively, R and C are interconnect total resistance and capacitance. In [21], it is shown that RC model for CNT bundle is good enough for the delay estimation as Equation 9 inequality never matches for the CNT bundle. In

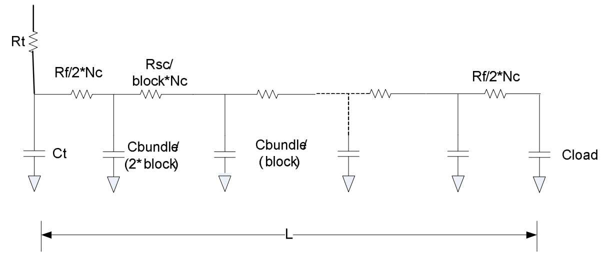


Figure 7. Reference figure to derive the delay equation. Here block indicates the repeater insertions, and L is total wire length. Rsc is the ohmic resistance referenced as Rw in below equations, Cbundle is total capacitance referenced as Cw in below equations and Nc is number of CNTs in bundle.

TABLE III. COMAPARISON FOR DIFFERENT REPEATER PARAMETERS (GEOMETRY USED AS GIVEN IN FIGURE 1)

| | Repeater Comparison | |
|---|---|---|
| | *CNT Bundle* | Cu |
| Buffer Size in µm | 22 | 32.08 |
| Optimal Length in µm | 580.80 | 225 |

this section equations for buffer size and number of repeater stages are derived.

To estimates the optimum repeater stages for given length, total delay equation is derived from Figure 7 and the delay is given by Equation 10. Taking partial derivative of the equation with respect to the number of segments and buffer size and equating them with zero, the optimum number of repeaters and the buffer size can be found by Equations 11 and 12, respectively.

$$T_{delay}=2MCtRt+L(CtRwN+\frac{CwRt}{N}+R_fCw)+L^2(\frac{CwRw}{2M})+MR_fCtN \quad 10)$$

$$N=\sqrt{\frac{CwRtL}{(6.45e3/Ncnt)MCt+LRwCt}} \quad 11)$$

$$M=L\sqrt{\frac{CwRw}{2CtRt+(6.45e3/Ncnt)NCt}} \quad 12)$$

Where, $T_{delay}$ is total delay. M and N are number of repeaters and size of buffer in micron, respectively. Ct and Rt are driver capacitance per gate width and gate width times driver resistance, respectively. $R_f$ is fundamental resistance of CNT independent from the length which can be replaced by $6.45e3/N_{cnt}$ as shown in Equations 11 and 12. $N_{cnt}$ is number of metallic CNTs in bundle.

To calculate M, put any arbitrary value of N and rest of the values in the Equation. As M and N are independent, selecting any arbitrary value for the N will not affect the outcome of M significantly. The same can be applicable for the calculation of N if N is to be calculated first. Optimal length can be calculated by dividing total length by M. Table III shows the comparison with Cu wire for the repeater insertion and buffer size for 45nm technology node.

## V. CONCLUSION

This paper demonstrated CNT bundle as a good replacement for the semi global and global interconnects by presenting various simulation results including buffer insertion algorithm. At the local interconnect level; better performance can be obtained by reducing the bundle capacitance. As shown in Section IV, CNT bundle is 2.58 times better in optimal length and requires 31% less buffer size than Cu wire, which means it can run longer without repeater and with smaller buffer than the Cu wire.

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