

# A Novel Design Methodology to Optimize The Speed and Power of the CNTFET Circuits

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**Abstract**— Carbon nanotubes with their superior properties have proved to be a potential alternative device to CMOS. In this paper, circuit optimization methods for high performance and low power CNFEET circuit are proposed. The proposed design methods for CNTFET circuit address how to decide the optimum CNTFET parameters such as pitch, diameter, number of CNTs (Carbon Nano Tube), optimum fan-out factor and logical efforts to deliver the minimum power-delay product. The proposed method makes it possible to accomplish 56% dynamic power reduction and 22% less delay by optimizing the pitch, number of CNTs, fan-out factor, and logical efforts compared to the circuits that are not optimized and screening effects are ignored.

## I. INTRODUCTION

The Carbon Nanotube Field Effect Transistor (CNTFET), one of the promising new devices, avoids most of the fundamental limitations of the traditional silicon MOSFETs. With ultra long ( $\sim 1\mu\text{m}$ ) mean-free-path (MFP) for elastic scattering, ballistic or near ballistic transport can be obtained with intrinsic CNT under low voltage bias to achieve the ultimate device performance [1][2][3]. A typical structure of MOSFET-like CNTFET device is illustrated in Figure 1. The channel region of the CNT is undoped while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices. Carbon nanotubes are high-aspect-ratio cylinders of carbon atoms. The electrical properties of a single wall carbon nanotube (SWNT) offer a potential for molecular-scale electronics. A typical semiconducting single-wall carbon nanotube is 1.4nm in diameter with 0.6eV bandgap and bandgap is inversely proportional to the diameter). Recent carbon nanotube field effect transistors (CNFETs) have a metal carbide source/drain contact [6] and a top gated structure (Fig. 1) with thin gate dielectrics [7]. The contact resistance and the subthreshold slope of the CNTFET are comparable to those of silicon MOSFET. While silicon FET's current drive is typically measured in current per unitary device width (e.g.  $\mu\text{A}/\mu\text{m}$ ), the current of CNTFET is

measured in current per tube reflecting the structure of the CNTFET as an array of the carbon nanotubes that have the constant spacing and fixed diameter.

Efforts have been made in recent years on modeling and simulating CNT related devices such as CNTFET [2] and CNT interconnects [3] to evaluate the potential performance at the device level. However, the dynamic performance of a complete circuit system, consisting of more than one CNTFETs and interconnects, differs from that of a single device. In this paper, from physical design perspective for the application of CNTFET, a practical and effective circuit design method for CNTFET is proposed and its legitimacy is proved by extensive simulations. Circuit characteristics are compared with the case that the screening effect is ignored.

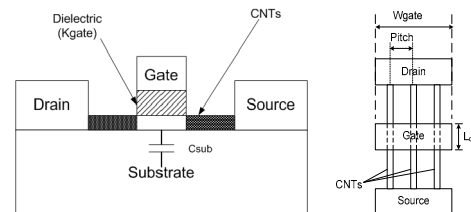


Figure 1. CNTFET Structure.

## II. ANALYSIS OF CNTFET DEVICE PARAMETERS

### A. Channel capacitance and current vs pitch

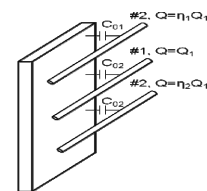


Figure 2. Three CNTs in array and electrode

The charges on the CNTs #2 and #3 will affect the electric field and electrostatic potential profile between the

electrode #0 and the CNT #1, and the coupling capacitance  $C_{01}$  in Figure 2 is given by;

$$C_{01} = \frac{Q_1}{V_1} = \frac{Q_1}{V_0 + V_{adj}} \quad (1)$$

$V_{adj}$  increase as the pitch decreases, and the capacitance  $C_{01}$  located in the middle of CNTs decrease. Figure 3 shows the channel capacitance of the CNTFET and the parameters that determine the gate capacitance. The  $C_{gc\_e}$  is the capacitance of the CNT located in the edge of the CNTFET device and the  $C_{gc\_m}$  is the capacitance of the CNT located in the middle of the CNTFET device.

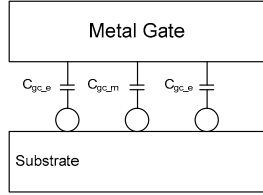


Figure 3. Three CNTs in parallel to the gate

Figure 4 shows the capacitances  $C_{gc\_e}$  and  $C_{gc\_m}$  for different pitches. As mentioned previously, the pitch of a CNT is also a parameter that determines the CNTFET current.

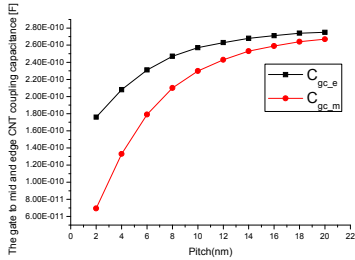


Figure 4, The gate to middle and edge CNT channel capacitances

If there are more than  $N$  ( $N > 2$ ) tubes in the CNTFET, then the total channel capacitance is given by  $(N-2)C_{gc\_m} + 2C_{gc\_e}$ , and it can be expressed in terms of  $C_{gc\_e}$  as  $(\eta(N-2)+2)C_{gc\_e}$ , and the total channel capacitance  $C_{gch}$  is, therefore, given by;

$$\begin{aligned} C_{gch} &= C_{gc\_l} && \text{if } N=1 \\ &= 2C_{gc\_e} && \text{if } N=2 \\ &= (\eta(N-2)+2)C_{gc\_e} && \text{if } 2 < N \end{aligned} \quad (2)$$

where  $N$  is the number of tubes,  $C_{gc\_l}$  is the channel capacitance of the CNTFET with only one tube, and  $\eta$  is the ratio between  $C_{gc\_e}$  and  $C_{gc\_m}$ , i.e.  $\eta = (C_{gc\_e}/C_{gc\_m})$ .  $\eta$  is determined based on the pitch, supply voltage, channel length, and the diameter of the CNT, and  $\eta$  is shown in Table 1 (found based on HSPICE simulation) for different pitches.

### B. CNTFET area

The total area of the CNTFET is determined by the width of the gate (as for the device structure of Fig. 1). The gate width can be determined by the pitch. By setting the minimum

gate width  $W_{min}$  and the number of tubes  $N$ , the gate width can be approximated as

$$W_{gate} = \text{Max}(W_{min}, N \cdot \text{pitch}) \quad (3)$$

The widths of the source and drain almost approach  $W_{gate}$  and therefore, the contact resistances and capacitances are determined by the widths.

Table 1.  $\eta$  versus pitch ( $V_{DD} = 0.6V$ , diameter = 2nm, channel length = 32nm).

Pitch(nm)	4	6	8	10	12	14	16	18	20
$\eta$	0.59	0.73	0.82	0.88	0.91	0.93	0.95	0.96	0.96

### C. Parameters for CNTFET Circuit Design

#### 1) Threshold voltage

By adjusting the diameter, the threshold voltage can be controlled and is given by [4]

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV_\pi}{eD_{CNT}} \quad (4)$$

where  $V_\pi$  ( $\sim 3.033$  eV) is the carbon  $\pi$ - $\pi$  bond energy in the tight bonding model [4] and  $e$  is the unit electron charge and  $D_{CNT}$  is diameter of CNT. In this paper,  $V_{th} = 0.2V$  is used because of the smallest value of PDP is attained by simulation

#### 2) Gate capacitance

The gate capacitance affects the speed and power consumption, and is determined based on device size. The CNTFET gate capacitance ( $C_{gate,CNT}$ ) consists of three components [8]: the gate to channel capacitance ( $C_{gch,CNT}$ ), the gate outer fringe capacitance ( $C_{fr,CNT}$ ), and the coupling capacitance between the gate and the adjacent contacts ( $C_{gig,CNT}$ ). Because the portion of the  $C_{fr,CNT}$  is much smaller than  $C_{gig,CNT}$  and  $C_{gch,CNT}$ , it can be ignored. Therefore, the total gate capacitance can be expressed as

$$C_{gate,CNT} \approx \{\eta(N-2)+2\}C_{gc\_e,CNT} \cdot C_{gig} \cdot W_g \quad (5)$$

#### 3) Fan-out factor for minimum delay

Its optimum value can be found by differentiating the minimum delay expression [9] by the number of stages and setting the result to 0, i.e.

$$\gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F} \ln F}{N} = \gamma + f - f \ln f = 0 \quad (6)$$

where  $\gamma(C_{int}/C_g)$  a proportionality factor that is only a function of technology and is determined by the pitch and the gate width, (that also determines the intrinsic capacitance),  $F$  denotes the overall effective fan-out of the circuit and  $f$  denotes the effective fan-out factor. For CNTFETs, the value of  $\gamma$  can be found by HSPICE simulation. It is a function of the pitch and the number of tubes. Using the simulated value of  $\gamma$ , the optimum fan-out factor  $f$  is given by 4.

## III. DESIGN METHODOLOGY FOR CNTFET CIRCUIT WITH PERFORMANCE OPTIMIZATION

1) *Optimum number of CNTs for minimum delay.*

For driving a load in CMOS technology, the ratio between the load and driver's gate capacitances is often used. In CMOS, this ratio is almost same as the ratio  $(W_{load}/L_{load})/(W_{driver}/L_{driver})$ . However for CNTFET, as shown in a previous section, the gate capacitance is not proportional to the number of carbon nanotubes. This is caused by the screening effect that affects the gate capacitance and the current. Therefore, it is important to choose a right number of tubes in each driver and load. As an example, a buffer chain is considered; in this circuit, the ratio between the gate capacitance of the  $i$ -th inverter and the next stage is

$$\{\eta(N_i - 2) + 2\}C_{gc\_e} \approx f \{\eta(N_{i-1} - 2) + 2\}C_{gc\_e} \quad (7)$$

Equation (8) is obtained by solving Equation (7) for  $N_i$

$$N_i = f \cdot N_{i-1} + 2 \left( 1 - f + \frac{f}{\eta} - \frac{1}{\eta} \right) = f \cdot N_{i-1} + K(f, \eta) \quad (8)$$

$$\text{where } K(f, \eta) = 2 \left( 1 - f + \frac{f}{\eta} - \frac{1}{\eta} \right)$$

$N_i$  denotes the number of carbon nanotubes of the  $i$ -th stage, and  $f$  is the effective fan-out factor.  $K(f, \eta)$  is a function of  $f$  and  $\eta$  and the values are determined by the pitch and the number of tubes in the CNTFET. Based on  $\gamma$  obtained from extensive simulations, the optimum value of  $f$  turns out to be 4 and the value of  $\eta$  can be found from Table 1.

2) *Logical effort for combinational logic.*

The so-called logical effort of a gate denotes the additional input capacitance of a gate to deliver the same output current as an inverter. The logical effort is an important figure of merit, because it is used to reduce the path delay of a circuit[9] [10].

Table 2. Logical Effort for CNTFET and CMOS

Number of Inputs	Logical Efforts				
	Inverter	NAND		NOR	
		CNFET	CMOS	CNFET	CMOS
1					
2		3/2	5/4	3/2	7/4
3		4/2	6/4	4/2	10/4
4		5/2	7/4	5/2	13/4
n		(N-1)/2	(N+3)/4	(N-1)/2	(3n+1)/2

In a CNTFET, the P-type and N-type have almost the same carrier mobility unlike CMOS technology (which is 3:1). Therefore, the sizes of the P-type and N-type CNTFETs can be the same in inverter. Table 2 shows the logical efforts for CNTFET and 32nm CMOS gates. Based on the CNTFET logical effort, different measures (such as the path logical effort, the path electrical effort, the path effort, the path branching effort, the path delay and the path effort delay) can be found [10]. Let's consider the circuit in Figure 5 as an example. The logical effort can be used to reduce the delay of this CNTFET based circuit. The path logical effort is given by  $G = (1) \cdot (4/2) \cdot (3/2) \cdot (1) = 12/4$ , the path electrical effort is  $H = 5$ , the path branching effort is  $B = 3 \times 2 = 6$ , the path effort is  $F = GBH = 152$ , and  $f = \sqrt[3]{F} = 5.3$ . As the parasitic delay is  $P = 2 + 3 + 2 = 7$  the minimum path delay is  $D = 3 \cdot 5.3 + 7 = 23$ , and

the gate capacitance to accomplish the delay are computed as  $y = 45 \cdot (3/2) / 5.3 = 12.7$  and  $x = (12.7 + 12.7) \cdot 4/2 / 5.3 = 9.6$ .

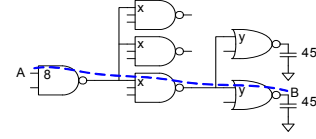


Figure 5. Example of circuit for logical effort

To establish the number of tubes for each gate can be found using the Equation (8). Assume the first stage inverter gate has 8 tubes and its pitch is 4nm, then the 3-input NAND gate in the next stage can be found by using  $\eta = 0.6$  for 4nm pitch,  $f = 9.6/8 = 1.2$ , and  $N_{i-1} = 8$ . Therefore, the number of tubes of the three input NAND gate is 12. Similarly, the number of tubes for the third stage 2-input NOR gate can be found to be 16.

IV. SIMULATION RESULTS

The technology parameters for the CNTFETs are used as an default of CNTFET HSPICE library[4] except diameter and pitch, gate width.

1) *Delay*

To verify the proposed design methodology to find the number of tubes for each logic stage, an inverter chain is designed and its delay has been simulated. Each CNTFET in the inverters has the same pitch (4nm) and fan-out factor ( $f=4$ ) except for the fourth stage which is the load. The load has 64 tubes and 20nm pitch. Theoretically, the number of tubes for the second stage must be 8 from Equation (8). However, since an approximation was used when deriving Equation (8), the exact number of tubes for the second stages can be different from 8. Extensive simulations were performed for different numbers of tubes near the value of 8 for the second stage to find the optimum delay. The optimum number of tubes is found in the same way for the third stage.

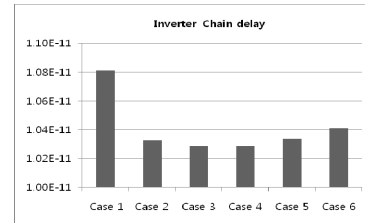


Figure 6. Inverter chain delay for 6 cases.

Six different cases are simulated for different number of tubes in each stage. The number of tubes in each stage is denoted as  $(1^{st}, 2^{nd}, 3^{rd}, 4^{th})$ . From case 1 to case 6, the numbers of tubes are  $(1, 4, 16, 64)$ ,  $(1, 6, 24, 64)$ ,  $(1, 7, 32, 64)$ ,  $(1, 8, 36, 64)$ ,  $(1, 9, 40, 64)$ ,  $(1, 10, 44, 64)$ , respectively. For Case 1, the screening effect is not considered. For all cases, the first stage inverter has only one tube (corresponding to a minimum sized inverter), the number of tube for the second stage (i.e.  $(4, 6, 7, 8, 9, 10)$ ) was chosen near the theoretical value (8), and the number of tubes for the third and the fourth inverters are determined based on

Equation (8). The delay of the inverter chain is shown in Figure 6. These results show that either case 3 or case 4 provides the best delay and this value is close to the value obtained from Equation (8). Therefore, simulation has shown that the proposed methodology is effective in finding the optimum number of CNTs for minimum delay. Figure 7 shows the results of the case where the logical effort approach is used to find the optimum gate size for the circuit shown in Figure 5. Two cases are considered. The first case is the practical one with the screening effect (pitch 4nm,  $\eta=0.6$ ) and the other corresponds to the ideal case in which there is no screening effect (pitch 20nm,  $\eta=1$ ). In both cases, the numbers of tubes are calculated from Equation (8). From these results, a 48% difference between ideal and non-ideal cases is found, which shows that the minimum delay can be achieved even with the presence of the screening effect by using the proposed methodology to find optimum pitch and fanout, diameter, number of CNTs (Carbon Nano Tube).

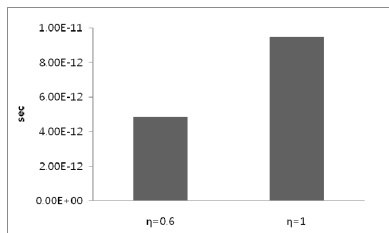


Figure 7. Delay of the circuit in Figure 5 using logical efforts and proposed design method. ( $\eta=0.6$  and 4nm pitch,  $\eta=1$  and 20nm pitch for ideal CNTFET case)

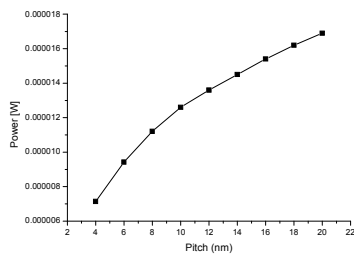


Figure 8. Power consumption of inverter (channel length =32nm,  $V_{DD} = 0.6$ ,  $V_{th} = 0.2$  number of tubes =4) versus pitch

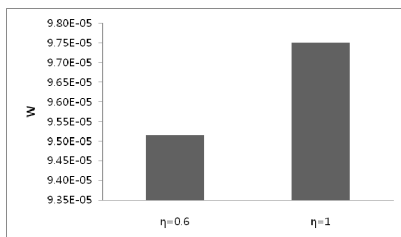


Figure 9. Power consumption of the test circuit in Figure 5

Both the gate capacitance and the current are reduced due to the screening effect at a small pitch. Both reductions cause to dissipate a smaller amount of power. Figures 8 and 9 show the power consumption of the inverter and test circuits with channel length =32nm,  $V_{DD} = 0.6$ ,  $V_{th} = 0.2$ , and number of tubes =4. As expected, the small pitch consumes less power.

## V. CONCLUSIONS

In this paper, a new design methodology for CNTFET was proposed. The characteristics of CNTFET is different from conventional bulk CMOS. These characteristics are explained in this paper and a design method for CNTFET circuits was investigated based on the characteristics. By choosing the diameter form chirality, the threshold voltages can be determined. The channel capacitance and current vary as pitch changes because of screening effects. With these factors, the gate capacitance was approximated with number of tubes in device and optimum fan-out factor was found. Using those parameter, logical effort was calculated and the minimum delay of multistage circuit topology was analyzed. To prove the effectiveness of the proposed circuit design method, simulations have been performed using HSPICE with CNTFET library [4][5], and their results demonstrate that the proposed design methods are effective and practical. In order to design the CNTFET circuit, circuit designer have to take into account the diameter at certain chirality, pitch, and the optimum number of tubes. Considering all those factors, this paper proposed the design methods to find the optimum pitch, diameter, number of CNTs (Carbon Nano Tube), optimum fan-out factor, and proved their legitimacy. It will be a good reference for the future design methodology for any other emerging technologies.

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