

A Novel CNTFET-Based Ternary Logic Gate Design

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Abstract—This paper presents a novel design of ternary logic inverters using carbon nanotube FETs (CNTFETs). Multiple-valued logic (MVL) circuits have attracted substantial interest due to the capability of increasing information content per unit area. In the past extensive design techniques for MVL circuits (especially ternary logic inverters) have been proposed for implementation in CMOS technology. In CNTFET device, the threshold voltage of the transistor can be controlled by controlling the chirality vector (i.e. the diameter); in this paper this feature is exploited to design ternary logic inverters. New designs are proposed and compared with existing CNTFET-based designs. Extensive simulation results using SPICE demonstrate that power delay product is improved by 300% comparing to the conventional ternary gate design.

I. INTRODUCTION

Traditionally, digital computation is performed on two-value logic, i.e. there are only two possible values (0 or 1, true or false) for any proposition to take in the Boolean space. Multiple-valued logic (MVL), such as ternary logic (or three-valued logic), has attracted considerable interests due to its potential advantages over binary logic for designing digital systems. Compared with binary logic, ternary logic allows more information to be transmitted over a given set of lines or stored for a given register length, thus reducing the complexity of interconnects and chip area and achieving simplicity and energy effectiveness in digital design [1]. Furthermore, serial and serial-parallel arithmetic operations can be carried out at higher speeds if ternary logic is employed. Extensive research on the design and implementation of ternary logic using complementary metal-oxide semiconductor (CMOS) can be found in the technical literatures [1] [2]. It has been shown that chip area and power dissipation can be reduced by more than 50% using an efficient MVL implementation of a signed 32-bit multiplier compared to its fastest binary counterpart [3]. MVL modules have been inserted in binary logic ICs to enhance performance of CMOS technologies [4].

Scaling in CMOS has resulted in increased short-channel effects, reduced gate control, exponentially rising leakage currents, severe process variations, and high power densities. As today's VLSI systems mostly rely on silicon CMOS technology, it has been predicted that in the nano regimes, its expected high density will encounter substantial difficulties (as related to physical phenomena and technology limitations), possibly preventing the continued improvements in figures of merit for low power

and high performance operation. New materials and devices have been investigated to replace silicon in nanoscale transistors from the year 2015 and beyond. Carbon nanotube transistors (CNTFETs), for example, are especially promising because their unique one-dimensional band-structure suppresses backscattering and makes near-ballistic operation a realistic possibility [5]-[7].

The multi-threshold CMOS design relies on transistor body effects that apply different bias voltages to the base or the bulk terminal of the transistors. The threshold voltage of a CNTFET is determined by the CNT diameter. Therefore, a multi-threshold design can be accomplished by employing CNTs with different diameters (and therefore, chirality) in the CNTFETs. In this paper, a novel multi-valued logic design based on multi-threshold CNTFETs is proposed, assessed, and compared with existing multi-valued logic designs based on single-threshold CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in [3], however, in this configuration large off-chip resistors (of at least 100M Ω values) are needed due to the current requirement of the CNTFETs. The design technique in this paper eliminates the large resistance issue by employing the proposed ternary logic design with P-type transistor loads.

In this paper, the design of new ternary logic inverters based on CNTFETs is presented. These designs are described in detail, and the extensive HSPICE simulation results demonstrate substantial advantages in terms of speed and power consumption.

II. REVIEW OF TERNARY LOGIC

The ternary logic functions are defined as those functions having significance if a third value is introduced to the binary logic. In this paper, 0, 1, and 2 denote the ternary values to represent false, undefined, and true, respectively. Any n variable (x_1, \dots, x_n) ternary function $f(X)$ is defined as a logic function mapping $\{0,1,2\}^n$ to $\{0,1,2\}$, where $X=\{x_1, \dots, x_n\}$. The basic operations of ternary logic can be defined as follows, where $x_i, x_j \in \{0,1,2\}$ [8]:

$$\begin{aligned} X_i + X_j &= \max \{X_i, X_j\} \\ X_i \cdot X_j &= \min \{X_i, X_j\} \\ \overline{X_i} &= 2 - X_i \end{aligned} \quad (1)$$

where the notation is as follows: $-$ denotes the arithmetic subtraction; the operations $+$, \cdot , and $\overline{}$ are referred to as the OR, AND and NOT in ternary logic, respectively.

TABLE I.
LOGIC SYMBOLS

Voltage Level	Logic Value
0	0
$1/2 V_{dd}$	1
V_{dd}	2

TABLE II.
TRUTH TABLE OF STI, PTI, AND NTI

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

The most fundamental building block in the design of digital systems is the ternary inverter. The logic symbols defined for the ternary logic are shown in Table I. Ternary gates are designed according to Equation (1). A general ternary inverter is an operator (gate) with one input x , and three outputs denoted by y_0 , y_1 , and y_2 such that

$$\begin{aligned} y_0 &= C_0(x) = \begin{cases} 2 & \text{if } x = 0 \\ 0 & \text{if } x \neq 0 \end{cases} \\ y_1 &= C_1(x) = \bar{x} = 2 - x \\ y_2 &= C_2(x) = \begin{cases} 2 & \text{if } x \neq 2 \\ 0 & \text{if } x = 2 \end{cases} \end{aligned} \quad (2)$$

Therefore, the implementation of a ternary inverter would require three inverters, a negative ternary inverter (NTI), a standard ternary inverter (STI), and a positive ternary inverter (PTI), if y_0 , y_1 , and y_2 in Equation (2) are the outputs [1]. The truth table of the three ternary inverters is shown in Table II.

III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Carbon nanotube field effect transistors (CNTFETs) utilize semiconducting single-wall CNTs to assemble electronic devices similar to MOSFETs [5]. A single-wall carbon nanotube (or SWCNT) consists of one cylinder only; the simple manufacturing process of this device makes it very promising for use as a transistor and alternative to today's MOSFET. An SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m) . A simple method to determine if a carbon nanotube is metallic or semiconducting is to consider its indices (n, m) . The nanotube is metallic if $n=m$ or $n-m=3i$, where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the following Equation (3) [9] – [11].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi} \sqrt{n^2 + m^2 + nm} \quad (3)$$

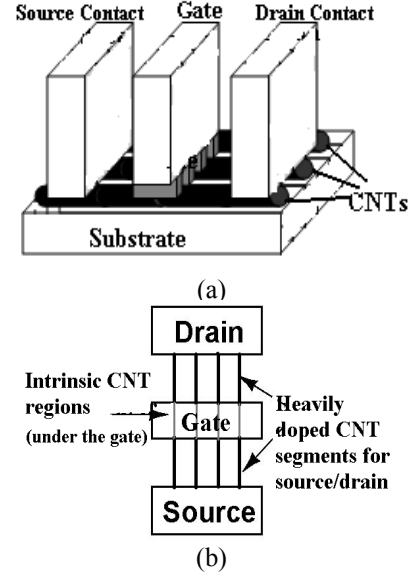


Figure 1. Schematic diagram of a carbon nanotube transistor: (a) cross sectional view; (b) top view.

where $a_0 = 0.142nm$ is the inter-atomic distance between each carbon atom and its neighbor. Fig.1 shows the schematic diagram of a CNTFET [9] – [11]. Similar to the traditional silicon device, the CNTFET has also four terminals. As shown in Fig.1, undoped semiconducting nanotubes are placed under the gate as channel region while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the on-state [5]. As the gate potential increases, the device is electrostatically turned on or off via the gate.

The current-voltage (I-V) characteristics of the CNTFET are similar to the MOSFET's. The threshold voltage is defined as the voltage required to turn on the transistor. The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap, which is an inverse function of the diameter [9] – [11], i.e.

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{aV\pi}{eD_{CNT}} \quad (4)$$

Where $a = 2.49 \text{ \AA}$ is the carbon to carbon atom distance, $V\pi = 3.033 \text{ eV}$ is the carbon π - π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter. As D_{CNT} of a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels, is 0.293 V from (4). As the chirality vector changes, the threshold voltage of the CNTFET will also change. For example, the threshold voltage of a CNTFET using (13, 0) CNTs is 0.428 V while the threshold voltage of a (19, 0) CNTFET is 0.293 V. CNTFETs provide a unique option to control threshold voltage by changing the chirality vector or the diameter of the CNT [3]. [12] [13] have reported advances on processes for manufacturing well-controlled CNTs. Therefore, in this paper, we use a multi-diameter CNTFET-based design for the ternary inverter implementations.

IV. CNTFET BASED TERNARY INVERTER DESIGN

A. Existing Design

A CNTFET based ternary logic design has been initially proposed in [3]. It employs dual-diameter CNTFETs and resistors. Fig.3 shows the schematic diagram of the STI (Standard Ternary Inverter) discussed previously in section II. It consists of two CNTFETs with resistive pull-ups. In this paper, a power supply voltage of 0.9V, (as default value of the CNTFET model of [9]) is used. Therefore, logic 0 corresponds to a voltage value less than 0.3V, logic 1 corresponds to a voltage value between 0.3V and 0.6V, and logic 2 corresponds to a voltage value greater than 0.6V. In Fig.3, one of the transistors (T1) has a diameter $d_1=1.487\text{nm}$ while the other transistor (T2) has a diameter $d_2=0.783\text{nm}$, which makes the two transistors have threshold voltages of $V_{th1}=290\text{mV}$ and $V_{th2}=550\text{mV}$, respectively. When the input voltage is lower than 300mV, both T1 and T2 are off, and the output voltage is 900mV. As the input voltage increases beyond 300mV, T1 is on and T2 is still off, and the output voltage is held approximately at $V_{dd}/2$ until the input voltage reaches V_{th2} . Once the input voltage exceeds V_{th2} , both T1 and T2 are on and the output voltage is pulled down to nearly zero. By choosing CNTFETs with proper threshold voltages, a ternary logic inverter design is achieved. However, as shown in Fig.3, two large resistors, usually greater than $100\text{M}\Omega$, are required using the design of [3], their values are too large to be integrated into the CNTFET technology.

B. Proposed CNTFET-based Inverter Design

One of the most widely used logic design style is static complementary CMOS. The main advantages of the complementary design are robustness, good performance, and low power consumption with little static power dissipation. A complementary CNTFET network can also be used for ternary logic design to achieve good performance, low power consumption and to avoid the use of large resistors, and reduce area overhead. Fig.4 shows the proposed CNTFET based STI design; the standard ternary inverter in Fig.4 consists of six CNTFETs. The chiralities of the CNTs used in T1, T2, and T3 are (19, 0), (10, 0), and (13, 0). From Equation (3), the diameters of T1, T2, and T3 are 1.487nm, 0.783nm, and 1.018nm, respectively. Therefore, the threshold voltages of T1, T2,

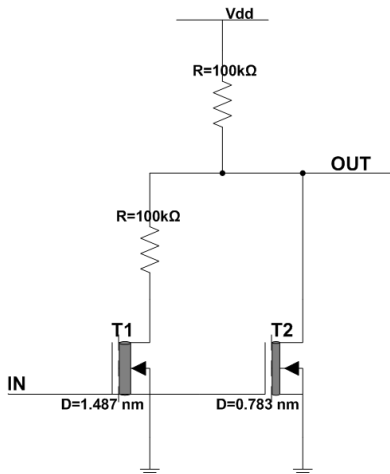


Figure 3. Schematic of the CNTFET-based STI in [3]

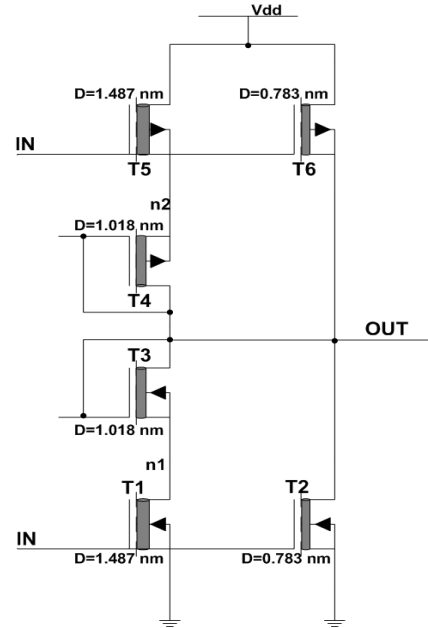


Figure 4. The proposed CNTFET-based STI design.

and T3 are turned out to be 0.289V, 0.559V, and 0.428V, respectively from Equation (4). The threshold voltages of T5, T6, and T4 are -0.289V, -0.559V, and -0.428V, respectively. When the input voltage is changed from low to high at the power supply voltage of 0.9V, initially the input voltage is lower than 300mV. At this moment both T5 and T6 are on and both T1 and T2 are off, which

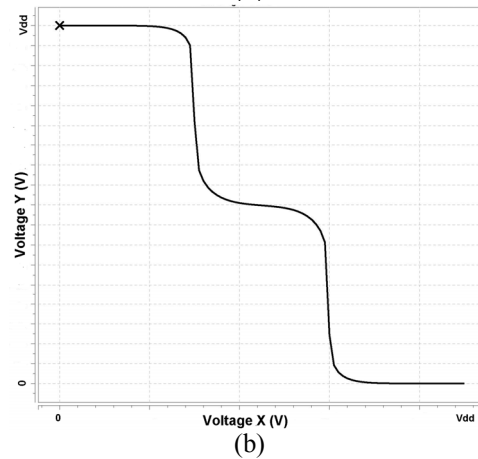
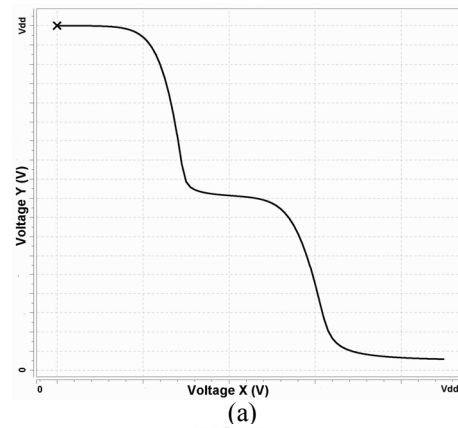


Figure 5. VTC of the STI: (a) STI in Fig.3; (b) STI in Fig.4.

V. CONCLUSION

This paper presented the design of a new ternary circuit based on carbon nanotube field effect transistors (CNTFETs). Based on the fact that the threshold voltage of the CNTFET is function of the geometry of the CNTFET (i.e. the chirality), a novel multi-diameter CNTFET-based ternary design has been proposed for the cost and performance effective ternary inverters.

The proposed ternary inverter design uses multi-diameter (threshold voltage) CNTFETs, and the proposed ternary inverters achieve three times higher performance, low power, and small area due to the removal of resistors compared with previous CNTFET-based designs. All simulations have been performed in HSPICE using the CNTFET model provided by [9]. Simulation results confirm that the power and delay improvement is practical and viable by the proposed ternary inverters.

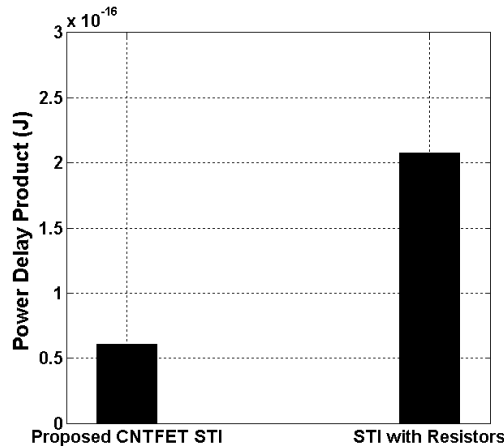


Figure 6. Comparison of power-delay product of the proposed CNTFET-based STIs.

makes the output voltage 0.9V that corresponds to logic 2. As the input voltage increases beyond 300mV, T6 is off and T5 is still on while T1 is on and T2 is off. The diode connected T4 and T3 produce a voltage drop of 0.45V from node n2 to the output and from the output to n1 due to the threshold voltage of T4 and T3. Therefore, the output voltage 0.45V is produced, which is half of the power supply voltage. As shown in Table I, half V_{dd} represents logic 1. Once the input voltage exceeds 0.6V, both T5 and T6 are off, and T2 is on to pull the output voltage down to zero. The high to low transition is similar to the low to high transition.

The voltage transfer characteristics (VTC) of the STI in Fig.3 and Fig.4 are shown in Fig.5(a) and Fig.5(b), respectively. Compared with the conventional STI design in Fig.3, the proposed STI design provides a larger noise margin, which is a positive feature for low power supply circuits. Furthermore, the proposed STI achieves a rail to rail output swing in contrast to the STI design shown in Fig.3.

HSPICE simulation has been performed to investigate the performance of the CNTFET based STI. As the performance metric, the power-delay is used for the CNTFET based STI. In this paper, the power delay product (PDP) is the product of the average power consumption and the average delay. In the simulation setup for HSPICE, two STIs are cascaded as a ternary buffer. Average power consumption is the average power consumption of two STIs, while the average delay is the average of the delay from 0 to 1, delay from 1 to 2, delay from 2 to 1, and delay from 1 to 0.

Fig.6 shows that the proposed CNTFET based STI achieves more than 300% performance improvement in terms of power-delay product. For the NTI and PTI, the circuit configurations are the same and no further comparison is needed. By replacing the external resistors with transistors, a significant saving in area is also achieved. The simulation results confirm that the proposed CNTFET-based ternary inverter is a fast and low-power solution compared with the conventional ternary designs.

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