Assessment of CNTFET Based Circuit Performance and Robustness to PVT Variations

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Abstract— **Carbon nanotubes (CNTs) have superior transport properties, excellent thermal conductivity, and high current handling capability; recently the CNT has been proposed as an alternative device technology to supersede CMOS. In this paper, the circuit-level performance of CNT-based FETs (CNTFETs) is initially compared to MOSFETs; simulation is performed for various logic gates and benchmark circuits to assess the sensitivity to PVT variations using the same minimum gate length. The simulation results show that the delay of CNTFET-based gates is about 10 times lower; moreover, the power delay product (PDP) and the leakage power of CNTFET-based gates are lower than MOSFET based gates by orders of magnitude. These orders of improvements in performance metrics are also achieved while attaining excellent robustness to process, voltage, and temperature variations.**

Carbon NanoTube Field Effect Transistors (CNTFETs); Fan-out; Power; Delay; Power Delay Product (PDP); PVT variation

I. INTRODUCTION

The Carbon NanoTube Field Effect Transistor (CNTFET) is a promising new device that may supersede some of the fundamental limitations of a silicon based MOSFET as encountered in the nano ranges; with ultra long (~1μm) mean-free-path (MFP) for elastic scattering, ballistic or near ballistic transport phenomena can be attained by a CNT under a very low voltage bias and at high performance [1]. Many concerns have been raised for CNTFETs; these concerns are related to manufacturing yield with respect to variations in a carbon nanotube (CNT) diameter, misaligned/misplaced CNTs, and contact resistance. However, different approaches have been proposed to overcome these problems and an extensive literature has appeared to ensure an accurate modeling for electrical simulation [2][3][4][5][6].

Significant efforts have been made in recent years to model and simulate CNT based devices such as the CNTFET [7] and a CNT interconnect [8]. However, these efforts have been concentrated mostly at a device-level. The dynamic performance of a circuit made of multiple CNTFETs and an interconnect has not been properly addressed in the technical literature. Moreover, device-level characteristics may not be fully retained at the higher circuit-level to be viable for manufacturing high performance circuits over the next few years using this new technology. To evaluate the potential benefits of this new technology, the assessment of performance for replacing MOSFETs by CNTFETs is made at circuit level. However, a CNTFET has a different structure than a MOSFET, so comparison of these two technologies should be performed under fair conditions.

In this paper, a new metric for benchmarking is suggested and a detailed performance analysis and comparison between CNTFETs and bulk nano CMOS technology are undertaken at circuit-level for high performance and low power dissipation. Design features (such as same gate length for the transistors) are considered for a fair assessment of these two technologies. Logic gates and benchmark circuits are investigated for performance, energy efficiency, and leakage current under different operational conditions by considering process, power supply voltage, and temperature (PVT) variations. In this manuscript, circuit simulation is extensively employed; it uses the 32nm CNTFET HSPICE model (that includes non-ideal features and conditions for the realization of a CNTFET [3][9]) and the 32nm BSIM PTM (predictive technology model) for a Si MOSFET [10].

II. CNTFET

CNTs are sheets of graphene rolled into tubes; depending on the chirality (i.e., the direction in which the grapheme sheet is rolled), a single-walled CNT can be either metallic or semiconducting. Parallel semiconducting CNTs are grown or transferred to a substrate of CNTFET. A typical structure of a MOSFET-like CNTFET device is illustrated in Figure 1. The CNT channel region is undoped, while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices. The conductivity of these undoped regions is controlled by the gate. A ballistic or near-ballistic transport can be obtained under low voltage bias with CNTs due to the CNTs' ultralong (1 micrometer) mean free path (MFP) for elastic scattering. By positioning additional CNTs, a linear increase in current can be achieved; however, depending on the distance between CNTs (pitch) and the diameter of each CNT, the current cannot be increased linearly with the number of CNTs in a CNTFET because a small pitch causes the so-called screening effect to occur and the diameter determines the amount of current in a CNT [3].

To determine the PMOS/NMOS ratio for CMOS, the transistor width (*W*) is modified. In a CNTFET, the number of CNTs is changed because a CNTFET uses CNTs for the conducting channel between the source and the drain. In this paper, a single-walled CNT with a 17:7 chirality is used; it is also assumed that the CNTs are positioned in parallel and the width of the CNTFET is increased when the number of CNTs in a CNTFET is increased (similar to the width change in a MOSFET).

III. CNTFET DEVICE SIZING

For comparing performance at circuit-level, the inverter (as fundamental logic gate) is usually considered first; in this paper, the inverter is designed with minimal width and a number of tubes in 32nm technology. For Si CMOS, a PMOS/NMOS ratio between 2 and 3 is used for compensating the difference in mobility between PMOS and NMOS. A 3 to 1 (PMOS:NMOS) ratio is used when designing an inverter because the Voltage Transfer Characteristic (VTC) of the MOSFET inverter shows a more symmetrical shape in the center of the logic threshold voltage (VDD/2) at this ratio value for 32nm technology (as shown in Figure 2). However, for the CNTFET, a 1:1 (pFET:nFET) ratio is used because the nFET and the pFET have almost the same current driving capability with same transistor geometry [3]. Figure 2 shows that the VTC of the CNTFET has also a symmetrical shape at a 1:1 (pFET:nFET) ratio. Even though the current in a CNT is smaller than for a minimum sized MOSFET (at 32nm), a CNTFET has a steeper curve in the transition region due to the higher gain. This contributes to a 22.5% improvement in Noise Margin (NM); this improvement in performance is preserved under a decrease in power supply voltage, as shown in Figure 2. In this paper, the ratio value of the inverter is also utilized when designing more complex logic gates and benchmark circuits [11]. Moreover, it is used to determine the width and the number of tubes of the CNTFET.

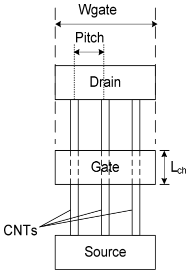

Figure 1. CNTFET Structure

IV. LOGIC GATES PERFORMANCE ANALYSIS

Based on assumptions mentioned in the previous section and design rules for a MOSFET and a CNTFET, basic logic gates are designed at 32nm; delay, power, PDP, and leakage power are simulated to assess their performance. In general, the amount of leakage power is different depending on the applied input vector. In this paper, the maximum leakage power is chosen from the input vectors; Table 1 shows the delay, power, PDP, and maximum leakage power of gates for 32nm MOSFET and 32nm CNTFET technologies. As shown in this table, the PDP and the maximum leakage power of the 32nm CNTFET are about 100 times and 75 times lower than for the 32nm MOSFET.

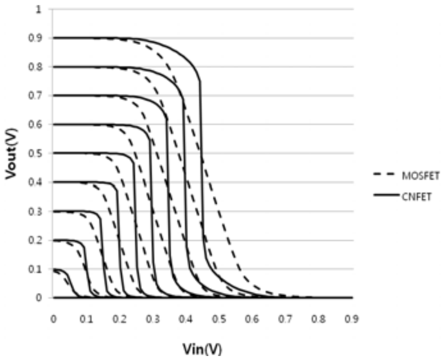

Figure 2. Voltage Transfer Characteristic (VTC) of the 32nm CNTFET and MOSFET inverters for different power supplies

Table 1. Delay, Power, PDP, and maximum leakage power for 32nm MOSFET and 32nm CNTFET logic gates

		Delay (p Sec)	**Power (micro W)**	**PDP (a Joule)**	**Leakage (n W)**
MOSFET	**Inverter**	17.66	1.39	24.58	10.52
	NAND2	22.57	1.96	44.12	21.02
	NAND3	29.92	2.77	82.85	31.51
	NOR2	39.70	2.58	102.50	22.16
	NOR3	69.70	4.04	281.70	33.71
CNTFET	**Inverter**	2.42	0.11	0.27	0.14
	NAND2	3.49	0.19	0.66	0.29
	NAND3	5.06	0.29	1.47	0.44
	NOR2	3.50	0.19	0.65	0.29
	NOR3	5.08	0.27	1.39	0.44

V. LOGIC GATES PVT VARIATION

With technology scaling, the effects of systematic and random variations in process, supply voltage, and temperature (PVT) have led to inconsistent delay and leakage in low power circuits, thus becoming a major obstacle for device scaling [12]. Therefore, the possible performance degradation due to PVT variations has become a major criterion in assessing the performance of a new technology.

A. Process Variation

When investigating physical process variations, channel length and width are usually considered for a MOSFET transistor in MOSFET. However, MOSFET and CNTFET have different characteristics, as evidenced in Figure 3. The current change in a MOSFET is about ±30% (±13%) for a ±10% change in length (width) at a gate voltage of 0.9V while the current change in a CNTFET is below ±0.5%. However when the diameter of the CNTFET is changed by ±10%, the current change in a CNTFET is about ±17%. Therefore for a CNTFET, the diameter variation is more important because a CNTFET is more sensitive to diameter variation than length and width variations. Based on this observation, the PDP and leakage of a CNTFET are computed and plotted in Figure 4 and Figure 5, respectively. When the diameter of a CNTFET is changed, this causes a change in PDP. Figure 5 shows that the maximum leakage power increases when the diameter is increased. Moreover, the threshold voltage and diameter of a CNTFET are determined based on the chirality of the CNTs used in this device.

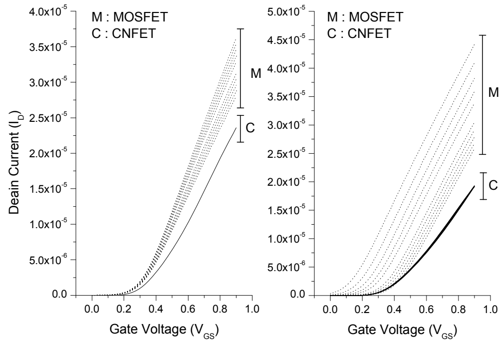

Figure 3. Ids vs. Vgs curve with ±10% change of gate length and width for 32nm MOSFET and 32nm CNTFET.

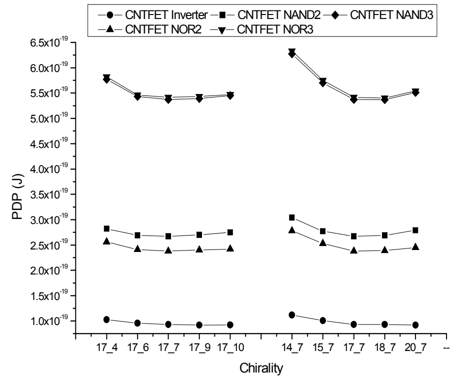

Figure 4. Power delay product (PDP) of 32nm CNTFET logic gates vs. diameter (chirality) of carbon nanotube

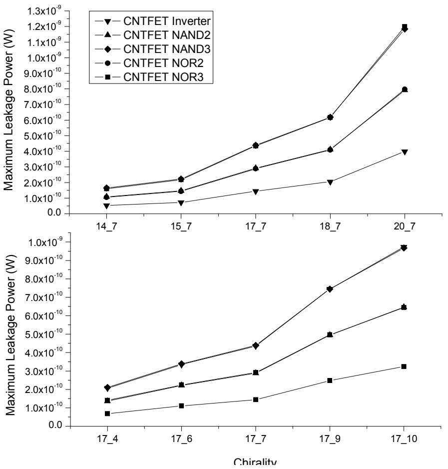

Figure 5. Maximum leakage power of the 32nm CNTFET logic gates vs. diameter (chirality) of carbon nanotube

B. *Voltage Variation*

Figures 6 and 7 show the Power Delay Product (PDP) and maximum leakage power for 32nm MOSFET and 32nm CNTFET logic gates, respectively when the supply voltage is decreased until the gate stops functioning correctly. Even though PDP is changed depending on the supply voltage, the change of PDP in a CNTFET is less than a MOSFET because a CNTFET has a lower gate capacitance and a higher mobility than a MOSFET [2]. The maximum leakage power of the CNTFET (MOSFET) gates decreases linearly (exponentially) as shown on Figure 7, however the overall leakage power of the MOSFET gates is greater than for the CNTFET gates.

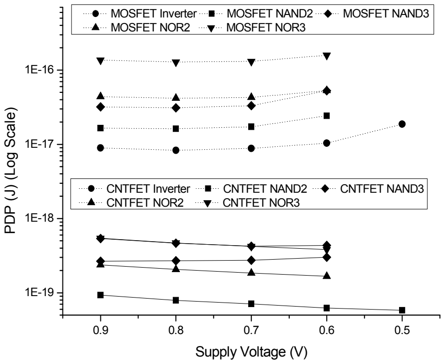

Figure 6. Power delay product (PDP) of 32nm MOSFET and 32nm CNTFET logic gates vs. supply voltage.

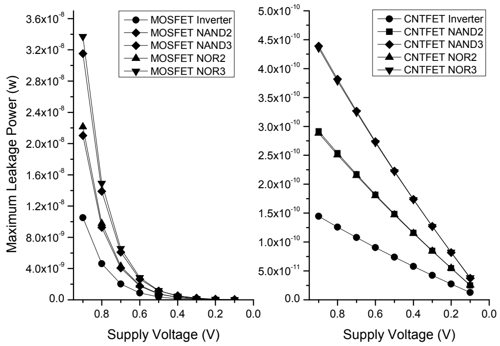

Figure 7. Maximum Leakage Power of 32nm MOSFET logic gates and 32nm CNTFET logic gates vs. supply voltage.

C. *Temperature Variation*

Figures 8 shows that the PDP of the MOSFET gates increases with temperature; however, the PDP of the CNTFET logic gates is constant due to the high thermal stability of CNFETs [13]. Moreover, the maximum leakage power of the MOSFET gates increases linearly with temperature, while for the CNTFET-based gates this increase is exponential (as shown in Figures 9).

VI. PERFORMANCE ANAYSIS

Few combinational circuits have also been evaluated. Table 2 shows the simulation results of circuits designed with 32nm

CNTFET and 32nm CMOS technologies. As shown in Table 2, the average delay and power consumption of the 32nm MOSFET circuits is about 10 times and 100 times higher than for the 32nm CNTFET circuits respectively; these results confirm the findings found previously in Section 4 for the CNTFET and MOSFET logic gates. Moreover, it shows that indeed CNTFET-based designs offer significant improvements over MOSFET-based designs.

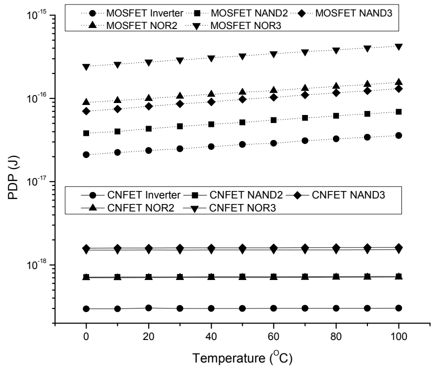

Figure 8. Power delay product (PDP) of 32nm MOSFET and 32nm CNTFET logic gates vs. temperature.

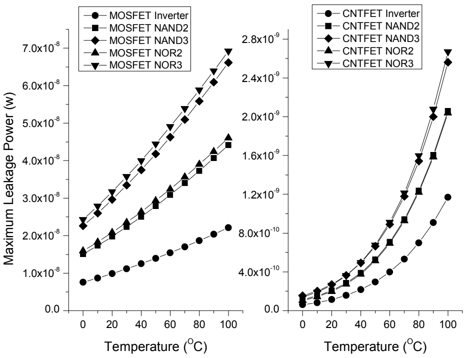

Figure 9. Maximum Leakage Power of 32nm MOSFET and 32nm CNTFET logic gates vs. Temperature.

VII. CONCLUSION

The Carbon Nanotube Field Effect Transistor (CNTFET) is one of the most promising devices among emerging technologies to extend and/or complement the traditional Si MOSFET. In this paper, delay and leakage power consumption of CNTFET gates have been assessed and compared against the counterparts in CMOS using the same minimum gate channel length. Simulation results have shown that the PDP and the leakage of the CNTFET based gates are 100 and 75 times lower than for the MOSFET gates, respectively. This paper has demonstrated the advantages offered by CNTFET gates under different operational conditions such as very low power supply voltage and high temperature. The circuits designed using CNTFET gates have a high robustness to process, voltage, and temperature variations. The quantitative results of this paper have confirmed that CNTFET technology is a viable solution to replace conventional MOSFET technology. Moreover, this paper makes it possible to quantitatively estimate the delay, leakage current, and power of CNTFET-based gates.

Table 2. FO4 Delay, Power, and PDP for 32nm MOSFET and 32nm CNTFET benchmark circuits

		Delay(s)	Power(w)	PDP(joule)
MOSFET	**Inverter Chain**	2.886e-11	9.601e-07	2.771e-17
	2 : 4 Decoder	3.013e-11	7.811e-06	2.354e-16
	4 : 16 Decoder	5.504e-11	1.028e-05	5.655e-16
	C17	3.811e-11	6.969e-06	2.656e-16
	1-bit Full Adder	5.187e-11	9.459e-06	4.906e-16
	3-bit Ripple Carry Adder	8.526e-11	2.530e-05	2.157e-15
	74182	6.401e-11	9.219e-06	5.901e-16
CNTFET	**Inverter Chain**	4.337e-12	8.164e-08	3.541e-19
	2 : 4 Decoder	4.966e-12	7.298e-07	3.624e-18
	4 : 16 Decoder	9.648e-12	1.215e-06	1.173e-17
	C17	6.847e-12	6.712e-07	4.596e-18
	1-bit Full Adder	8.097e-12	9.087e-07	7.357e-18
	3-bit Ripple Carry Adder	1.213e-11	1.299e-06	1.577e-17
	74182	7.668e-12	6.198e-07	4.753e-18

VIII. REFERENCES

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