Probabilistic Leakage Power Estimation of Partially-Depleted Silicon-On-Insulator (SOI) Gates

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***Abstract*— This paper presents a novel probability based analysis for leakage power estimation of Partially-Depleted Silicon-On-Insulator (PD-SOI) circuits. The proposed leakage power estimation algorithms is implemented in C language, and the proposed methodology is tested by ISCAS85 benchmark circuits designed in 100nm SOI technology. The results show that the error is within 4% compared with Hspice Monte Carlo simulation results.**

I. Introduction

Partially-Depleted Silicon-On-Insulator (PD-SOI) has been advocated as a substitute for conventional silicon technology. It has been demonstrated that a SOI transistor offers high performance, dense integration, and reduced power consumption at low operating voltage [1].

Due to the continued scaling device and supply/threshold voltage reduction, leakage power is significant in the power supply dissipation of nanoscale CMOS circuits. Therefore, various methodologies have been proposed to reduce the static leakage power [2][3]. However, only a few methods have analyzed and modeled the leakage power in PD-SOI CMOS circuits; moreover, they do not fully consider the floating body effect on leakage power [4][5].

In PD-SOI CMOS circuits, the main leakage components are subthreshold current and gate leakage current. As transistor geometries are reduced, it is necessary to reduce the supply voltage to avoid electrical break down while it is necessary to reduce transistor threshold voltage(V_{th}) to improve performance. However, the reduced V_{th} increases the sub-threshold leakage current exponentially. To control the short channel effect and increase the transistor driving strength in deep-sub micron circuits, gate-oxide thickness is reduced as technology scales down.

An aggressive scaling in the gate-oxide increases the tunneling current through the oxide exponentially with the oxide thickness and decreases the tunneling current exponentially with the voltage across the oxide [2][3]. In addition, the body voltage of PD-SOI affects these leakage currents because the body voltage is related to the threshold voltage and gate-body tunneling of PD-SOI CMOS. The body voltage is affected by the history effect: the potential of the floating body on PD-SOI is a function of many factors including circuits topology and switching history. In [4][5], the gate leakage current is not considered because these papers focus on the OFF state of simple gates. However, a better understanding and a more accurate model of the leakage currents are essential for an accurate leakage power estimation of PD-SOI CMOS technology.

This paper shows that the accuracy of modeling the leakage current in PD-SOI CMOS circuits is improved significantly by considering interactions between the sub-threshold leakage and the gate tunneling leakage, the stacking effect, the history effect, and the fanout effect along with a new input-independent leakage power estimation method based on a probabilistic approach.

The remainder of this paper is organized as follows. In Section II, statistical leakage power model and analysis of PD-SOI gates are described. Section III shows a new probabilistic leakage power model and analysis for PD-SOI gates. Results from the experimental leakage power analysis on ISCAS85 benchmark circuits are listed and compared with Monte Carlo methods in Section IV followed by conclusion in Section V.

II. Leakage Power Model and Analysis for PD-SOI Gates

The main leakage components are the subthreshold current and the gate leakage current for PD-SOI gates. In particular, the body voltage of PD-SOI affects these leakage currents because the body voltage is related to the threshold voltage and gate-body tunneling of the PD-SOI gate.

A. Gate Leakage Current

Gate leakage is a current flowing(tunneling) into the gate of the transistor. The tunneling current decreases exponentially as gate oxide increase as shown in the following equation.

$$I_{gate_tunneling} = (A \cdot C) \cdot (W \cdot L) e^{-B \cdot \frac{T_{ox}}{V_{gs}} \cdot \alpha} \quad (1)$$

where $A = q^3/8\pi h\phi_b$, $B = 8\pi\sqrt{2m_{ox}}\phi_b^{3/2}/3hq$, $C = (V_{gs}/T_{ox})^2$, α is a parameter that ranges from 1 to 0.1 depending on the voltage drop across the oxide, H is Planck's constant, and ϕ_b is the barrier height for electrons/holes in the conduction/valence band.

The gate tunneling leakage current has been increased to more than twice the sub-threshold leakage current in nanoscale

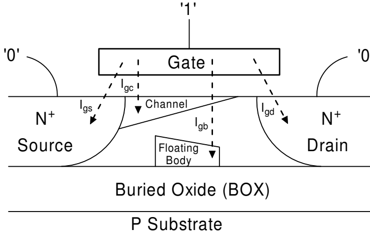
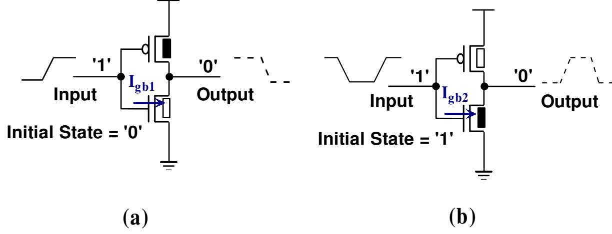


Fig. 1. Gate Tunneling Current of PD-SOI NMOS



(a) (b)

Fig. 2. Gate Tunneling Current in the Different Initial State (a) Initial Input = '0', (b) Initial Input = '1'

CMOS technology. Figure 1 shows the gate tunneling leakage currents of SOI NMOS transistor. As shown in Fig. 1, the gate tunneling current consists of four components: gate-to-channel tunneling (I_{gc}), gate-to-drain edge tunneling (I_{gd}), gate-to-source edge tunneling (I_{gs}), and gate-to-body tunneling (I_{gb}). The magnitude of the gate tunneling is dependent on the applied voltage V_{gs}. For NMOS, four possible states exist depending on the voltages of its three CMOS terminals: drain/gate/source = "1/0/0", "1/0/1", "0/0/1", and "0/1/0". The leakage current under the "0/1/0" state is the highest due to the strong inversion. For PMOS transistor, the current direction and the voltages are the opposite to NMOS transistor (as shown in Fig. 1). Since holes must pass a higher barrier to tunnel, the PMOS tunneling current is less than the NMOS tunneling current [6].

In PD-SOI with thin film, the body current (I_{gb}) is not negligible. The current is changed by the history effect, and it does not affect the body potential at the OFF state transistor. Since the initial input state of the SOI inverter is "LOW" in Fig. 2(a), there is little gate-to-body current initially and the body potential of NMOSFET is close to zero. When the input is changed to "HIGH", I_{gb1} is generated depending on the gate-to-drain voltage only. However, when the initial input state is "HIGH" (as shown in Fig. 2(b)), the gate-to-body current is generated. Therefore, when the input is changed to "HIGH", I_{gb2} flows and its magnitude is greater than I_{gb1} because the body potential is the sum of the previous body voltage and the current body potential.

B. Subthreshold Leakage Current

Even though the transistor's gate voltage decreases below V_{th}, a small current still flows between the source and drain terminals [2][3]. The equation for the sub-threshold leakage current is given by

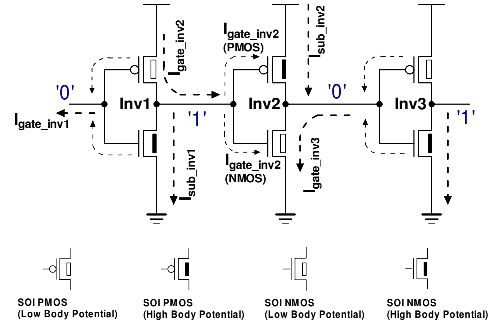


Fig. 3. Leakage Current flows in nanoscale PD-SOI circuits

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_{th}}{\eta kT/q}} (1 - e^{-\frac{V_{ds}}{kT/q}}) \quad (2)$$

where $I_0 = \mu_0 C_{ox} (W/L) (\frac{kT}{q})^2 (1 - e^{1.8})$, W and L are the transistor channel width and length, μ_0 is the low field mobility, C_{ox} is the gate oxide capacitance, k is Boltzmann's constant, q is the electronic charge, and N is the sub-threshold swing factor.

In PD-SOI, the threshold voltage (V_{th}) is inversely proportional to the body potential, i.e. the high body potential makes the threshold voltage low, and the subthreshold voltage increases. Therefore, the history effect of PD-SOI affects the subthreshold leakage current.

C. Stacking Effect and Fanout Effect

When there are two or more stacked off-transistors, the sub-threshold leakage is reduced. The reduction depends on the input pattern during standby periods because it determines the number of OFF transistor in the stack. Figure 3 shows the static current paths that can appear when the leakage current is considered in CMOS circuits. In the circuits, each inverter has a few paths of subthreshold and gate tunneling leakage current. It is assumed that Inv2 is the DUT (Device Under Test), and the input of the Inv1 is '0'. Inv2 has three leakage components that are dependent on the fanout structures of the Inv2.

- The first component is the gate tunneling current I_{gate_inv2} starting from the PMOS of Inv1.
- The second is the subthreshold leakage of the turned-off state PMOS in Inv2 (I_{sub_inv2}).
- The last component is the gate tunneling current I_{gate_inv3} staring from Inv3.

Therefore, the total leakage current is the sum of I_{gate_inv2}, I_{sub_inv2}, and I_{gate_inv3}. In Fig. 3, I_{gate_inv3} should be considered as the gate tunneling leakage of Inv3, i.e. only I_{gate_inv2} and I_{sub_inv2} are the leakage currents of Inv2. Depending on the primary input pattern, the subthreshold leakage current and the gate tunneling are affected by adjacent fanout logic circuits. Figure 4 illustrates the dependence of the leakage current on the fanout structures.

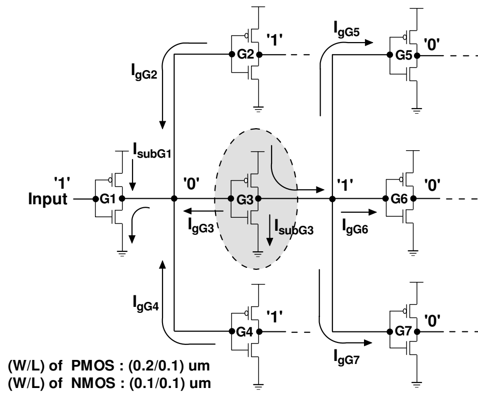


Fig. 4. Fanout effect for G3 gate

In Fig. 4, the primary input is logic ’1’, the number of fanouts of inverter G2 is two, and the number of fanouts of inverter G3 is three. First, the current I_{gG3} is the gate tunneling leakage of inverter G3. In this circuit, I_{gG2} and I_{gG4} are the gate tunneling leakage current of G2 and G4, respectively. The directions of the three currents converge into the input of inverter G3.

The sum of gate leakage current at node N3 is a function of fanout of gate G1 and the subthreshold current of G2, G3, and G4. The ’0’ state voltage at node N3 increases as the fanout of G1 increases, which in turn reduces the gate leakage current of G2, G3, and G4 since the voltage between the input and output of those gates are reduced. The gate leakage current of G2, G3, and G4 are also a function of their subthreshold current since the subthreshold currents affect the voltage between the input and output of those gates. Considering these fanout effects, I_{gG3} is about one third of the gate tunneling leakage of the case where G1 has only one fanout. Consequently, the subthreshold current is influenced by the number of fanouts of the previous driver. However, the fanout of inverter G3 cannot have a significant effect on the leakage current of the inverter G3. As the number of fanout of G3 increases, the output voltage of G3 is reduced, and then the subthreshold leakage and gate tunneling leakage of G3 are reduced.

In summary, the total leakage of inverter G3 is affected by the fanouts of G1 and G3 and it is necessary to consider the interaction of each leakage current component in both previous stages and the next stages for an accurate leakage estimate in nanoscale CMOS circuits. However, the effects of the leakage current components beyond one logic level from the DUT is negligible.

Figure 5 presents the fanout effect on the leakage current for inverter G3 shown in Fig. 4. The leakage currents are measured at inverter G3 in Fig. 4. The number of fanouts of G1 is varied from 1 to 5, and the number of fanout circuits is varied from 1 to 5. It is assumed that the history effect is ignored to show the fanout effect on SOI gates only. Figures 5 (a) and (b) show the subthreshold leakage and gate tunneling, respectively when the input of the inverter G3 is ’1’. Figures 5(c) and (d) show the subthreshold leakage and gate tunneling, respectively when

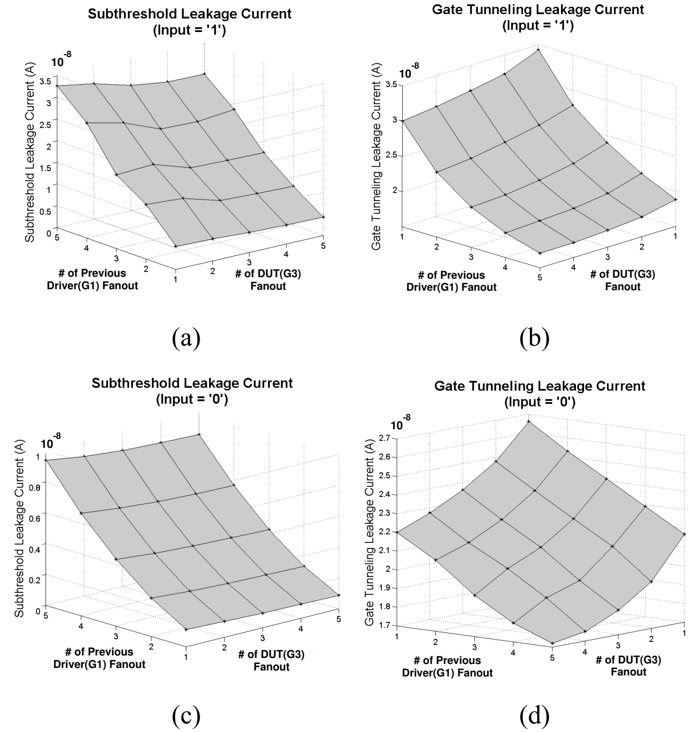


Fig. 5. Leakage Current Variation due to fanout effect in BSIMSOI 100nm technology: (a) Sub-threshold leakage current (Input=’1’), (b) Gate tunneling leakage current (Input=’1’), (c) Subthreshold leakage current (Input=’0’), (d) Gate tunneling leakage current (Input=’0’)

the input of the inverter G3 is ’0’. As expected, the number of fanouts of G1 affects the leakage current. For the ’0’ input to G3, the fanouts of G3 have a considerable effect on the leakage current, but less than the fanouts of the previous driver.

The smallest total leakage (2.29 μA) is measured for the ’0’ input with one fanout of G1 and five fanouts of G3. The highest total leakage (5.15 μA) is observed for the ’1’ input with five fanouts of G1 and one fanout of G3. If the fanout effect is not considered to model the leakage current, the smallest total leakage is 3.32 μA under the ’0’ input and the largest total leakage is 6.13 μA under the ’1’ input.

III. Probabilistic Leakage Power Model and Analysis for PD-SOI Gates

The leakage current in bulk nanoscale CMOS circuits is dependent on the input state. Therefore, models and analysis algorithms have been proposed to estimate the leakage current based on input patterns. Although these algorithms are very accurate, the input dependent analysis is very time consuming. In a few papers, static (input-independent) analyses have been proposed for leakage current using the probability of occurrence of the inputs and outputs [7][8]. However, these methodologies are limited to bulk CMOS circuits only. In this paper, a new analysis method is proposed by considering the history effect of PD-SOI. Unlike static timing, the probability analysis for leakage current does not need any transition information, i.e. the analysis requires only signal state propagation.

TABLE I

EXPERIMENTAL RESULTS FOR LEAKAGE POWER

Circuit	# of gates	error(%)	Monte Carlo Simulation		Proposed Method for Leakage Power	
			CPU time (sec)	Leakage (μW)	CPU time (sec)	Leakage (μW)
C432	160	1.20	7007.18	7.89	43.64	7.99
C499	202	4.00	9090.32	6.24	56.35	5.99
C880	383	1.83	12830.12	15.85	120.34	16.54
C1355	546	3.11	17070.68	24.74	180.58	23.97
C2670	1193	2.75	2810.24	68.76	425.62	66.87
C3540	1669	2.00	3454.56	81.49	650.73	83.12
C5315	2307	1.49	4759.68	128.54	850.53	430.45

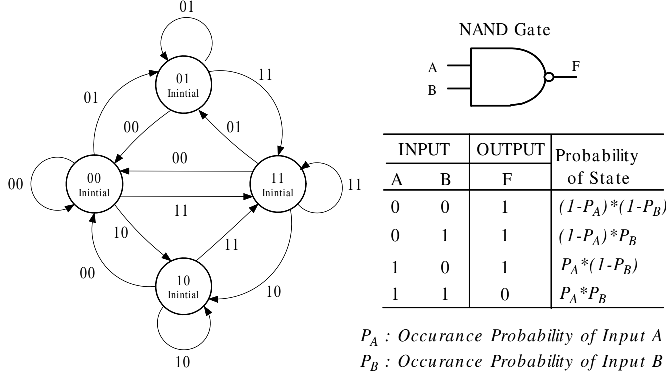


Fig. 6. Probability of Occurrence of Output States for a 2-Input Nand

Figure 6 shows the calculation methodology of the occurrence probability of a 2-input nand gate by considering the history effect. The table in Fig. 6 presents the well known probability calculation method in combinational logic. However in SOI gates, the initial state is required to calculate an accurate leakage current. The state diagram in Fig. 6 shows all the possible states by considering the initial and present inputs. For all initial and current states, the look-up tables are pre-characterized.

Finally, the average leakage current in PD-SOI gates is the sum of the leakage currents for all gates in each initial and present states, i.e.

$$Average_Leakge = \sum_i \sum_j P_i(j) L_i(j) \quad (3)$$

where i is the number of gates, j is the number of inputs to each gate, $P_i(j)$ is the occurrence probability of each state, and $L_i(j)$ is the leakage power of each state.

IV. EXPERIMENTAL RESULTS

The proposed statistical timing and leakage power analysis for PD-SOI has been implemented in Hspice, and C language and run on a 500MHz UltraSPARC-IIe with 500Mbyte of memory. The algorithm has been evaluated using the ISCAS85 benchmark circuits. Each benchmark circuit has been designed using Hspice in a 100nm BSIMSOI3.2 technology to make the look-up table for random variables. The variables are generated by Monte Carlo simulation with 50 repetitions in Hspice and considering all variation sources in the PD-SOI MOSFET. The primary inputs are characterized by Gaussian distribution.

Table I shows the summary of the leakage power for each case in the Monte Carlo simulation and the proposed method using various ISCAS85 benchmark circuits. The leakage power is measured in Hspice using Monte Carlo simulation, and the proposed methodology considers the fanout effect and the history effect of SOI gates.

The first column shows the circuits, and the second column shows the number of gates in the circuits. The third column is the error between the Monte Carlo simulation and the proposed method. The fourth and sixth columns show the CPU simulation time for each method. Finally, the fifth and seventh columns are the estimated leakage power for each method.

The experiments show that the proposed method has a high accuracy(within a 4% difference) and efficiency in terms of CPU runtime compared with Hspice results.

V. CONCLUSION

PD-SOI MOSFET is a state-of-the-art technology for high performance and low power circuit design. However, as technology scales down below 90nm, leakage current becomes a critical problem. In this paper, to calculate leakage current in PD-SOI gates, a new probability based analysis for leakage current is proposed. The proposed methodology focuses on the fanout effect based on a simple model and the history effect of PD-SOI gates. The experimental results show that the proposed method has a high accuracy(within 4 % error) and efficiency in terms of CPU runtime compared with Hspice.

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