

Energy Efficient PWAM Transmitter Design

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Abstract—PWAM transmitter combines pulse width modulation (PWM) and pulse amplitude modulation (PAM) together to boost the performance of the high speed serial link transceiver. In this paper, two PWAM transmitter architectures are proposed and the performances of them are compared based on the power consumption analysis of the drivers. Bipolar driver is an energy efficient choice for the PWAM scheme. It can save more than half of the driver power consumption. The correct clock scheme for phase selector is also discussed in this work.

I. INTRODUCTION

In recent years, the development of the data transmission speed increases the demand of more sophisticated wireline input/output (I/O) transceiver design. Therefore, some modulation schemes and advanced technologies used in the field of digital wireless communication have been implemented into the wireline communication field to counter the channel loss. Among them, pulse amplitude modulation (PAM)[1], [2] and pulse width modulation (PWM)[3] are two very promising modulation schemes. PAM trades the vertical eye opening with the high frequency loss. For PAM-4, amplitude per signal level is 33% of NRZ while the data rate is twice the data rate of NRZ. Due to the modern low supply voltage process, PAM-4 is the limitation that PAM scheme can reach in today and next generation serial link transceiver design. PWM scheme is also a very popular modulation scheme used in high speed serial link. PWM can increase the data rate as well as PAM based on the same symbol rate. And it is easier to extract the clock from the PWM signal since it guarantees a rising edge in one clock period. In this work, an universal PWAM transmitter design methodology is proposed and the design of energy-efficient PWAM drivers is presented.

II. PWAM TRANSMITTER ARCHITECTURE

[4] first introduced a transceiver that uses both PWM and PAM modulation to boost the data transmission rate. However its application is limited to the relatively low-speed data transmission (250M symbol/s) and it utilizes the conventional PWM and PAM symbol representation. [5] proposes an universal PWAM scheme and jitter analysis methodology. In the following, two different PWAM transmitter architectures will be discussed and the performance of them will be compared. PWAM- $(M \times N)$ scheme combines PAM-M (M is the number of different voltage levels) and PWM-N (N is the number of different pulse widths) together. With M different pulse amplitudes and N different pulse widths, there exist $M \times N$

different symbol representations. $M \times N$ symbols represent $(\log_2 M + \log_2 N)$ bits binary information. Therefore, the bit rate of PWAM- $(M \times N)$ is $(\log_2 M + \log_2 N)$ times the symbol rate. Fig. 1 shows two sets of PWAM symbols: PWAM- (4×4) and PWAM- (4×2) . Using PWAM- (4×4) scheme, the bit rate can be reached four times the symbol rate while PWAM- (4×2) is used, the bit rate is three times the symbol rate. The basic PWAM- (4×4) and PWAM- (4×2) transmitter architecture are shown in Fig 2 (a) and (b) respectively. The transmitter circuit consists of PLL, phase selector, driver and some digital logic. The major difference between PWAM- (4×4) and PWAM- (4×2) transmitter is the design of the differential driver. In the next section, the driver design based on the energy consumption analysis is proposed.

III. ENERGY EFFICIENT DRIVER DESIGN

If the differential pair is used, 3bit information can be transmitted using one symbol in one clock period for PWAM- (4×2) transmitter. There are two different architectures for PWAM drivers: unipolar and bipolar[6], [7]. In unipolar architecture as shown in Fig 3(a), current I is steered either in right or left transistor in the current-steering differential pair. Therefore, even if there is no pulse transmitted, the driver still consumes the same amount of the power since at least one of the transistors in the differential pair is conducted and carries the tail current from supply to ground. However in the bipolar pair as shown in Fig 3(b), all transistors can be closed when there is no pulse transmitted. Assuming four groups of symbols are transmitted with even probability, the average pulse width of the transmitted symbol is $t_b + 1.5t_d$ (averaging $t_b, t_b + t_d, t_b + 2t_d, t_b + 3t_d$). While t_b is the basic pulse width and t_d is the unit pulse width as shown in Fig 1. Therefore, the driver consumes the power only part of the clock period. So it saves the energy consumption of the current source in one clock period. And the switching power to turn on and off the transistors is in the same level of that of the bipolar driver. Another benefit of bipolar PWAM driver is that it can reach the same voltage swing between node *outn* and *outp* as unipolar driver with only half of the tail current. For example, to generate the differential voltage swing of $2IR$, the tail current of unipolar driver is $2I$ and the energy consumption is $2IV_{CC}T$ (where V_{CC} is the supply voltage and T is the clock period to transmit one symbol). In the case of the bipolar driver, the energy consumption is only $IV_{CC}(t_b + t_d)$. The total average power consumption one clock

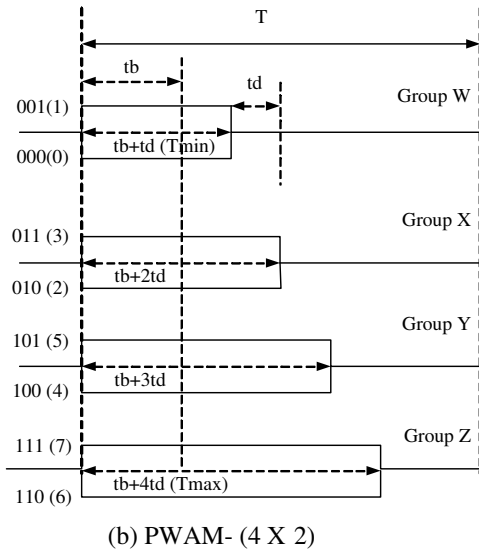
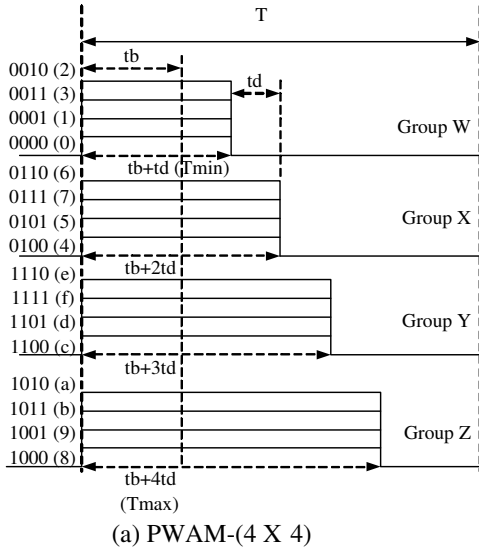


Fig. 1. PWAM scheme: (a) PWAM-(4 × 4) Symbols (b) PWAM-(4 × 2) Symbols

period of the bipolar driver is $\frac{t_b + t_d}{2T}$ that of the unipolar driver. However, the added p transistor pair and current source limit the maximum achievable voltage swing. The bipolar driver also adds the area overhead.

The structure of PWAM - (4 × 4) drivers are shown in Fig 4 (a) (b). In the case of the bipolar driver, the right unit can be turned off whenever $\pm IR$ are to be transmitted to reduce the power. As shown in Table I, if the logic of bit0 and bit1 are opposite, $bit1n1$ and $bit1n2$ are low to turn off the transistor $mn3$ and $mn4$ while $bit1p1$ and $bit1p2$ are high to turn off transistor $mp3$ and $mp4$. Assuming symbol 0,1,...e transmitted with equal probability, average energy consumption per clock cycle is:

$$AVGE = \frac{IV_{CC}(t_b + 1.5t_d) + 3IV_{CC}(t_b + 1.5t_d)}{2} \quad (1)$$

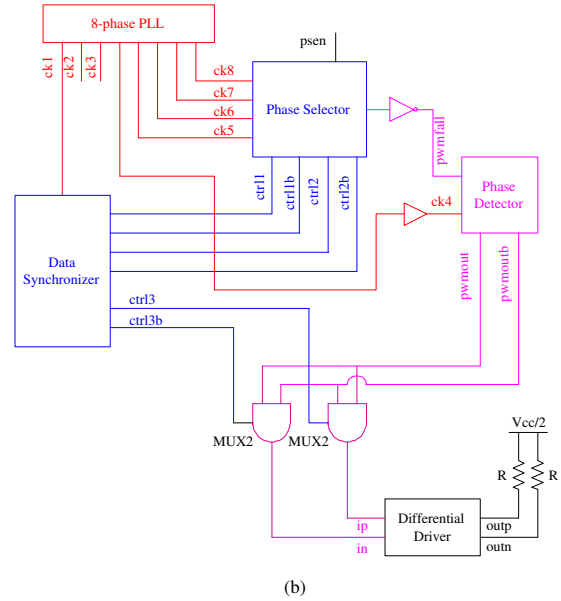
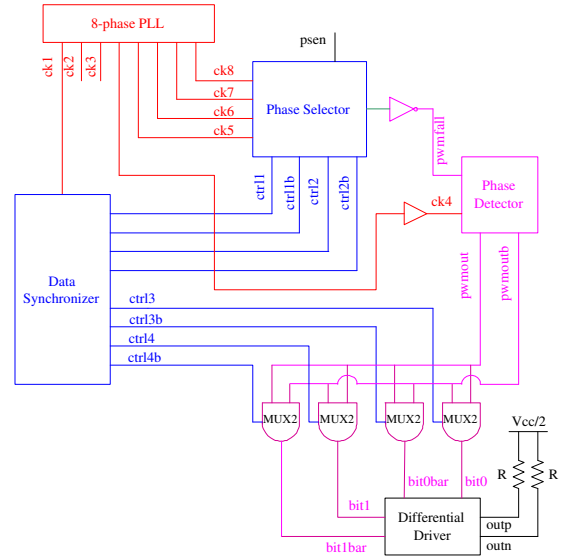


Fig. 2. PWAM Transmitter Architecture: (a) PWAM-(4 × 4) Transmitter Architecture (b) PWAM-(4 × 2) Transmitter Architecture

$$= 2IV_{CC}(t_b + 1.5t_d). \quad (2)$$

While in the unipolar case, to reach the same voltage swing as the bipolar driver, the energy consumption per clock cycle is $6IV_{CC}T$. Therefore, bipolar driver only consumes $\frac{(t_b + 1.5t_d)}{3T}$ the energy the unipolar driver consumes. The performances of four PWAM transmitters are compared in Table II. To be more fair, the power consumption per bit transmitted is compared. Therefore, for PWAM-(4 × 2) driver, the total power consumption has to be divided by 3 while in PWAM-(4 × 4) case, it has to be divided by 4. Also, to keep the same energy to noise ratio, voltage difference of each voltage level is made as $2IR$. In order to make the results more clear, a numerical example is added in the table. In this numerical example, we make $V_{CC} = 1.8V$, $I = 4mA$, $t_b = 250ps$, $t_d = 125ps$,

| Bit0 | Bit1 | Bit1n1 | Bit1n2 | Bit1p1 | Bit1p2 | outp | outn |
|------|------|--------|--------|--------|--------|--------------------------|--------------------------|
| low | low | low | high | low | high | $\frac{V_{DD}}{2} - 3IR$ | $\frac{V_{DD}}{2} + 3IR$ |
| low | high | low | low | high | high | $\frac{V_{DD}}{2} - IR$ | $\frac{V_{DD}}{2} + IR$ |
| high | low | low | low | high | high | $\frac{V_{DD}}{2} + IR$ | $\frac{V_{DD}}{2} - IR$ |
| high | high | high | low | high | low | $\frac{V_{DD}}{2} + 3IR$ | $\frac{V_{DD}}{2} - 3IR$ |

TABLE I
THE TRUTH TABLE OF BIPOLAR PWAM DRIVER

| Driver Type | PWAM - (4 × 2) | | PWAM - (4 × 4) | |
|---------------------------------------|----------------------|----------------------------------|----------------|----------------------------------|
| | unipolar | bipolar | unipolar | bipolar |
| Power Consumption Per Bit | $\frac{2IV_{CC}}{3}$ | $\frac{IV_{CC}(t_b+1.5t_d)}{3T}$ | $1.5IV_{CC}$ | $\frac{IV_{CC}(t_b+1.5t_d)}{2T}$ |
| Power Consumption Per Bit | 4.8mW | 1.05mW | 10.8mW | 1.575mW |
| Total Power Consumption of the Driver | 14.4mW | 3.15mW | 43.2mW | 6.3mW |

TABLE II
THE POWER CONSUMPTION COMPARISON OF EACH PWAM TRANSMITTER IMPLEMENTATION

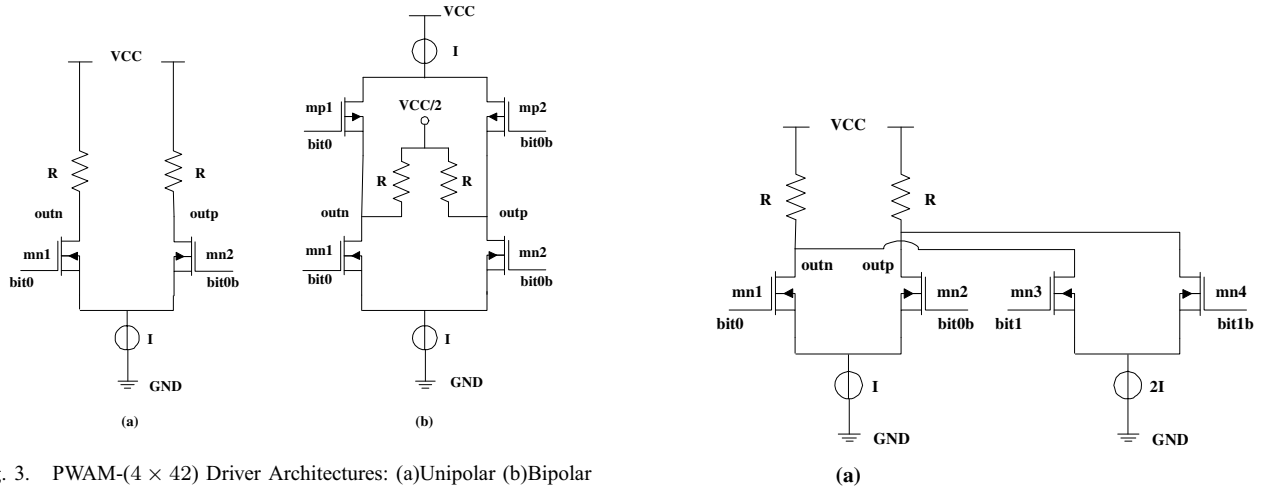


Fig. 3. PWAM-(4 × 2) Driver Architectures: (a)Unipolar (b)Bipolar

$T = 1ns$ and $R = 50\Omega$.

IV. OTHER CIRCUIT BLOCKS

In the section, the remaining circuit blocks in PWAM transmitter are discussed. 8-phase PLL uses the topology proposed in [8]. For the phase selector, instead of the traditional analog method using comparator and sawtooth signal to generate PWM signal, a digital approach to generate PWM waveform is utilized in this work [3]. *ctrl1* and *ctrl0* are used as control signals for the pseudo nMOS phase selector as shown in Fig 5. Four clocks with different phases are chosen according to the different control signals. The output of the phase selector is fed into a phase detector. The operation principle of this phase detector is similar to the phase frequency detector used in the PLL. The rising edge of this signal is combined with the rising edge of another clock signal to generate the PWM waveform. In the circuits of the phase selector, the transition of the different control signals may result in the undesirable rising edge of the signal *pwmfall* as shown in Fig 6(a). So the control signals should be synchronized with the clock 180°

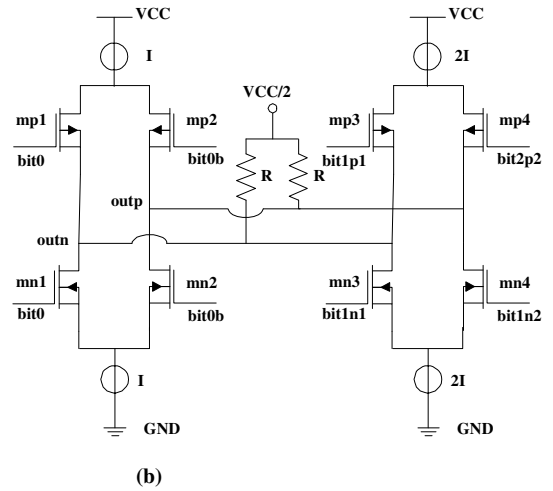


Fig. 4. PWAM-(4 × 4) Driver Architectures: (a)Unipolar (b)Bipolar

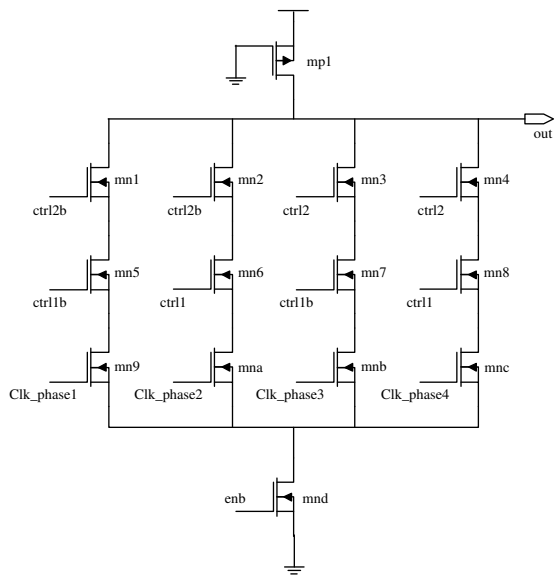


Fig. 5. Phase selector

phase-lead of $CLKPhase1$ to avoid the unwanted rising edges as shown in Fig 6(b).

V. CONCLUSIONS

In this paper, two PWAM transmitter architectures are proposed and the power consumption of each transmitter is analyzed. Bipolar PWAM driver can save a lot of power consumption comparing with the unipolar one. As presented in [8], the power consumption of PLL is around $10mW$. Therefore, the power consumption of the driver is dominant in the power consumption of the whole transmitter. And since the circuits of the PWAM- (4×2) receiver is relatively simpler than that of PWAM- (4×4) receiver. Therefore, PWAM- (4×2) scheme with the bipolar driver is the best solution for today's PWAM transmitter design.

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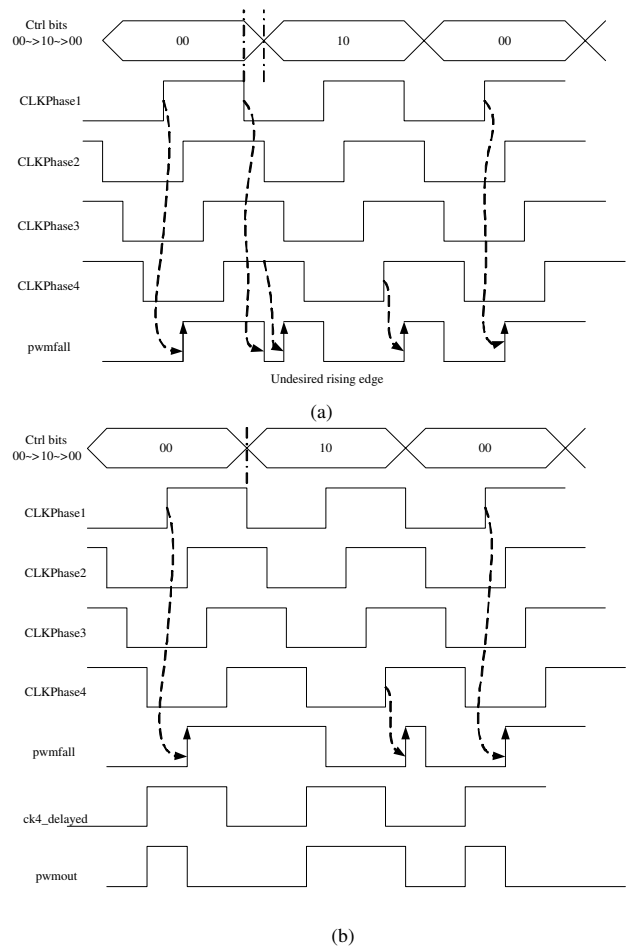


Fig. 6. Timing Diagram of the Phase Selector

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