

A Low Power CMOS CORDIC Processor Design for Wireless Telecommunication

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Abstract—A CORDIC processor for wire telecommunication is integrated in a 0.5 μ m CMOS technology. The CORDIC (coordinate rotation digital computer) processor reduces the circuit complexity by performing a sequence of elementary rotations using shift and add operations without multiplications. Hard wired-logic eliminates the shifter and includes pre-calculated arctan angle values. The average power consumption is 76mW with 50MHz clock and 5V power supply. The fabricated modulator consumes 24mW at 61.44MHz sampling rate and 5V power supply

I. INTRODUCTION

The advent of third generation standards (3G) has created new demands on multimode systems that support various modulation formats such as CDMA and WCDMA [1]. To achieve multi mode operation, transmitters must accommodate constant envelop signals as well as non-constant envelop signals [2]. To avoid distorting non-constant envelops, conventional transmitters must employ linear (class-A) or use predistortion techniques to linearize slightly saturated (class-AB) amplifiers. Both implementations sacrifice power efficiency and result in decreased battery life. Furthermore, I/Q based transmitter design may be problematic in multi-band operation since baseband mixing produces unwanted spurious signals.

Fortunately, a polar modulation offers an alternative for multimode and multiband operations [3]. Figure 1 depicts a high level architecture abstraction of a polar transmitter for WCDMA. The shaded block shows a polar modulator which consists of a CORDIC processor, interpolators, a barrel-shifter, and a DAC-PWM generator. The digitized amplitude envelope and the synchronized phase-modulated RF carrier are recombined at the power amplifier to produce linear and efficient RF transmission.

In burst-mode communication systems, a rapid carrier is crucial. Therefore, a fast rectangular-to-polar conversion of the CORDIC processor is desired. Delay-matching of amplitude and phase is crucial since the restoration of the transmitted data at the PA (Power Amplifier) may be imperfect if the delays are unmatched.

This paper presents a power-efficient CMOS CORDIC processor design using 0.5 μ m CMOS process.

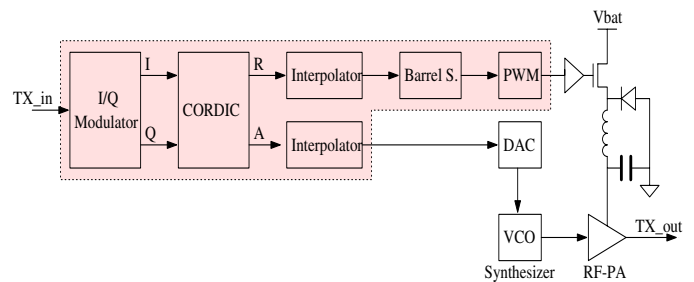


Figure 1. Polar transmitter architecture for WCDMA.

II. CORDIC ARCHITECTURE

There are two well-known implementations for a rectangular to polar coordinate conversion. One method uses a ROM lookup table with both real and imaginary components as inputs. This is practical for lower accuracy requirements as the ROM size grows exponentially with an increasing number of input bits. The other approach is the CORDIC processor [4] which realizes low-cost systems by reducing system complexity. The CORDIC arithmetic technique makes it possible to perform two dimensional rotations using simple hardware components without multipliers.

A distinct feature of the CORDIC algorithm is its use of a sequence of elementary rotations to realize a variety of complicated and non-linear functions. Each rotation requires a simple simultaneous shift and adds operations. By unfolding the iterations for an elementary rotation, a pipelined CORDIC array processor is realized.

A. CORDIC Vectoring Mode for Polar Modulation

The CORDIC algorithm performs a planar rotation which transforms a vector (X_i, Y_i) into a new vector (X_j, Y_j) as shown in Fig. 2a.

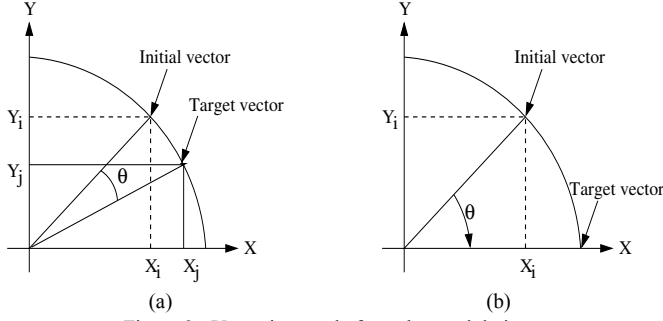


Figure 2. Vectoring mode for polar modulation.

Using a matrix form, a planar rotation for a vector of (X_i, Y_i) is defined as

$$\begin{bmatrix} X_j \\ Y_j \end{bmatrix} = \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} X_i \\ Y_i \end{bmatrix} \quad (1)$$

The θ angle rotation is executed in several steps. Each step is defined in Table I and modified by eliminating the $\cos \theta_n$ factor as

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -\tan \theta_n \\ \tan \theta_n & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix} \quad (2)$$

Implementation of (2) requires three multiplications. Two multipliers are eliminated by selecting the angle steps such that the tangent of a step is a power of 2. The angle for each step is given by

$$\theta_n = \arctan\left(\frac{1}{2^n}\right) \quad (3)$$

All summed iteration-angles are equal to the rotation angle θ .

$$\sum_{n=0}^{\infty} S_n \theta_n = \theta, \quad S_n = \begin{cases} -1 & \text{if } Y_n < 0 \\ +1 & \text{if } Y_n \geq 0 \end{cases} \quad (4)$$

Define a variable Z which represents the part of the angle θ as given in (5).

$$Z_{n+1} = \theta - \sum_{i=0}^n \theta_i \quad (5)$$

These results in

$$\tan \theta_n = S_n 2^{-n} \quad (6)$$

Combining (2) and (6) gives

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos \theta_n \begin{bmatrix} 1 & -S_n 2^{-n} \\ S_n 2^{-n} & 1 \end{bmatrix} \begin{bmatrix} X_n \\ Y_n \end{bmatrix} \quad (7)$$

The $\cos \theta_n$ coefficient is eliminated by pre-computing the final result (assume that $n = 8$).

$$K = \prod_{n=0}^{\infty} \cos\left(\arctan\left(\frac{1}{2^n}\right)\right) \approx 0.607259 \quad (8)$$

TABLE I. 10-BITS BINARY VALUES FOR ARCTAN (2^{-i})

Step	arctan	Angle (degree)	10-bits binary
1	$\arctan(2^0)$	45.0000	7F = 00 0111 1111
2	$\arctan(2^{-1})$	26.5651	4B = 00 0100 1011
3	$\arctan(2^{-2})$	14.0362	27 = 00 0010 0111
4	$\arctan(2^{-3})$	7.1250	14 = 00 0001 0100
5	$\arctan(2^{-4})$	3.5763	A = 00 0000 1010
6	$\arctan(2^{-5})$	1.7899	5 = 00 0000 0101
7	$\arctan(2^{-6})$	0.8952	2 = 00 0000 0010
8	$\arctan(2^{-7})$	0.4476	1 = 00 0000 0001

Ignoring the congruence constant K , CORDIC performs the following formulae.

$$\begin{aligned} X_{n+1} &= X_n - S_n 2^{-2n} Y_n \\ Y_{n+1} &= Y_n + S_n 2^{-2n} X_n \end{aligned} \quad (9)$$

$$Z_{n+1} = Z_n - S_n \arctan(2^{-2^n})$$

As shown in Fig. 2b, the CORDIC computes

$$[X_j, Y_j, Z_j] = \left[\frac{1}{K} \sqrt{X_i^2 + Y_i^2}, 0, \arctan\left(\frac{Y_i}{X_i}\right) \right] \quad (10)$$

where the arctan is pre-calculated.

B. Polar Pre-/Post-processing for WCDMA Transmitters

Since I/Q data-streams' polarity is always positive due to the DAC's input, the origin is moved to the center of data angle as shown in Fig. 3a. Then performing a quadrant move shifts everything to the first quadrant as in Fig. 3b. In post processing, the CORDIC processor recovers the original quadrant and scales the congruence constant.

C. Rectangular to Polar CORDIC Architecture

A CORDIC element (CE) architecture is shown in Fig. 4. The datapath of the CE has 2-bits fixed point extension which reduces truncation errors. Using cyclic convolution provides the advantages of high computing parallelism and low computation complexity. A parallel structure shown in Fig. 5 consists of an array of CEs, each of which performs a computation in parallel and is separated by registers to form a pipelined structure.

The CE is the kernel of the CORDIC processor and its primary function is to perform (9). The rectangular to polar CORDIC accepts three input variables X_i , Y_i , and Z_i and generates the output X_j , Y_j , and Z_j . It is operated in the vectoring mode where variable Y_i is forced to zero.

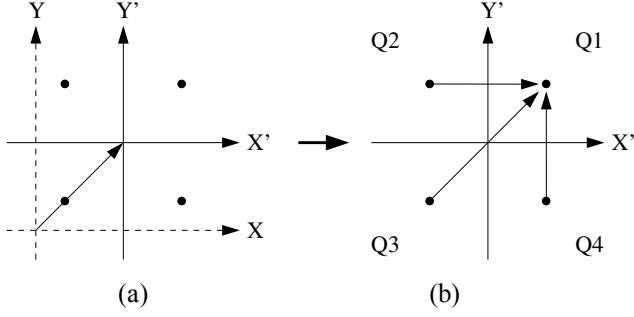


Figure 3. Pre-processing for a polar transmitter

From the hardware implementation point of view, this operation is carried out using only shift and add operations since multiplication of any quantity by 2^{-i} is a shift of the binary representation of the quantity by i -bit to the right.

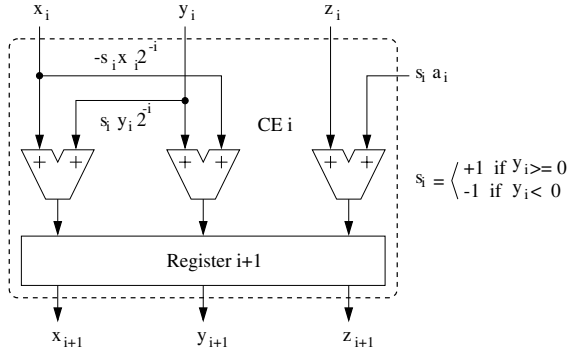


Figure 4. CORDIC element architecture abstraction.

As a result, all the evaluation procedures in CORDIC are computed as a vector rotation in three coordinate systems with an iterative unified formulation. The main components of each CE are three adders, a shifter, a look-up table, and a register. Since the function of the shifter in the pipeline is fixed, the shift operation is implemented by wiring. Moreover, the lookup table is replaced with hardwired logic because each stage has a congruent constant rather than a lookup table. Therefore, only three adders and a register are required for a CE. Figure 5 depicts the entire design, and the pseudo-rotation and the scaling factor blocks are very fast parallel, pipeline structures. Since the RF digital baseband output is unsigned binary and is the input of the CORDIC processor, the unsigned values are converted to signed binary by moving the origin. The pre-processing module also performs a shift to quadrant one from the other quadrants. The function of the post-processing block is to scale the magnitude and to recover the original quadrant. To do this the post-processing stage consists of adders and wired-shifters.

D. Post-processing for WCDMA requirements

For larger word sizes, it is not economical to extend the sampling rate from 8 to 32 times per cycle for WCDMA

input data using the direct ROM approach. Therefore, an unsigned linear interpolation technique is used where the distance between tabulated points is uniform.

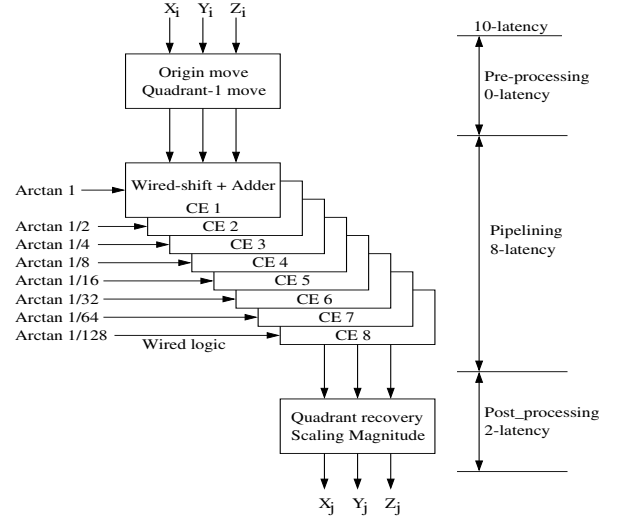


Figure 5. CORDIC processor architecture abstraction.

The interpolation method reduces the clock frequency for CORDIC and the interpolators except for the counter, which in turn decreases the power dissipation of these blocks by factor of 4. The output of the barrel-shifter block reflects a gain from the external inputs. There is an overflow signal which indicates the output of the DAC-PWM module is out-of-range, and the output is fixed as the maximum value. To match the delays of the amplitude and angle, registers are used at the final stage. The angle ports have additional MUXes for serial- and parallel-outputs. The delay difference is less than 1ns. The DAC-PWM module in Fig. 1 converts parallel data to serial data. This makes the switch mode regulator simpler.

III. SIMULATIONS AND EXPERIMENTAL RESULTS

To simulate and verify the CORDIC in the modulator, the input data is generated by a digital I/Q modulator implemented using an Altera Flex10K FPGA. The 10-bit CORDIC processor and other post-processing blocks are modeled in Verilog HDL and are fully synthesized. The datapath of CORDIC core consists of 0-latency pre-processing, 8-latency pipeline, and 2-latency post-processing. To integrate all components of the polar transmitter, the design is mapped onto a $0.5\mu\text{m}$ four-metal CMOS technology. The layout uses the standard cell based design flow of Apollo with 80% core utilization ($1.1 \times 1.3\text{mm}^2$, 10,000 gates). The nominal supply voltage for core cells is 5V. The average power consumption of the proposed architecture without low power circuit techniques is about 24mW with a 61.44MHz clock frequency. Table II shows the vectoring mode average power dissipation comparison with [5]. Figure 6 shows the die photo of the CORDIC for a digital polar modulator. Table II lists the

errors between the results and the calculations caused by truncation and limited pipeline stage. X, Y and X', Y' are the unsigned and the signed 10-bits inputs, respectively (See Fig. 3a). R is the polar magnitude from the origin (512, 512), and A is the polar phase angle whose maximum value 1024(0 indicates 360°). The error between the calculation and the results for the modulator including channel noise is tolerable during demodulating. Note that the % error of A(c) is deviation from 90°.

IV. CONCLUSION

Due to CORDIC's regularity and simplicity, the proposed transmitter architecture is very suitable for VLSI implementation. The CORDIC architecture proposed in this paper adopts a hard-wired pipeline strategy to increase the performance and reduce the size at the architectural level. The separate distribution of angle constants to each adder also permits a hardwire solution instead of using a lookup table, and all the shifters are hard-wired. Moreover, the interpolation method reduces the sampling rate of the CORDIC and the interpolators except for the counter, and, in turn, decreases the power dissipation of those blocks by factor of 4. The delays-matching of amplitude and phase is accomplished in 1ns. The proposed digital polar modulator is designed, integrated, and fabricated using 0.5μm CMOS process; it is tested, and used successfully for CDMA applications. The modulator is a good reference for a low power communication VLSI chip integration, especially SoC (Systems-on-Chip).

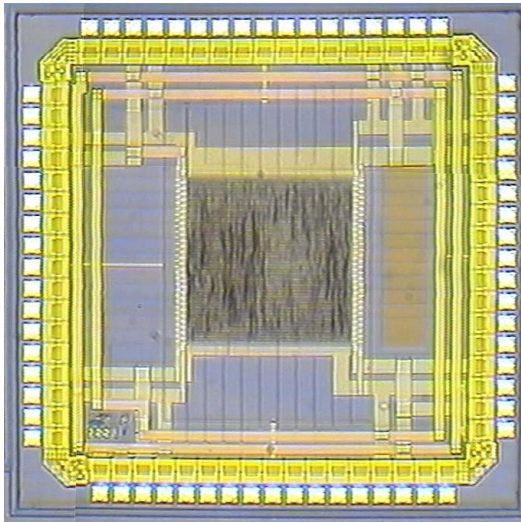


Figure 6. The CORDIC die photo for digital polar modulator

TABLE II. POST-LAYOUT SIMULATION RESULTS AND CALCULATIONS

Input X (X')	Y (Y')	Output		Calculation		Error (%)	
		R(o)	A(o)	R(c)	A(c)	R(c)	A(c)
612 (100)	562 (50)	112	75	111.80	85.33	0.18	4.04
612 (100)	612 (100)	142	127	141.42	128.0	0.41	0.39
612 (100)	712 (200)	224	181	223.61	170.6	0.17	4.04
512 (0)	712 (200)	200	255	200.00	256.0	0	0.39
412 (-100)	712 (200)	224	331	223.61	341.3	0.17	4.04
412 (-100)	612 (100)	142	385	141.42	384.0	0.41	0.39
412 (-100)	562 (50)	112	437	111.80	426.6	0.18	4.04

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