LOW POWER REAL TIME ELECTRONIC NEURON VLSI DESIGN USING SUBTHRESHOLD TECHNIQUE

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ABSTRACT

We discuss a VLSI electronic neuron circuit that implements Hindmarsh and Rose neuron model. Magnitude and time scaling techniques are employed for 2V power supply operation. A subthreshold operation technique and a single MOS resistor are used to minimize area and power consumption. Output bursts of the electronic neuron can be modulated dynamically by varying the input voltage level. The circuit is designed using 0.25μm CMOS standard process, and the total power dissipation is 163.4μwatt.

1. INTRODUCTION

Developing analog locomotion controllers using actual biological neuron circuitry has much advantages over conventional digitized processing using a microcontroller. As the demand for real time adaptability to environment increases, an analog controller becomes more attractive than a digital approach. It is very difficult to process large amounts of sensory input from natural environment with digital circuits. A digital approach requires substantial hardware resources such as analog-to-digital / digital-to-analog converter, adder and multiplier. Although digital controllers show high computing power, their output results strongly depend on the resolution of data, which requires higher power and more area. Analog circuits can process with virtually infinite resolution and much smaller area if low noise is guaranteed, this makes it possible to process large quantities of sensory inputs in real time with low power operation using subthreshold techniques.

An adaptive analog controller consists of neuron and synapse circuits that mimic the biological nervous systems. The neuron's behavior is modeled using Hindmarsh and Rose (HR) differential equations[1]. One approach has been to simulate the neural bursting using an oscillator[2]. However, this is not an exact implementation of actual biological neuron's behavior because the slow adaptation current component (z) is assumed to be constant and the circuit is so reduced that it does not produce realistic bursts. Electronic neurons have been built using 3-dimensional HR model by Pinto, *et al* [3]. This circuit was designed with ± 15V using discrete components, leading to large neuron hardware size and significant power consumption. This paper presents a precise and low power VLSI implementation of HR neuron circuit using small silicon area. Output bursts of electronic neurons can be dynamically modulated by varying input voltage levels. This neuron design is implemented using 0.25μm CMOS technology with 2V power supply voltage. Section 2 explains the neuron model and Section 3 describes the methodology to design neuron circuit with emphasis on low power and small area. Section 4 shows the simulation results followed by conclusion in Section 5.

2. NEURON MODEL

This paper presents a low power electronic neuron implementation of HR neuron model. Compared to other neuron models such as Fitzhugh-Nagumo or Hodgkin-Huxley, the HR model has several advantages. The mathematical equations are simpler than Hodgkin-Huxley model, which is based on global behavior rather than eletrophysiological process. Therefore, it requires less hardware resources and less design complexity. Also this model provides an accurate output frequency-input current relationship, which is not described by Fitzhugh-Nagumo. The equations of HR neuron model are given by [1].

$$\frac{dx}{dt} = y - ax^3 + bx^2 - z + I \tag{1}$$

$$\frac{dy}{dt} = c - dx^2 - y \tag{2}$$

$$\frac{dz}{dt} = r\left(s\left(x - x_1\right) - z\right) \tag{3}$$

where,

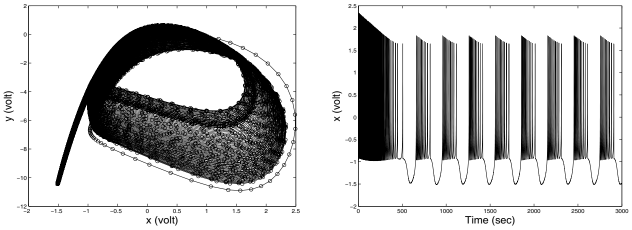
x: membrane potential of neuron, y: recovery current of neuron, z: adaptation current of neuron, I: applied current, and x_1: the leftmost equilibrium point of the neuron model without adaptation.

Coefficients of the Equation (1),(2) and (3) are:

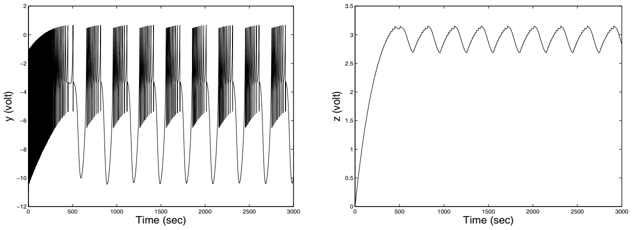
a = 1, b = 3, I = 3.024, c = 1.01, d = 5.0128, r = 0.0021, s

= 3.966, and x_1 = 1.605.

The equations with given coefficients are used to describe the behavior of biological neuron's action potential. Figure 1 (a) shows the solution to the Hindmarsh-Rose neuron model in phase plane. This behavioral simulation provides a reference to design the electronic neuron circuit. The output waveforms are simulated using Matlab and shown in Figures 1 (b) $x(t)$, (c) $y(t)$ and (d) $z(t)$.



(a) Phase Plane (b) X variable



(c) Y variable (d) Z variable

Fig. 1. Solutions of Hindmarsh-Rose Neuron Model

3. DESIGN OF NEURON CIRCUIT

3.1. Magnitude and Time scaling

As shown in Figure 1, the output bursts of the neuron is larger than the power supply range. Also the output frequency is too slow compared to real neuron's burst. For electronic neuron to work at low power supply,the magnitude and the frequency of the neuron outputs must be scaled. Using magnitude scaling factor for x, y, and z (x_{ms}, y_{ms}, and z_{ms}, respectively), and time scaling factor T_s, the following new equations are obtained.

$$\frac{dx}{dt} = \frac{1}{T_s}\left(\frac{y_{ms}}{x_{ms}}y - x_{ms}^2 a x^3 + x_{ms} b x^2 + \frac{1}{x_{ms}}I - \frac{z_{ms}}{x_{ms}}z\right) \tag{4}$$

$$\frac{dy}{dt} = \frac{1}{T_s}\left(\frac{1}{y_{ms}}c - \frac{x_{ms}^2}{y_{ms}}dx^2 - y\right) \tag{5}$$

$$\frac{dz}{dt} = \frac{1}{T_s}\left(r\left(s\left(\frac{x_{ms}}{z_{ms}}x - \frac{x_1}{z_{ms}}\right) - z\right)\right) \tag{6}$$

Figure 2 shows the electronic neuron VLSI circuit to implement Equation (4),(5), and (6) based on the discrete circuit diagram to implement Hindmarsh-Rose model in[3]. To implement this VLSI circuit on silicon, operational amplifiers, current sources, and multipliers are needed. In addition, MOS Resistive Circuits are required to minimize the silicon area.

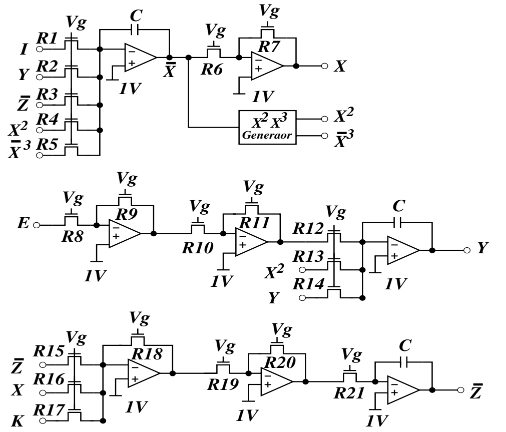


Fig. 2. Hindmarsh-Rose Neuron Circuit.

3.2. Operational Amplifier at Subthreshold region

Major issues in designing neuron circuit are area and power consumption due to battery operation of the adaptive autonomous robot controller. Since electronic neuron circuit consists of several integrators, low power operational amplifiers are strongly required. A two stage operational amplifier architecture shown in Figure 3 is used. The current source is biased in the subthreshold region to allow subthreshold operation of the opamp [4],[5]. The gain of the two stage operational amplifier is represented by transconductance of the driver times the load resistance of each stage. The transconductance is $g_m = \frac{I_D}{nV_T}$, where I_D is related to the reference current as derived in Equation (9) from the current source (in Section 3.3). Then the gain of the subthreshold opamp can be modified as follows:

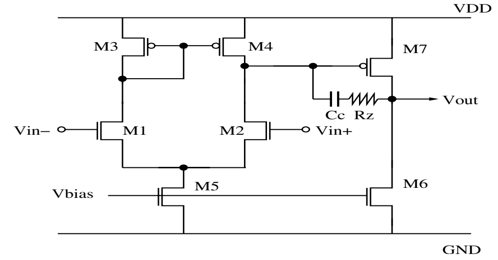


Fig. 3. Two Stage Subthreshold Operational Amplifier

$$A_{dc} = \left(\frac{\ln S}{nR_1}\right)(r_{o2}\|r_{o4})\left(\frac{\ln S}{nR_1}\right)(r_{o6}\|r_{o7}) \tag{7}$$

where

A_{dc} is the total gain of 2 stage amplifier, r_o is output resistance of transistor, n is slope factor, and S is a current

source area ratio $\left(= \frac{S_3 S_2}{S_1 S_4}\right)$.
Since the temperature term in g_m is canceled with V_T in current Equation (9), the gain is affected only by the temperature slope of early voltage or channel length modulation (r_o). Therefore, the gain is relatively constant and independent of temperature and process variations.

3.3. Current Source for OPAMP

A conventional PTAT current source for subthreshold bias shows poor performance due to process variation. To overcome this problem, a new current source circuit shown in Figure 4 is used [4],[5]. The process related sensitivities are significantly reduced due to sufficiently large loop gain introduced by the opamp. The equilibrium voltage and I_{ref} is given by

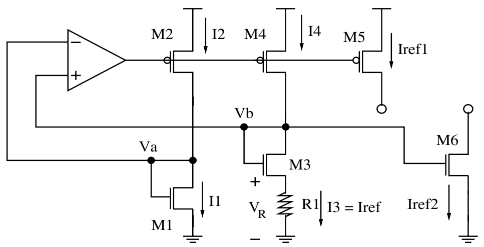


Fig. 4. Current Source Circuit

$$V_R = V_T \ln\left(\frac{S_3}{S_1}\frac{S_2}{S_4}\right) \tag{8}$$

where, $V_T = \frac{KT}{q}$

$$I_{ref} = \frac{V_R}{R_1} = \frac{V_T}{R_1}\ln\left(\frac{S_3}{S_1}\frac{S_2}{S_4}\right) \tag{9}$$

Consequently, the temperature coefficient (TC) of I_{ref} is

$$TC = \frac{1}{I_{ref}}\frac{\partial I_{ref}}{\partial T} = \frac{1}{T} - \frac{1}{R_1}\frac{\partial R_1}{\partial T} \tag{10}$$

Monte-carlo simulation is performed for both conventional and process-insensitive current source circuits, where the reference current is 500nA and V_{TH} is selected as a variable process parameter. The current variation of the circuit in Figure 4 is from 499.03nA to 501.77nA, while the conventional current circuit ranges from 489.81nA to 519.34nA.

3.4. Multiplier

The neuron circuit requires a multiplication function to produce square and cubic of variable x. The multiplier used for the adaptive analog controller is shown in Figure 5[6]. This architecture is simple and requires a low supply voltage. Also the output signal linearity is good because of its operation in the saturation region. Output of the multiplier is given by,

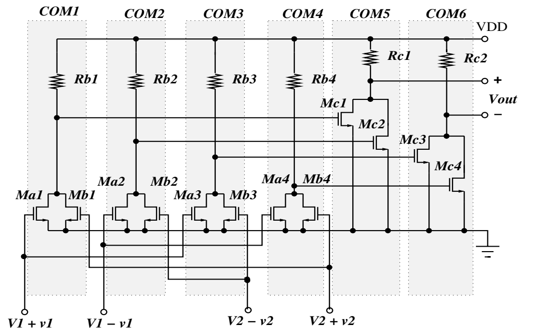


Fig. 5. The Multiplier Core Circuit.

$$v_{out} = \left[-32 R_c K_c (R_b)^2 K_b K_a (V_1 - V_{TH})(V_2 - V_{TH})\right] v_1 v_2 \tag{11}$$

To generate x^2 and x^3 terms using this multiplier, additional circuitry as shown in Figure 6 is required. Because of its nature of taking differential inputs and generating differential outputs, circuits generating complementary signal and making differential output to single-ended output are needed. An inverting amplifier is used to generate a complementary signal (denoted as Bar_Generator). For making single-ended output from a differential output, a difference amplifier with an attenuation network is used (denoted as Double_To_Single). $V_{Bar\_Generator}$ and $V_{Double\_To\_Single}$ are given by:

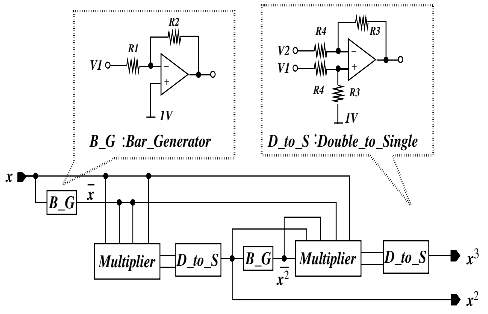


Fig. 6. Square and Cubic generation.

$$V_{Bar\_Generator} = \frac{R_2}{R_1} v_{in} \tag{12}$$

$$V_{Double\_To\_Single} = \frac{R_3}{R_4}(v_1 - v_2) \tag{13}$$

The resistor ratios $\frac{R_2}{R_1}$and $\frac{R_3}{R_4}$ are set to be unity for both cases. Positive terminals of the operational amplifier are biased at 1 volt due to the use of a single rail power supply ($V_{SS} = GND$ and $V_{DD} = 2V$). The connectivity among the multiplier core circuits, Bar_Generator, and Double_To_Single is shown in the Figure 6. The power consumption to generate x^2 and x^3 is only 82μwatt due to the fact that all the amplifiers are operating in the subthreshold region and the multiplier core is optimized for low power operation. The simulated x^2 and x^3 for a sine wave input x are shown in the Figure 7.

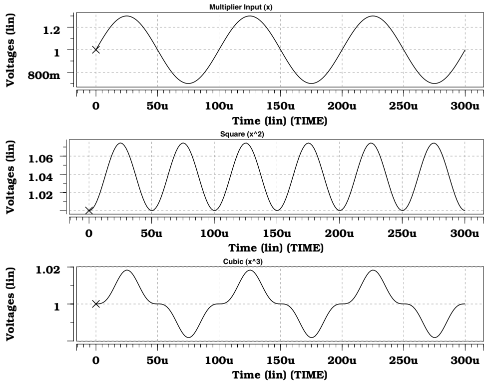


Fig. 7. x^2 and x^3 output waveform

3.5. MOS resistor

To implement the Equations (4),(5) and (6), the size of the resistors and capacitors used in integrators becomes a bottleneck for the integrated circuit. To satisfy the coefficients of neuron model, large capacitor or resistor values are required. Because capacitance consumes more area than resistance per square, capacitance values should be fixed as small as possible. Then resistor values are in the order of mega-ohm to satisfy time constants of differential equations. Because the output signal of the adaptive analog robot controller is chaotic, linearity is not a critical factor. Therefore, a single MOS transistor operating in the linear region is used to implement the resistor. This single MOS resistor's advantages are: 1) Area is smaller compared to other MRC(MOS Resistive Circuit) [7] circuits, which requires at least four MOS transistors. 2) Since all resistors are composed of unit transistor, MOS resistor shows good matching performance. 3) Special process step is not required. The only disadvantage is that it requires high gate voltage (V_g).

4. SIMULATION RESULT

The output waveform of the neuron circuit is shown in Figure 8. The waveforms of neuron circuit imitates the output of neuronal behavioral simulation except the fact that it is scaled down for integrated circuit. The global behavior depends on the input current I. If I is lower than the activation threshold (1.5V), the cell stays at rest as shown in Figure 8(c). Above the threshold, the cell begins to fire. The frequency of spikes per burst increases as I increases as shown in (a) I=2V, and (b) I=1.75

5. CONCLUSION

An electronic neuron circuit using 2V power supply is implemented using 0.25μm CMOS technology. The electronic neuron is able to mimic the behavior of actual biological neurons with real time adaptability. Each building block for the neuron circuit is designed for low power and small silicon area. Simulated results show that the output burst of electronic neuron changes dynamically for different input levels. This neuron circuit with synapse circuit is being used to build an adaptive analog controller for autonomous robots.

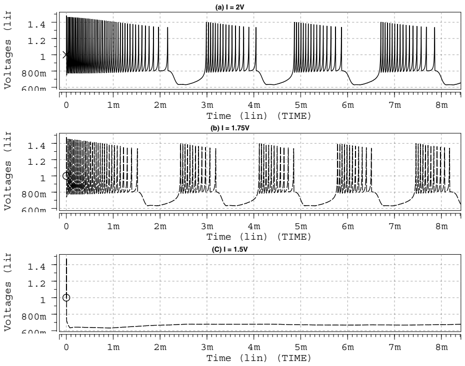


Fig. 8. Neuron Outputs

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