

A Low Power Methodology for Portable Electronics

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Abstract

This paper introduces a power savings methodology for portable electronics based on PowerWise™ Interface (PWI), leakage handling, and low power amplifier scheme. The PWI system dynamically monitors circuit performance with a slacktime detector, and provides a substantially constant minimum-supply voltage for digital processors to properly operate at a given frequency. Back-biasing preventing current from leaking becomes more important as the technology goes deeper. And the efficiency of power amplifiers affects battery lifetime directly. A dynamic power model is presented to calculate power savings and battery life time according to systems topology.

I. INTRODUCTION

The trend in electronics is to move more and more of the computing resources into portable and wireless applications. As a result, portable power handheld products and computers now account for nearly 10% of humanities' total power usage [1]. Battery charging efficiencies and cost of manufacturing power delivery systems and components represent a significant portion of this 10%. On the other hand, manufacturers are quickly realizing that size and run time demands of their portable equipment cannot be met by increasing energy density in batteries.

To achieve the leap in wireless devices' functionality and run time, first of all, manufacturers are turning to high efficiency energy management of system functions. Decreasing the amount of energy it takes to complete a function means the battery has more energy left for other processes. This energy management philosophy is being developed for several common wireless functional blocks such as DSP and micro-processor. Next, shrinking integrated circuit technology (<0.13μm) causes the amount of leakage to equal or exceed the portion of dynamic power dissipation. Unless the leakage is reduced, the power delivery in deep submicron era will ultimately restrict the ability of handheld to meet the customer demand for improved capabilities. Third, presently 2.5G GPRS/EDGE GSM which dominates the cellular market place uses relatively low efficiency linear power amplifiers (PAs) to achieve the required data rate as well as to meet multimode and

multiband requirement. PAs play a critical part in determining the power efficiency of a RF system because of their high output power levels, which can reach 3W for some cellular systems. As a result, the design of highly efficient PAs is of great importance to extend battery life time.

The focus of this paper is to address these power management approaches to save power for portable electronics at the aspects of dynamic power (Section II), static power (Section III), and RF PA power (Section IV). Section V shows a dynamic power model to demonstrate power savings and battery life time according to systems topology.

II. POWERWISE™ ADAPTIVE VOLTAGE SCALING

A. Overview

As semiconductor process technology has become lower-voltage and deeper sub-micron, and the number of transistors per chip has increased according to Moore's Law, two critical circuit design issues are presented: 1) the non-uniformity of process parameters within a single die; and 2) the increment of power consumption per die [2]-[3]. In deep sub-micron circuit design, variations due to the first issue cause differences in transistor and interconnect characteristics across a single die. They in turn impact the performance of circuit since they generate deviations in MOSFET drive current, resulting in propagation delay distributions of the critical path across a chip. Furthermore, the distribution of process parameters expands from die to die within a wafer as well as a lot. After fabrication, operating variations such as power

supply voltage, chip temperature and across-chip temperature also affect the propagation delay. By combining both operational and process induced variations, the propagation delay fluctuates to 18% ~ 32% [2]. The yield of CMOS logic circuits satisfying a specific performance requirement is significantly influenced by the magnitude of critical path delay deviations due to both operational and intrinsic parameter fluctuations. To compensate the impact of these parameter fluctuations and to achieve a desired yield, there are two approaches: 1) to reduce performance by operating at a lower clock frequency, and 2) to increase the supply voltage.

While the operating frequency limits allowable propagation delay, this delay strongly depends on intrinsic process parameters, supply voltage and junction temperature (PVT). The propagation delay in a MOSFET is proportional to the product of the active resistance of the MOSFET and load capacitance as in (1).

$$R_{ON} = \frac{V_{DD}}{\beta \cdot (V_{DD} - V_T)^\alpha} \quad (1)$$

$$C_L = C_D + C_G + C_W$$

where α is the velocity saturation term, β is the process transconductance parameter, V_{DD} is the supply voltage, V_T is the threshold voltage, C_D is the drain capacitance, C_G is the gate capacitance, and C_W is the interconnect capacitance.

If a design is fabricated as the best process corner, and is operating at low temperature, it needs less than $\frac{3}{4}$ of the minimum supply voltage required at the worst case [2]. Process parameters and operating junction temperature are not controllable, but supply voltage is. This results in chances to reduce power consumption by adjusting supply voltage with regard to process and temperature.

In many portable-computing devices such MP3-players and digital cameras, the full processing power of a processor is not required all the time. There are certain times when an operating frequency can be reduced, and a lower frequency means a longer allowable delay. This longer time margin also allows a supply voltage level to be lowered whereas the applied lower voltage increases the propagation delay. Since power consumption is quadratic with the supply voltage and proportional to operating frequency, reducing both operating frequency and supply voltage allows an excellent energy-efficient operation. This technique, adaptive voltage scaling (AVS), decreases power consumption without sacrificing performance provided performed tasks are finished within the allowed time. From the trade-off between performance and energy consumption, supplying just enough voltage to a system at a given frequency represents its optimum power consumption [4]-[7].

B. PowerWise™ Interface

National Semiconductor and ARM have teamed up to develop an AVS energy management system that reduces the energy consumption of a processor to the minimum amount for

a given clock frequency. This AVS method uses an open standard 2 wire, low power communication interface between the processor and the energy management unit (EMU) called PowerWise™ Interface (PWI) [8]. The two combined provide for an intelligent and aware energy management system.

AVS in the general sense refers to a power supply rail that adjusts its voltage corresponding to the demands of its load which could be any compliant electronic device. The enormous benefit of AVS is that for completing the same function, an AVS compliant processor will use 30% to 60% less energy than a fixed voltage processor. This is the kind of energy savings that will allow heavier use of our wireless devices while maintaining the operating time between charges. The way to reduce energy consumption in a processor, then, is to not only to reduce the clock frequency as low as possible, but, more importantly, to reduce the core supply voltage to the minimum amount for a given clock frequency.

The goal of the AVS system is to reduce the supply voltage to the minimum amount and still maintain critical path deadlines. Open loop AVS accomplishes this by regulating the supply voltage to a pre-characterized value that guarantees operation over process, temperature, and power supply variations. However, regulating to a pre-characterized voltage does not guarantee minimum energy consumption. This is guaranteed when the maximum propagation delay (and thus minimum voltage) is present for any given situation (frequency, process, temperature). Closed loop AVS in fact accomplishes this by regulating the propagation delay margin. In other words, no matter what lot the processor is from, nor the temperature or frequency it is operating at, the specified delay margin is maintained. Because of the voltage/propagation delay relationship, this condition necessarily requires that the supply voltage be at the acceptable minimum at all times.

As shown in Figure 1, the closed loop AVS system developed by National Semiconductor and ARM has two hardware components: the Intelligent Energy Manager™ (IEM) and Adaptive Power Controller (APC), located in the processor, and the AVS compliant energy management unit (EMU). The ARM IEM determines the minimum performance (clock frequency) required by the processor for given tasks. The APC accepts a performance request from the IEM and determines the minimum voltage the processor can operate at for that performance level. It also commands the EMU to attain the lowest supply voltage for a given clock frequency. It is important to realize that the APC is synthesizable code operating in the processor, and it manages the IEM requests and voltage control without any intervention from the processor. All the software hooks for controlling performance are contained in the IEM. The APC controls the supply voltage transparent to the IEM, however it is coupled to the external EMU. The AVS EMU is equipped to interpret commands from the APC through a new open standard interface, PowerWise™ Interface (PWI). PWI is a low power, 2 pin serial protocol specifically designed to meet the needs of next generation AVS portable systems.

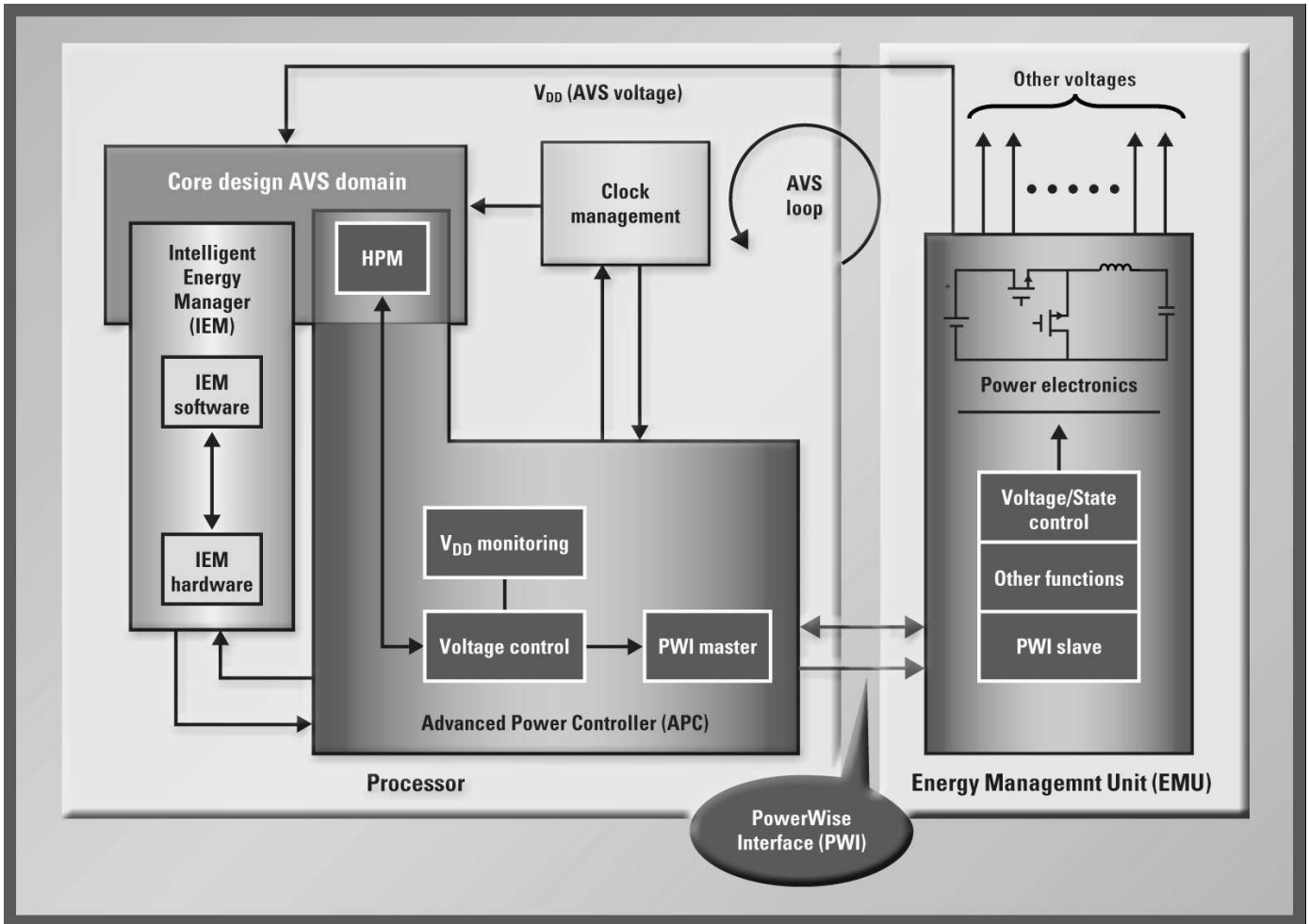


Figure 1: The closed loop AVS system consists of an Intelligent Energy Manager (IEM) and Adaptive Power Controller (APC) located in the processor, and an Energy Management Unit (EMU). The AVS loop regulates propagation delay margin to ensure the minimum supply voltage is achieved.

Closed loop AVS is distinguished from open loop, table based voltage scaling techniques in that it regulates the propagation delay margin in logic cells. In this system, the power supply voltage is a variable that increases or decreases, and the delay margin is a fixed parameter that is regulated over parts, temperature, and clock frequency. Many advantages arise from this methodology. Closed loop AVS relaxes the characterization process. There is no need for characterizing voltage/frequency tables because a delay margin is maintained by the AVS feedback loop. Another incentive is that less demand is placed on power supply regulation. The AVS loop adjusts the supply voltage as necessary, compensating for the $\pm 5\%$ tolerance typically allocated to power supply regulation. By and far the most beneficial advantage is that the minimum operating voltage is realized for all conditions, and can dynamically change as conditions change. For example, as temperature changes, the cell delays change, and the voltage is adjusted to maintain the same delay margin – without using voltage/frequency tables. Figure 2 shows this temperature compensation. By using closed loop AVS, the designer can rest assured that the minimum voltage is being applied for any given clock frequency.

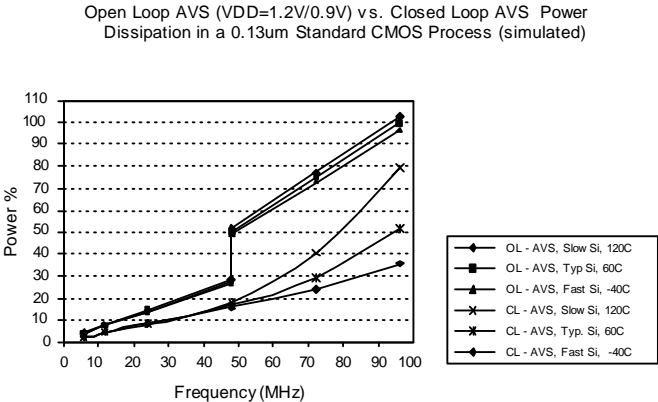


Figure 2: Power dissipation comparison between Open loop AVS and Closed Loop AVS. Closed loop AVS tracks temperature and process variations, and yields significant power savings over open loop AVS. The open loop method uses two voltages (1.2V between 48MHz and 96MHz, and 0.9V between 6MHz and 48MHz).

III. BACK BIAS LEAKAGE CONTROL

A. Overview

Static power dissipation is an important design criteria for modern battery powered portable devices since it can significantly impact battery life. The current trend is for increasing functionality in portable devices provided by complex system-on-chip ICs implemented in deep submicron processes. With each step improvement in transistor scaling the supply voltage V_{dd} is lowered. However in order to maintain performance, the threshold voltage V_t is also lowered to compensate for scaling in V_{dd} . This has the undesirable effect of increasing the drain-to-source leakage current I_{off} when the application IC is in standby. In some applications such as cell phones the static power dissipation of the application ICs can be as much as 40% of the total static power dissipation.

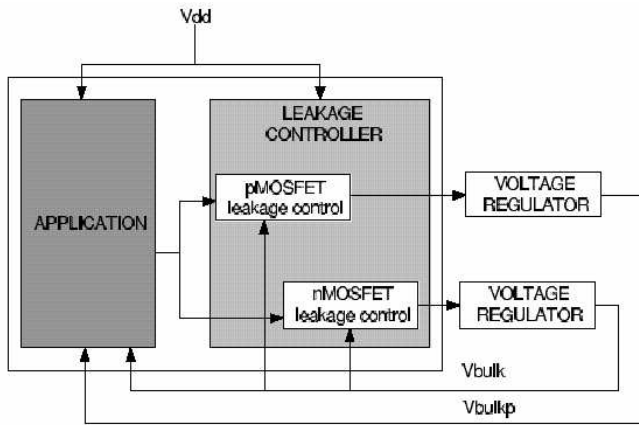


Figure 3: Block diagram of scheme with well regulators.

The use of reverse body bias has been demonstrated as an effective technique to reduce the total static power dissipation by reducing the total static (leakage) current I_{off} drained from the battery [9]. This technique is attractive to implement (as shown in the high level block diagram of Figure 3) because of the following reasons:

- it requires no changes to the process technology and can be used along with other leakage control techniques,
- the reverse body bias regulator can be implemented off-chip and incorporated into an external power management IC,
- it allows state retention upon standby (as opposed to another leakage control technique known as MTCMOS [10]),
- alternatively forward body bias can be applied to an application IC to reduce V_t variations at the expense of increased active power consumption [11].

B. Approaches on-chip leakage monitoring

1) Leakage controlled sawtooth oscillator

The circuit shown in Figure 4 can tightly track the on-chip leakage current. A simple sawtooth oscillator design is driven

by the leakage current of an NMOS transistor¹. During each cycle, the capacitor C_{gs} is charged to V_{dd} . When transistor M_1 is turned off, leakage current will discharge the capacitor until the threshold voltage of the inverter is reached. To prevent crowbar current between V_{dd} and ground, a positive feedback circuit rapidly switches the inverter output. After a small delay the capacitor is again charged to V_{dd} and the cycle repeats. The sawtooth input to a counter. The counter operates off a low-frequency clock (such as 32kHz). Hence, the output of the counter is a digital number that is proportional to the leakage current. Simple control logic sweeps the reverse body bias voltage and determines the smallest count that represents the optimal body bias voltage.

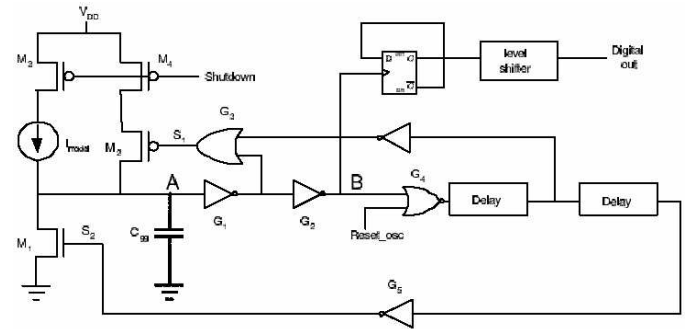


Figure 4: Leakage controlled sawtooth oscillator.

The circuit is capable of detecting leakage currents from a few pAs to several hundred μ As. At the lower end of the scale, the circuit can take long evaluation time (slow discharge of C_{gs}) and at the upper end of the scale, a high frequency oscillation consumes dynamic power from V_{dd} . Hence, the scheme is designed with split current sources that can be selected to provide the appropriate current input for a given operating condition (V_{dd} and temperature). The worst case average current consumed over $10ms^2$ evaluation period is determined by simulation to be $75 \mu A$.

2) Curve traversal algorithm for leakage detection

The circuit shown in Figure 5 will follow the leakage current curve until a reversal in the leakage current slope is observed (Figure 6). The circuit interprets this reversal to imply that (a) prior to the reversal, increasing the reverse body bias voltage decreases I_{off} and (b) after the reversal, increasing the body bias voltage increases I_{off} since the optimum body bias point has been crossed. Following this reversal the circuit will attempt to fine-tune the body bias voltage. The tradeoff is between a body bias voltage close to the optimum value and increased time for leakage current evaluation. The circuit is initialized at a body bias voltage which is lower than the optimum voltage. Traversal is simply done by determining whether the capacitor C_1 can be discharged in a given sample

¹ for a PMOS transistor the leakage current source is.

² this simulation model assumes that temperature shifts on chip occur at a time constant of about 10ms. Hence the leakage current monitor could be activated every 10ms. Once the evaluation is complete, the leakage monitor is shut down for the remaining part of the 10ms time period.

period. C_1 is comprised of individual capacitors and can be calibrated during initialization by the control logic. The sample period can be changed by factors of 2 to accommodate a larger variation in the leakage current. Once the reversal of leakage current is detected, the sampling time is increased and the leakage current can be monitored with higher resolution. Since there is no oscillator circuit to consumer dynamic power, this circuit scheme consumes very little current. Circuit simulations show an average current consumption of $7\mu\text{A}$ over a period of 10 ms.

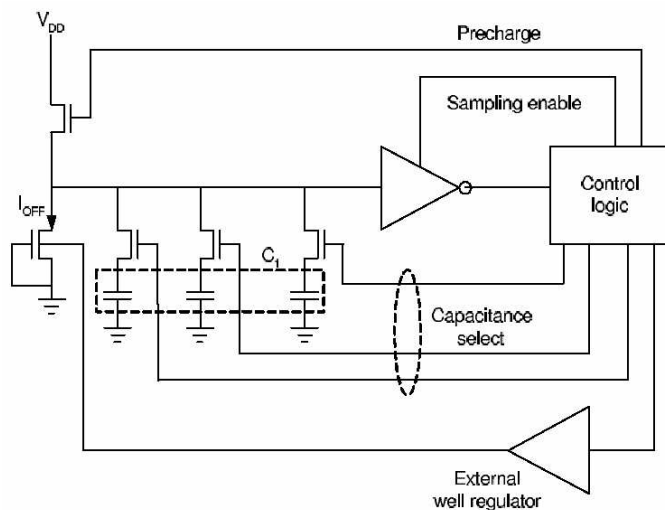


Figure 5: A circuit to traverse the leakage current curve.

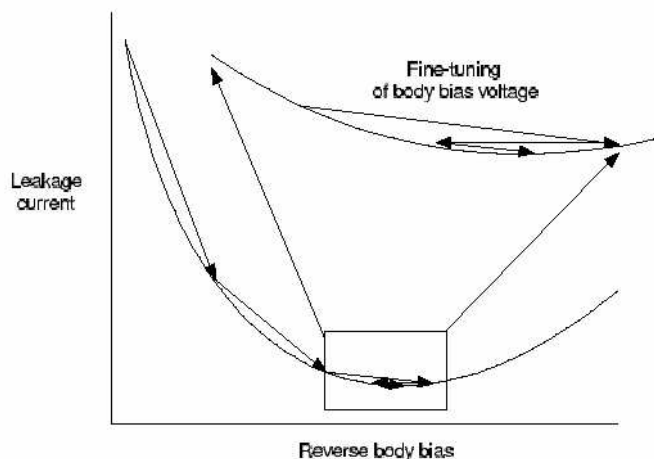


Figure 6: Illustration of the curve traversal.

IV. HIGH EFFICIENCY POWER AMPLIFIERS

A. Overview

The spread-spectrum wireless communications standard, 3GPP, requests stringent specifications for linearity and adjacent-channel power ratio (ACPR). To meet the 3GPP specifications, wideband-code-division multiple access (W-CDMA) wireless handsets require highly linear Class A or Class A-B RF power amplifiers (PAs). The power-added efficiency (PAE) for that type of PA, however, is about 35% maximum at an output power of +28 dBm. And the PA operates

discontinuously in voice mode. Without speaking, it runs at a half rate (50 percent of the time) or at a one-eighth rate. However, in data mode the PA runs continuously during transmitting the data transmission. Combining the PA's low efficiency and continuous operation results in discharging the battery quickly, and in turn may cause the phone too hot. Therefore, the most inefficient circuit in a cell phone is the RF PA.

On the other hand, demand for multi-mode and multi-band operation, longer battery life, and smaller size in cellular equipment is increasing [12]. To achieve multimode operation, transmitters must be able to accommodate constant envelope signals as well as non-constant envelope signals. Therefore, to avoid distortion of non-constant envelopes, conventional transmitters has to employ linear power amplifier (class-A) or use predistortion techniques to linearize slightly saturated amplifiers (class-AB). Linearity and power efficiency in transmit front ends are conflicting requirements demanding innovative solutions for present and future wireless mobile systems. Therefore, the design of PA linearising and efficiency improvement schemes, and architectures, is attracting much attention in recent years, including feedforward, envelope elimination and restoration (EER), Cartesian feedback, and predistortion techniques [13]-[16].

B. A Polar EDGE CMOS PA Controller with Flat Amplitude and Phase Response

A polar modulation is presented for the multimode multiband operation with high power efficiency because it uses amplifiers in the switched mode. The function of a PA control chip is to maintain an accurate control voltage when variations of process, supply voltage, and temperature are encountered. In the presented approach, an open loop method [17] is adopted in order to avoid the problematic issues of closed-loop power control such as non-linearity between PA and detector, small dynamic range, long calibration time, inaccurate current detector, and cost. The open loop design as shown in Figure 7 covers multiband and multimode such as GSM, DCS, PCS, GPRS and EDGE. The goal of this section is to design a high efficiency amplitude-tracking circuit to improve transmit power efficiency versus time. The incentive to use a CMOS technology is based on the per-unit-area cost which is roughly $\frac{1}{2}$ size of BiCMOS.

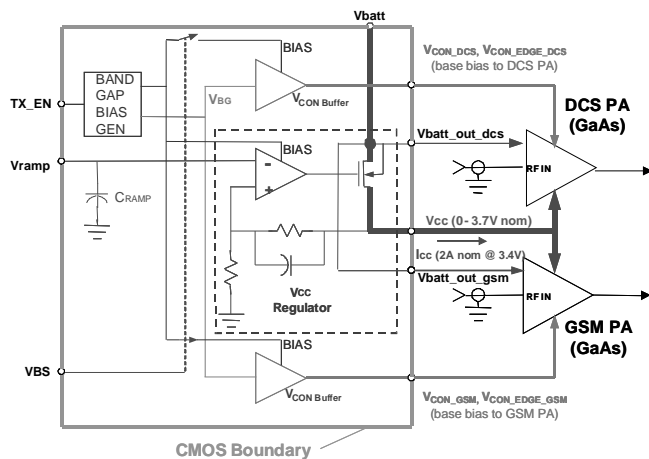


Figure 7: Block diagram of LM4401 with external PAs.

To reduce PSRR and circuit parameter sensitivities, each circuit module provides higher gain than its function requires. First of all, a bandgap (100 μ A) is optimized for both low noise and offset without a trim ($\pm 3\%$ maximum tolerance) where a folded cascode P-channel input stage eliminates the potential for shut down due to the input stage being biased below the threshold ($V_{be} < V_t$). In order to reduce noise, the bandwidth of the reference is also reduced, and a grounding in the immediate location to the bandgap is utilized to minimize coupling noise. Second, a P-channel shunt circuit is required to make sure no charge on nodes driving outputs. The input circuit uses a trickle subthreshold current source pull-down which is operational during initial power on. The TX enable completely shuts off all supplies and references but allows the input inverter to sense the power. A Schmitt trigger master slave implementation overcomes high standby current ($\sim 10\mu$ A) issues due to a high value resistor tied directly to the 2.9V supply. Third, a folded cascode LDO amplifier with an internal bandgap reference is utilized to make the input stage independent of supply voltage variations. The main power LDO is a circuit capable of delivering more than 4A of peak current to RF PA in a cell phone handset. And a high bandwidth bias amplifier slews in less than 1 μ s into a 56 Ω load with a 0.1 μ F capacitance in order to keep the quiescent current relatively constant into a load. Its bandwidth is approximately 2 MHz. An input level shifter utilizes a “diode” connected P-channel in series with an inverter to provide a 1.5 volt to 5.5 volt interface.

The P-channel power driver FET is a unique bent gate approach to maximize conductance and in turn to provide the lowest R_{ds} on per unit area in CMOS without latchup. Next, a power down circuit technique separates the circuit from the supply by using an N-channel switch with all of the analog active circuitry (N-channel sources connected to ground). This technique eliminates the need for an input supply reference voltage required by an inverter input stage. This results in a standby current of less than 1 μ A. The sum of the entire power down current and leakage current is less than 10 μ A over process voltage and temperature including pull up and pull down currents. Finally, a dedicate 1.6V reference is developed in order to provide an isolated direct reference for the input clamp. This clamps the input (Vramp) from ever allowing the

output to go beyond 3.7V. On the other hand, a separate 2.8V reference is used to set the input stage supply voltage of the VCC amplifier which drives to the collector of the PA. Making this node supply independent (fixed 2.8V) results in more controllable operation over the input common mode range (0~1.6V) as well as improved supply noise rejection.

The PA controller has a linear gain (2.6) transfer response from the DAC of a baseband to the output power of the PA to meet multi-mode specifications. The PA control loop is accurate, temperature-stable and fast enough to meet the turn-on time requirement ($< 3\mu$ s). The bias amplifier is able to deliver 50mA with a load capacitance up to 0.1 μ F. The supply controller precisely tracks the DAC’s input voltage and slews at better than 2V/ μ s into 1.7 Ω and 0.1 μ F capacitive load. Group delay variation of better than ± 10 ns over a bandwidth of 10 KHz to 3MHz without trim is realized with a potential to extend this to greater than 7MHz for WCDMA applications as shown in Figure 8. The gain flatness is also dramatically improved when the region of interest is moved near the band edge. This implies that bandwidth of the amplifier is increased. A reproducible and consistent gain characteristic is achieved as shown in Figure 9. This eliminates the need for costly active trim or calibration. Amplitude variation of less than ± 0.3 dB has been simulated to 3MHz which meets the requirements for WCDMA and polar EDGE. Since the bandwidth and gain of an amplifier are inversely related to the square root of the area divided by the current through the device, reducing the input channel length effectively increases the bandwidth without adversely affecting the gain. Interbusrt recovery time is less than 3 μ s settling to 10mV with typical off standby current less than 10 μ A including input control pull down current. Spot noise at 10MHz is less than 24nv/rtHz for both the bias amplifiers and the power LDO.

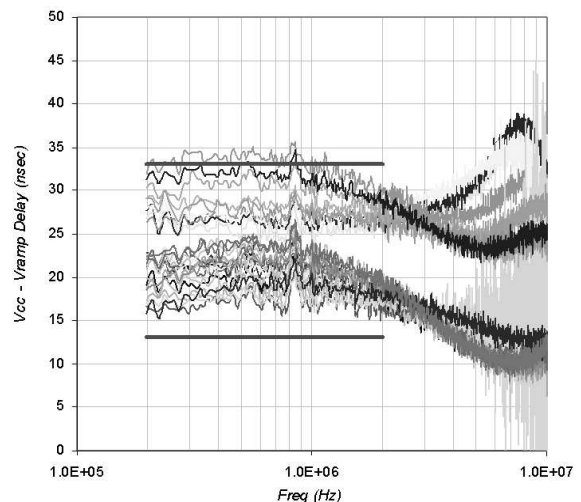


Figure 8: Group delay vs. frequency (Measured).

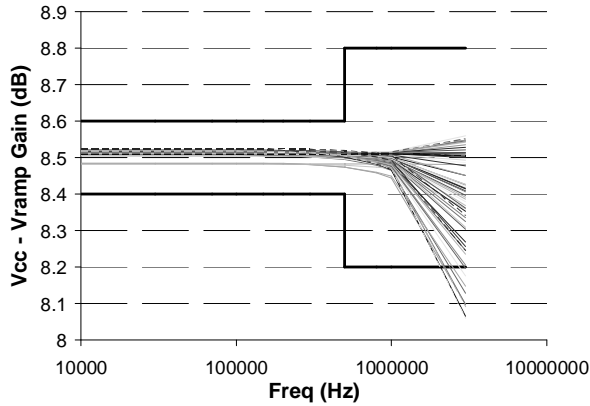


Figure 9: Gain vs. frequency.

Table 1. Features of LM4401.

Key Performance Limits	Min	Max	Units	Condition
Gain Flatness	-0.3	0.3	dB	1.5MHz
Group Delay Flatness		2	ns	
Group Delay Variation	10	30	ns	
LDO Bandwidth	25		MHz	
LDO Noise		24	nV/rtHz	10MHz
Power down Leakage		10	μA	
Supply Voltage	2.9	4.8	V	
Total Standby Current		25	mA	
Turn Time		3	μs	
Load Resistor		1	Ω	2A
Load Capacitor		0.1	μF	

And the linear CMOS controller is used with GaAs HBTs PA providing better than 37 dBc adjacent channel performance with peak efficiency of better than 40%. Not only does this power controller provide up to 4A supply current, it also is able to properly perform with temperatures exceeding 150°C. Significant improvement in performance, noise, and linearity are realized together with ruggedness enhancements including input clamping and offset techniques as shown in Table 1.

V. DYNAMIC POWER MODEL

A dynamic Excel spreadsheet as shown in Figure 10 is developed to show the improvements as a function of system demand requirements. Sliders or radial buttons can be used to determine the battery life in Figure 11 and power savings in Figure 12.

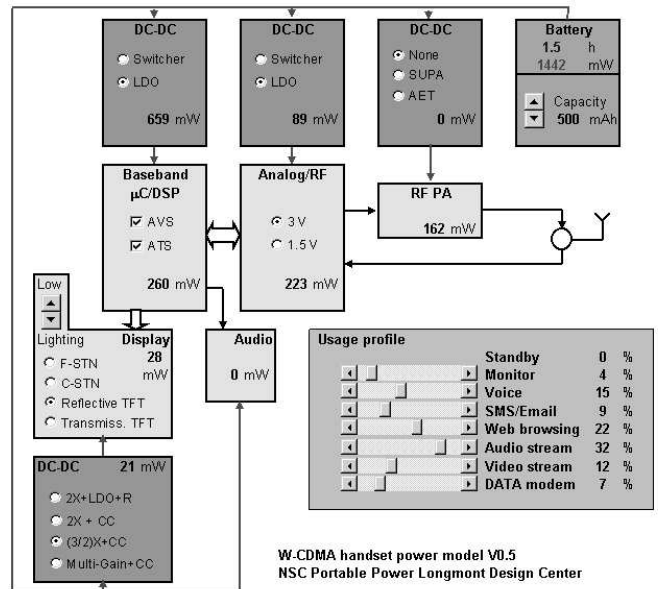


Figure 10: Dynamic Power Model.

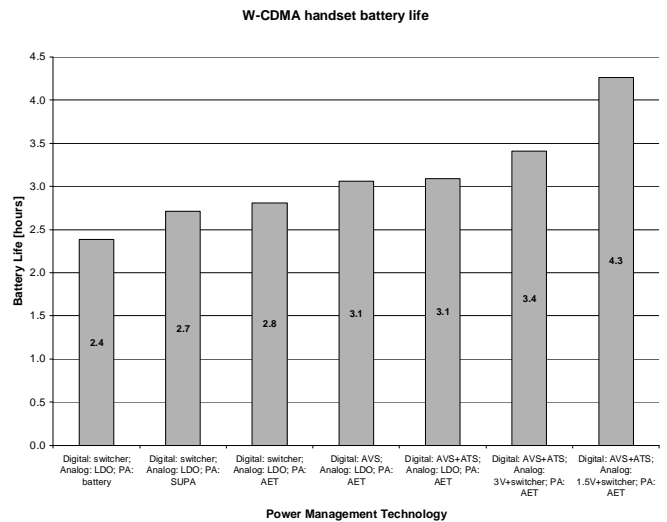


Figure 11: An example of battery life time calculation.

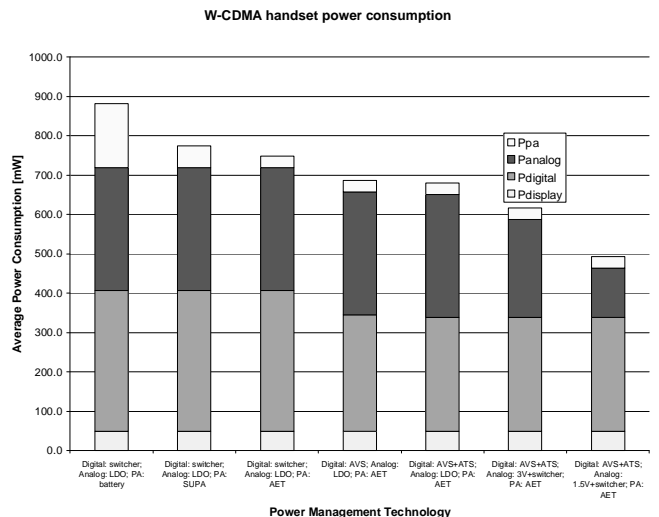


Figure 12: An example of power savings calculation.

VI. CONCLUSION

A power savings methodology for portable electronics has been described. Portable electronics are very vulnerable as the technology trend goes more complex and more power consuming because their power source depends on only a battery. Therefore, high energy-efficiency systems are required to extend the battery life time. Moreover, as RF products among consumer electronics are prevalent, their energy consumption becomes a major part of total home electronic products. As a result, the presented low power methodology will leverage the energy savings of total consumer electronics.

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